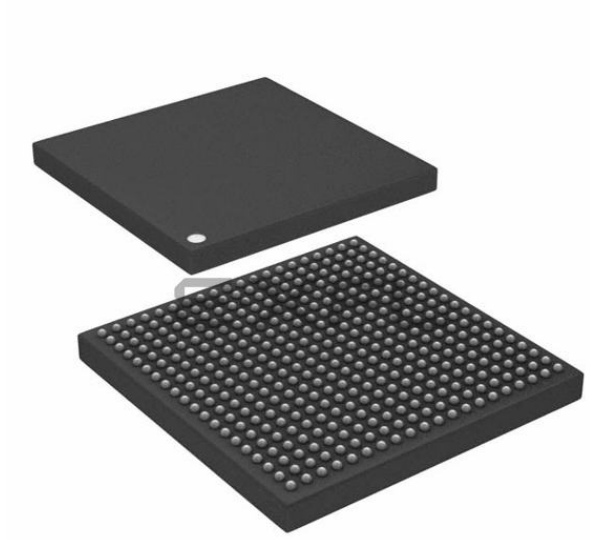

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART, USB
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	260kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf548bbcz-5aa

includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}) bits per second.
- Supporting data formats from seven to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

UART1 and UART3 feature a pair of $\overline{\text{UARTxRTS}}$ (request to send) and $\overline{\text{UARTxCTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UARTxCTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UARTxRTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

CONTROLLER AREA NETWORK (CAN)

The ADSP-BF54x Blackfin processors offer up to two CAN controllers that are communication controllers that implement the controller area network (CAN) 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network since the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The ADSP-BF54x Blackfin processors' CAN controllers offer the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- CAN wakeup from hibernation mode (lowest static power consumption mode).
- Interrupts, including: TX complete, RX complete, error and global.

The electrical characteristics of each network connection are very demanding, so the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The ADSP-BF54x Blackfin processors' CAN module represents only the controller part of the interface. The controller interface supports connection to 3.3 V high speed, fault-tolerant, single-wire transceivers.

An additional crystal is not required to supply the CAN clock, as the CAN clock is derived from the processor system clock (SCLK) through a programmable divider.

TWI CONTROLLER INTERFACE

The ADSP-BF54x Blackfin processors include up to two 2-wire interface (TWI) modules for providing a simple exchange method of control data between multiple devices. The modules are compatible with the widely used I^2C bus standard. The TWI modules offer the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. Each TWI interface uses two pins for transferring clock (SCLx) and data (SDAx), and supports the protocol at speeds up to 400K bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the ADSP-BF54x Blackfin processors' TWI modules are fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

PORTS

Because of their rich set of peripherals, the ADSP-BF54x Blackfin processors group the many peripheral signals to ten ports—referred to as Port A to Port J. Most ports contain 16 pins, though some have fewer. Many of the associated pins are shared by multiple signals. The ports function as multiplexer controls. Every port has its own set of memory-mapped registers to control port muxing and GPIO functionality.

PIN DESCRIPTIONS

The ADSP-BF54x processor pin multiplexing scheme is shown in Table 10.

Table 10. Pin Multiplexing

Primary Pin Function (Number of Pins)[1, 2]	First Peripheral Function	Second Peripheral Function	Third Peripheral Function	Fourth Peripheral Function	Interrupt Capability
Port A					
GPIO (16 pins)	SPORT2 (8 pins)	TMR4 (1 pin)	TACI7 (1 pin) TACLK7–0 (8 pins)		Interrupts (16 pins)
		TMR5 (1 pin)			
	SPORT3 (8 pins)	TMR6 (1 pin)			
		TMR7 (1 pin)			
Port B					
GPIO (15 pins)	TWI1 (2 pins) UART2 or 3 CTL (2 pins) UART2 (2 pins) UART3 (2 pins)		TACI2-3 (2 pins)		Interrupts (15 pins)
	$\overline{\text{SPI2 SEL1-3}}$ (3 pins)	TMR0–2 (3 pins)			
	SPI2 (4 pins)	TMR3 (1 pin)	HWAIT (1 pin)		
Port C					
GPIO (16 pins)	SPORT0 (8 pins)	MXVR MMCLK, MBCLK (2 pins)			Interrupts (8 pins)[3]
	SDH (6 pins)				Interrupts (8 pins)
Port D					
GPIO (16 pins)	PPI1 D0–15 (16 pins)	Host D0–15 (16 pins)	SPORT1 (8 pins)	PPI0 D18– 23 (6 pins)	Interrupts (8 pins)
			PPI2 D0–7 (8 pins)	Keypad Row 0–3 Col 0–3 (8 pins)	Interrupts (8 pins)
Port E					
GPIO (16 pins)	SPI0 (7 pins)	Keypad Row 4–6 Col 4–7 (7 pins)	TACI0 (1 pin)		Interrupts (8 pins)
	UART0 TX (1 pin)	Keypad R7 (1 pin)			
	UART0 RX (1 pin) UART0 or 1 CTL (2 pins) PPI1 CLK,FS (3 pins) TWI0 (2 pins)				Interrupts (8 pins)
Port F					
GPIO (16 pins)	PPI0 D0–15 (16 pins)	ATAPI D0-15A			Interrupts (8 pins) Interrupts (8 pins)
Port G					
GPIO (16 pins)	PPI0 CLK,FS (3 pins) DATA 16–17 (2 pins)	TMRCLK (1 pin)			Interrupts (8 pins)
		ATAPI A0-2A			
	$\overline{\text{SPI1 SEL1–3}}$ (3 pins)	Host CTL (3 pins)	PPI2 CLK,FS (3 pins)	CZM (1 pin)	
	SPI1 (4 pins)	MXVR $\overline{\text{MTXON}}$ (1 pin)	TACI4-5 (2 pins)		Interrupts (8 pins)
	CAN0 (2 pins)				
	CAN1 (2 pins)				

Table 11. Pin Descriptions

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port A: GPIO/*SPORT2–3/TMR4–7*			
PA0/*TFS2*	I/O	GPIO/*SPORT2 Transmit Frame Sync*	C
PA1/*DT2SEC/TMR4*	I/O	GPIO/*SPORT2 Transmit Data Secondary/Timer 4*	C
PA2/*DT2PRI*	I/O	GPIO/*SPORT2 Transmit Data Primary*	C
PA3/*TSCLK2*	I/O	GPIO/*SPORT2 Transmit Serial Clock*	A
PA4/*RFS2*	I/O	GPIO/*SPORT2 Receive Frame Sync*	C
PA5/*DR2SEC/TMR5*	I/O	GPIO/*SPORT2 Receive Data Secondary/Timer 5*	C
PA6/*DR2PRI*	I/O	GPIO/*SPORT2 Receive Data Primary*	C
PA7/*RSCLK2/TACLK0*	I/O	GPIO/*SPORT2 Receive Serial Clock/Alternate Input Clock 0*	A
PA8/*TFS3/TACLK1*	I/O	GPIO/*SPORT3 Transmit Frame Sync/Alternate Input Clock 1*	C
PA9/*DT3SEC/TMR6*	I/O	GPIO/*SPORT3 Transmit Data Secondary/Timer 6*	C
PA10/*DT3PRI/TACLK2*	I/O	GPIO/*SPORT3 Transmit Data Primary/Alternate Input Clock 2*	C
PA11/*TSCLK3/TACLK3*	I/O	GPIO/*SPORT3 Transmit Serial Clock/Alternate Input Clock 3*	A
PA12/*RFS3/TACLK4*	I/O	GPIO/*SPORT3 Receive Frame Sync/Alternate Input Clock 4*	C
PA13/*DR3SEC/TMR7/TACLK5*	I/O	GPIO/*SPORT3 Receive Data Secondary/Timer 7/Alternate Input Clock 5*	C
PA14/*DR3PRI/TACLK6*	I/O	GPIO/*SPORT3 Receive Data Primary/Alternate Input Clock 6*	C
PA15/*RSCLK3/TACLK7 and TACI7*	I/O	GPIO/*SPORT3 Receive Serial Clock/Alt Input Clock 7 and Alt Capture Input 7*	A
Port B: GPIO/*TWI1/UART2–3/SPI2/TMR0–3*			
PB0/*SCL1*	I/O	GPIO/*TWI1 Serial Clock* (Open-drain output: requires a pull-up resistor.)	E
PB1/*SDA1*	I/O	GPIO/*TWI1 Serial Data* (Open-drain output: requires a pull-up resistor.)	E
PB2/$\overline{\textit{UART3RTS}}$	I/O	GPIO/*UART3 Request to Send*	C
PB3/$\overline{\textit{UART3CTS}}$	I/O	GPIO/*UART3 Clear to Send*	A
PB4/*UART2TX*	I/O	GPIO/*UART2 Transmit*	A
PB5/*UART2RX/TACI2*	I/O	GPIO/*UART2 Receive/Alternate Capture Input 2*	A
PB6/*UART3TX*	I/O	GPIO/*UART3 Transmit*	A
PB7/*UART3RX/TACI3*	I/O	GPIO/*UART3 Receive/Alternate Capture Input 3*	A
PB8/$\overline{\textit{SPI2SS}}$/*TMR0*	I/O	GPIO/*SPI2 Slave Select Input/Timer 0*	A
PB9/$\overline{\textit{SPI2SEL1}}$/*TMR1*	I/O	GPIO/*SPI2 Slave Select Enable 1/Timer 1*	A
PB10 $\overline{\textit{SPI2SEL2}}$/*TMR2*	I/O	GPIO/*SPI2 Slave Select Enable 2/Timer 2*	A
PB11/$\overline{\textit{SPI2SEL3}}$/*TMR3/HWAIT*	I/O	GPIO/*SPI2 Slave Select Enable 3/Timer 3/Boot Host Wait*	A
PB12/*SPI2SCK*	I/O	GPIO/*SPI2 Clock*	A
PB13/*SPI2MOSI*	I/O	GPIO/*SPI2 Master Out Slave In*	C
PB14/*SPI2MISO*	I/O	GPIO/*SPI2 Master In Slave Out*	C

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port I: GPIO/*AMC*			
PI0/*A10*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI1/*A11*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI2/*A12*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI3/*A13*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI4/*A14*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI5/*A15*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI6/*A16*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI7/*A17*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI8/*A18*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI9/*A19*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI10/*A20*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI11/*A21*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI12/*A22*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI13/*A23*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI14/*A24*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI15/*A25/NR_CLK*[6]	I/O	GPIO/*Address Bus for Async Access/ NOR clock*	A
Port J: GPIO/*AMC/ATAPI*			
PJ0/*ARDY*/$\overline{WAIT}$	I/O	GPIO/ *Async Ready/NOR Wait*	A
PJ1/$\overline{ND\_CE}$[7]	I/O	GPIO/*NAND Chip Enable*	A
PJ2/$\overline{ND\_RB}$	I/O	GPIO/*NAND Ready Busy*	A
PJ3/$\overline{ATAPI\_DIOR}$	I/O	GPIO/*ATAPI Read*	A
PJ4/$\overline{ATAPI\_DIOW}$	I/O	GPIO/*ATAPI Write*	A
PJ5/$\overline{ATAPI\_CS0}$	I/O	GPIO/*ATAPI Chip Select/Command Block*	A
PJ6/$\overline{ATAPI\_CS1}$	I/O	GPIO/*ATAPI Chip Select*	A
PJ7/$\overline{ATAPI\_DMACK}$	I/O	GPIO/*ATAPI DMA Acknowledge*	A
PJ8/$\overline{ATAPI\_DMARQ}$	I/O	GPIO/*ATAPI DMA Request*	A
PJ9/*ATAPI_INTRQ*	I/O	GPIO/*Interrupt Request from the Device*	A
PJ10/$\overline{ATAPI\_IORDY}$	I/O	GPIO/*ATAPI Ready Handshake*	A
PJ11/$\overline{BR}$[8]	I/O	GPIO/*Bus Request*	A
PJ12/$\overline{BG}$[6]	I/O	GPIO/*Bus Grant*	A
PJ13/$\overline{BGH}$[6]	I/O	GPIO/*Bus Grant Hang*	A

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
DDR Memory Interface			
DA0–12	O	DDR Address Bus	D
DBA0–1	O	DDR Bank Active Strobe	D
DQ0–15	I/O	DDR Data Bus	D
DQS0–1	I/O	DDR Data Strobe	D
DQM0–1	O	DDR Data Mask for Reads and Writes	D
DCLK0–1	O	DDR Output Clock	D
$\overline{\text{DCLK0–1}}$	O	DDR Complementary Output Clock	D
$\overline{\text{DCS0–1}}$	O	DDR Chip Selects	D
DCLKE[9]	O	DDR Clock Enable (Requires a pull-down if hibernate with DDR self-refresh is used.)	D
$\overline{\text{DRAS}}$	O	DDR Row Address Strobe	D
$\overline{\text{DCAS}}$	O	DDR Column Address Strobe	D
$\overline{\text{DWE}}$	O	DDR Write Enable	D
DDR_VREF	I	DDR Voltage Reference	
DDR_VSSR	I	DDR Voltage Reference Shield (Must be connected to GND.)	
Asynchronous Memory Interface			
A1-3	O	Address Bus for Async and ATAPI Addresses	A
D0-15/ND_D0-15/ATAPI_D0-15	I/O	Data Bus for Async, NAND and ATAPI Accesses	A
$\overline{\text{AMS0–3}}$	O	Bank Selects (Pull high with a resistor when used as chip select. Require pull-ups if hibernate is used.)	A
$\overline{\text{ABE0}}$ / *ND_CLE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Command Latch Enable*	A
$\overline{\text{ABE1}}$ / *ND_ALE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Address Latch Enable*	A
$\overline{\text{AOE}}$ / *NR_ADV*	O	Output Enable / *NOR Address Data Valid*	A
$\overline{\text{ARE}}$	O	Read Enable / *NOR Output Enable*	A
$\overline{\text{AWE}}$	O	Write Enable	A
ATAPI Controller Pins			
$\overline{\text{ATAPI\_PDIAG}}$	I	Determines if an 80-pin cable is connected to the host. (Pull high or low when unused.)	
High Speed USB OTG Pins			
USB_DP	I/O	USB D+ Pin (Pull low when unused.)	
USB_DM	I/O	USB D– Pin (Pull low when unused.)	
USB_XI	C	Clock XTAL Input (Pull high or low when unused.)	
USB_XO	C	Clock XTAL Output (Leave unconnected when unused.)	
USB_ID[10]	I	USB OTG ID Pin (Pull high when unused.)	

Parameter		Test Conditions	Nonautomotive 400 MHz[1] Min	Typ	Max	All Other Devices[2] Min	Typ	Max	Unit
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.10 V, f_{CCLK} = 300 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		145			178		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.20 V, f_{CCLK} = 400 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		199			239		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.25 V, f_{CCLK} = 533 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00					301		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.35 V, f_{CCLK} = 600 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00					360		mA
$I_{DDHIBERNATE}$[13, 14]	Hibernate State Current	V_{DDEXT} = V_{DDVR} = V_{DDUSB} = 3.30 V, V_{DDDDR} = 2.5 V, T_J = 25°C, CLKIN= 0 MHz with voltage regulator off (V_{DDINT} = 0 V)		60			60		µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDUSB-FS}$	V_{DDUSB} Current in Full/Low Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, Full Speed USB Transmit		9			9		mA
$I_{DDUSB-HS}$	V_{DDUSB} Current in High Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, High Speed USB Transmit		25			25		mA
$I_{DDDEEPSLEEP}$[13, 15]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 16			Table 17	mA
$I_{DDSLEEP}$[13, 15]	V_{DDINIT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (0.77 × V_{DDINT} × f_{SCLK})[16]			$I_{DDDEEPSLEEP}$ + (0.77 × V_{DDINT} × f_{SCLK})[16]	mA[16]
I_{DDINT}[15, 17]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} > 0 MHz			$I_{DDSLEEP}$ + (Table 19 × ASF)			$I_{DDSLEEP}$ + (Table 19 × ASF)	mA

[1] Applies to all nonautomotive 400 MHz speed grade models and all extended temperature grade models. See Ordering Guide.
[2] Applies to all 533 MHz and 600 MHz speed grade models and automotive 400 MHz speed grade models. See Ordering Guide.
[3] Applies to output and bidirectional pins, except USB_VBUS and the pins listed in table note 4.
[4] Applies to pins DA0–12, DBA0–1, DQ0–15, DQS0–1, DQM0–1, DCLK1–2, $\overline{\text{DCLK1–2}}$, $\overline{\text{DCS0–1}}$, DCLKE, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, and $\overline{\text{DWE}}$.
[5] Applies to all input pins except JTAG inputs.
[6] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[7] Applies to DDR_VREF pin.
[8] Absolute value.
[9] For DDR pins (DQ0-15, DQS0-1), test conditions are V_{DDDDR} = Maximum, V_{IN} = V_{DDDDR} Maximum.
[10] Applies to three-statable pins.
[11] For DDR pins (DQ0-15, DQS0-1), test conditions are V_{DDDDR} = Maximum, V_{IN} = 0 V.
[12] Guaranteed, but not tested.

Asynchronous Memory Read Cycle Timing

Table 27 and Table 28 on Page 45 and Figure 13 and Figure 14 on Page 45 describe asynchronous memory read cycle operations for synchronous and for asynchronous ARDY.

Table 27. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	5.0		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	5.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.3		ns

[1] Output pins include $\overline{AMS3–0}$, $\overline{ABE1–0}$, ADDR19–1, $\overline{AOE}$, and $\overline{ARE}$.

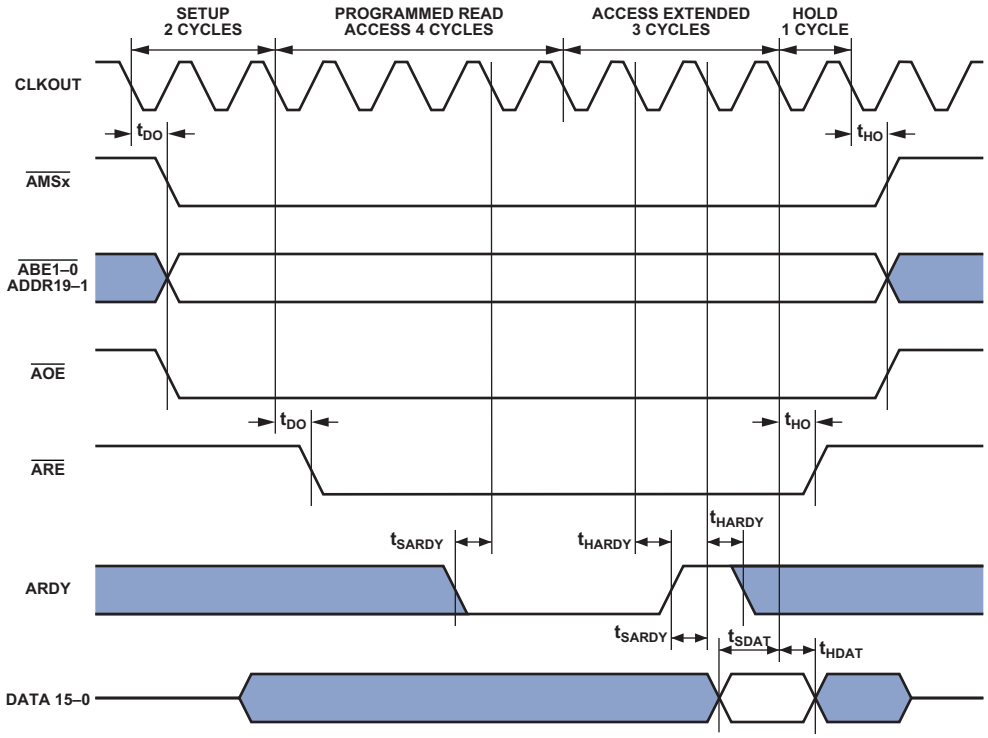


Figure 13. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

DDR SDRAM/Mobile DDR SDRAM Clock and Control Cycle Timing

Table 31 and Figure 17 describe DDR SDRAM/mobile DDR SDRAM clock and control cycle timing.

Table 31. DDR SDRAM/Mobile DDR SDRAM Clock and Control Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Switching Characteristics						
t_{CK}[1]	DCK0-1 Period, Non-Extended Temperature Grade Models	7.50		7.50	8.33	ns
	DCK0-1 Period, Extended Temperature Grade Models	10.00		N/A	N/A	ns
t_{CH}	DCK0-1 High Pulse Width	0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	DCK0-1 Low Pulse Width	0.45	0.55	0.45	0.55	t_{CK}
t_{AS}[2, 3]	Address and Control Output SETUP Time Relative to CK	1.00		1.00		ns
t_{AH}[2, 3]	Address and Control Output HOLD Time Relative to CK	1.00		1.00		ns
t_{OPW}[2, 3]	Address and Control Output Pulse Width	2.20		2.30		ns

[1] The t_{CK} specification does not account for the effects of jitter.
[2] Address pins include DA0-12 and DBA0-1.
[3] Control pins include $\overline{\text{DCS0-1}}$, DCLKE, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, and $\overline{\text{DWE}}$.

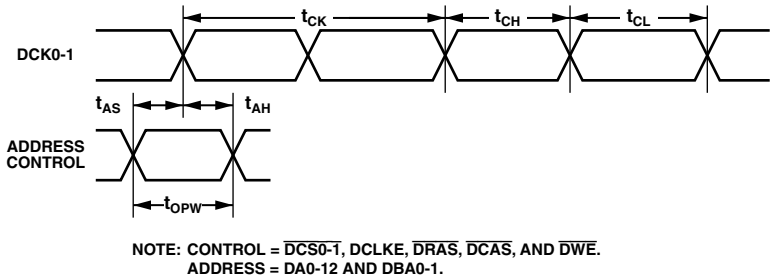


Figure 17. DDR SDRAM /Mobile DDR SDRAM Clock and Control Cycle Timing

DDR SDRAM/Mobile DDR SDRAM Timing

Table 32 and Figure 18/Figure 19 describe DDR SDRAM/mobile DDR SDRAM read cycle timing.

Table 32. DDR SDRAM/Mobile DDR SDRAM Read Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Timing Requirements						
t_{AC}	Access Window of DQ0-15 to DCK0-1	–1.25	+1.25	0.0	6.00	ns
t_{DQSCK}	Access Window of DQS0-1 to DCK0-1	–1.25	+1.25	0.0	6.00	ns
t_{DQSQ}	DQS0-1 to DQ0-15 Skew, DQS0-1 to Last DQ0-15 Valid		0.90		0.85	ns
t_{QH}	DQ0-15 to DQS0-1 Hold, DQS0-1 to First DQ0-15 to Go Invalid	$t_{CK}/2 - 1.25$[1] $t_{CK}/2 - 1.75$[2]		$t_{CK}/2 - 1.25$		ns
t_{RPRE}	DQS0-1 Read Preamble	0.9	1.1	0.9	1.1	t_{CK}
t_{RPST}	DQS0-1 Read Postamble	0.4	0.6	0.4	0.6	t_{CK}

[1] For 7.50 ns $\leq t_{CK} < 10$ ns.
[2] For $t_{CK} \geq 10$ ns.

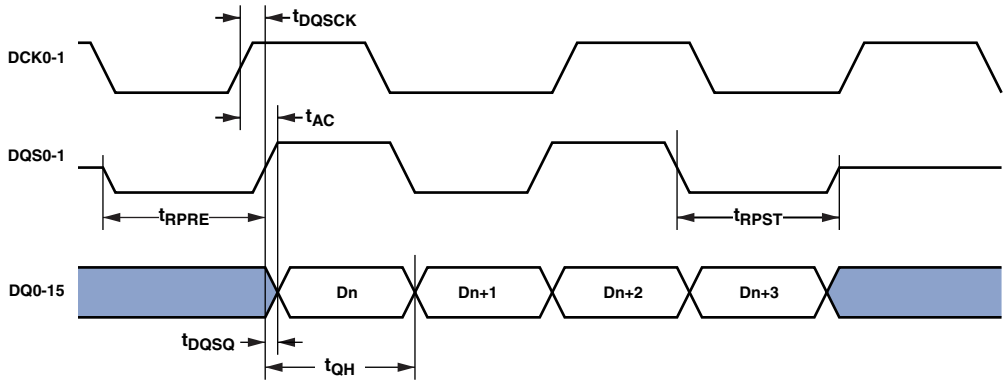


Figure 18. DDR SDRAM Controller Read Cycle Timing

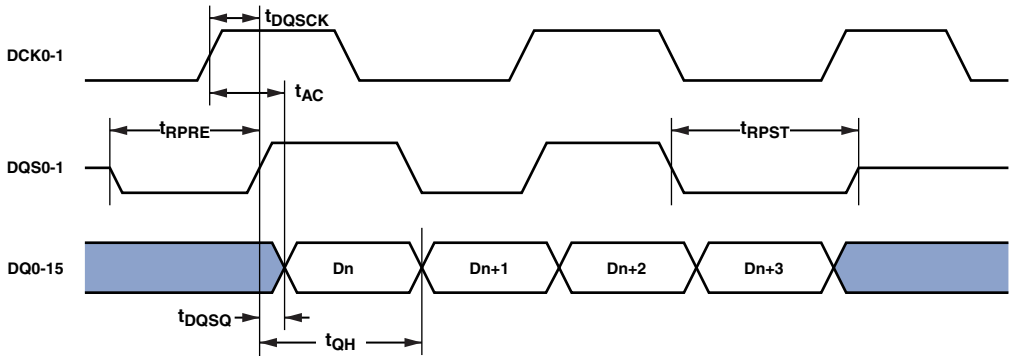


Figure 19. Mobile DDR SDRAM Controller Read Cycle Timing

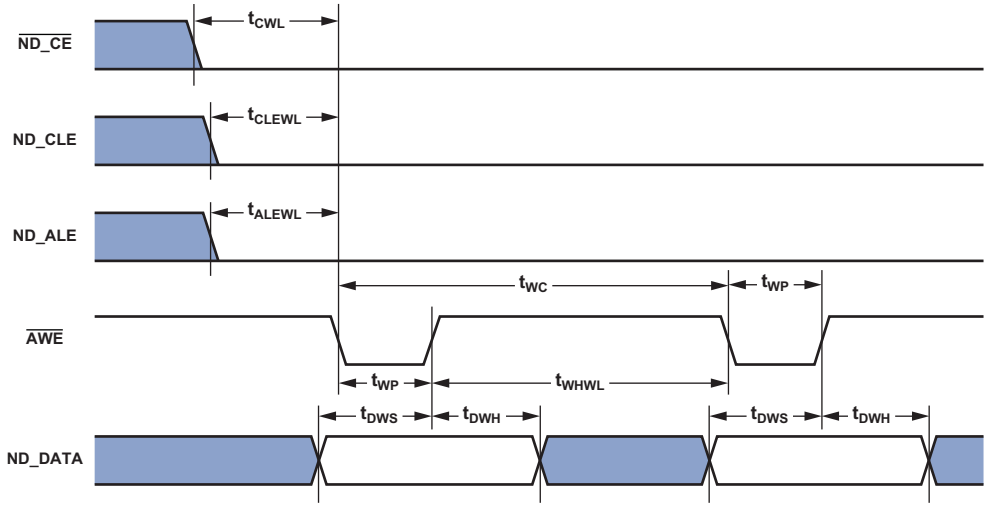


Figure 25. NAND Flash Controller Interface Timing—Data Write Operation

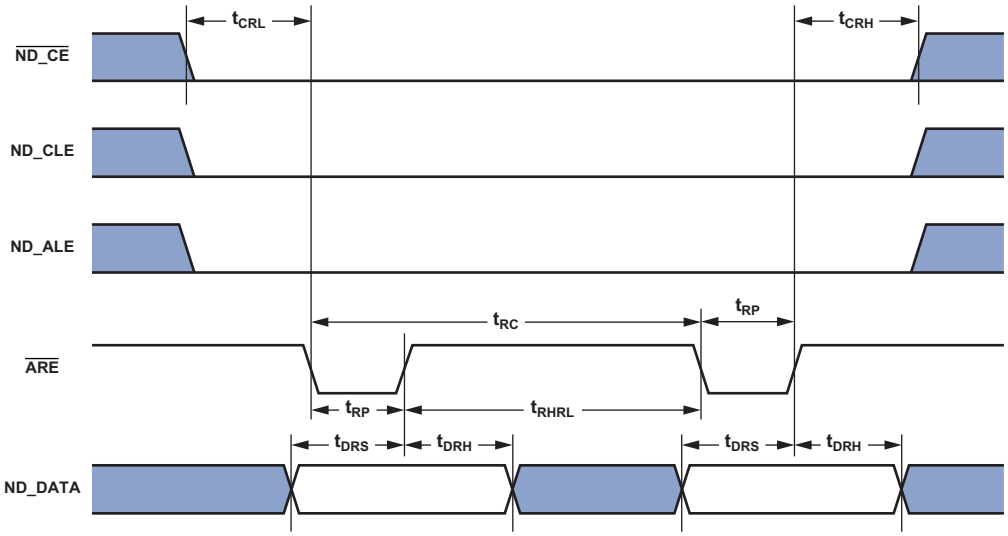


Figure 26. NAND Flash Controller Interface Timing—Data Read Operation

Enhanced Parallel Peripheral Interface Timing

Table 39 and Figure 32 on Page 60, Figure 30 on Page 59, Figure 33 on Page 60, and Figure 31 on Page 59 describe enhanced parallel peripheral interface timing operations.

Table 39. Enhanced Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPIx_CLK Width	6.0		ns
t_{PCLK}	PPIx_CLK Period	13.3		ns
Timing Requirements—GP Input and Frame Capture Modes				
t_{SFSPE}	External Frame Sync Setup Before PPIx_CLK	0.9		ns
t_{HFSPE}	External Frame Sync Hold After PPIx_CLK	1.9		ns
t_{SDRPE}	Receive Data Setup Before PPIx_CLK	1.6		ns
t_{HDRPE}	Receive Data Hold After PPIx_CLK	1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPIx_CLK		10.5	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPIx_CLK	2.4		ns
t_{DDTPE}	Transmit Data Delay After PPIx_CLK		9.9	ns
t_{HDTPE}	Transmit Data Hold After PPIx_CLK	2.4		ns

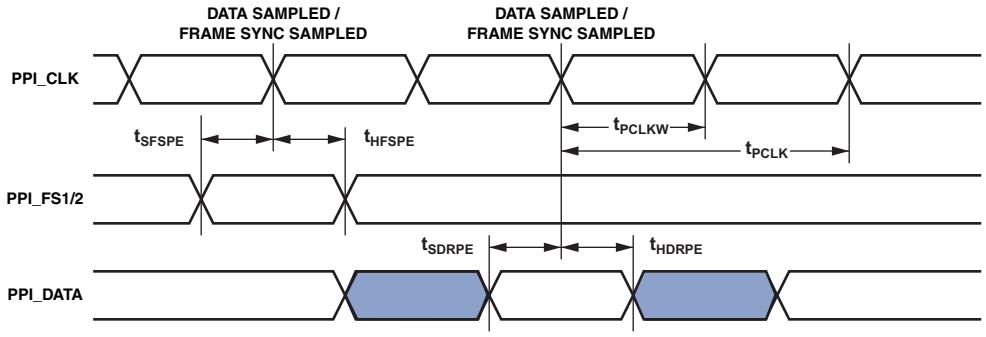


Figure 30. EPPI GP Rx Mode with External Frame Sync Timing

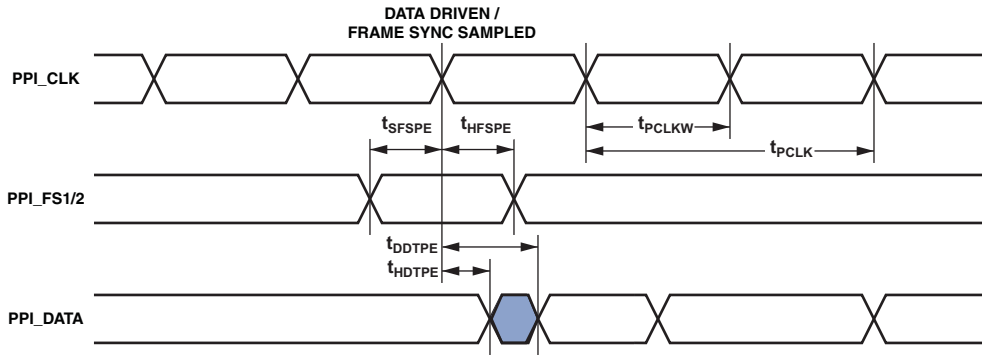


Figure 31. EPPI GP Tx Mode with External Frame Sync Timing

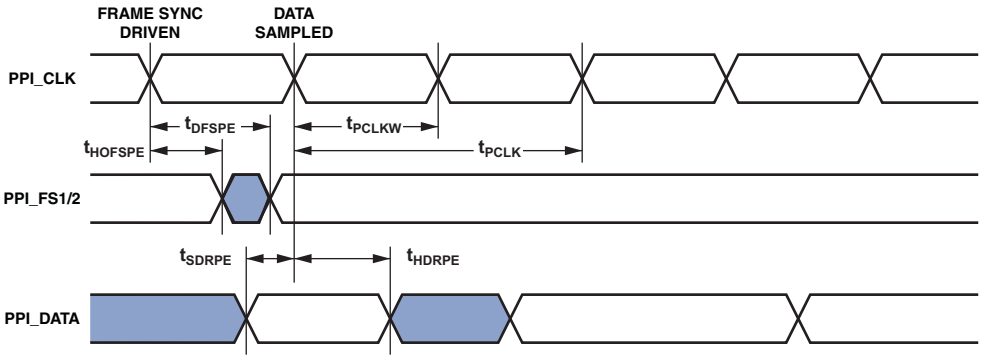


Figure 32. EPPI GP Rx Mode with Internal Frame Sync Timing

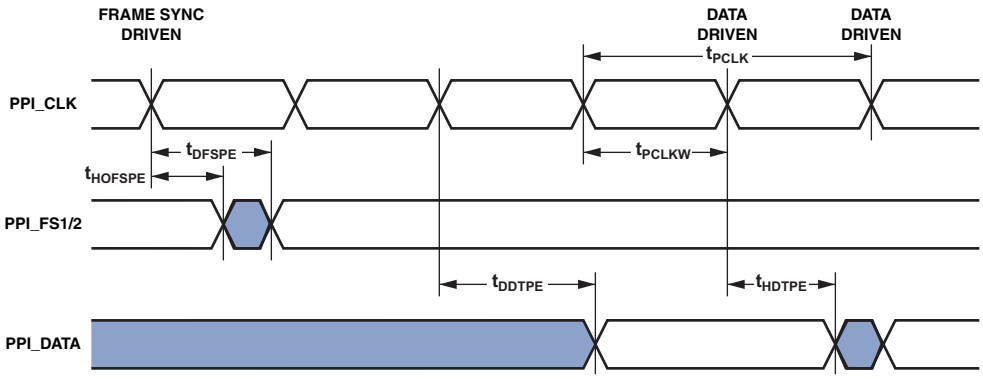


Figure 33. EPPI GP Tx Mode with Internal Frame Sync Timing

Up/Down Counter/Rotary Encoder Timing

Table 49 and Figure 43 describe up/down counter/rotary encoder timing.

Table 49. Up/Down Counter/Rotary Encoder Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{WCOUNT}	CUD/CDG/CZM Input Pulse Width	t_{SCLK} + 1		ns
t_{CIS}	CUD/CDG/CZM Input Setup Time Before CLKOUT High[1]	7.2		ns
t_{CIH}	CUD/CDG/CZM Input Hold Time After CLKOUT High[1]	0.0		ns

[1] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize counter inputs.

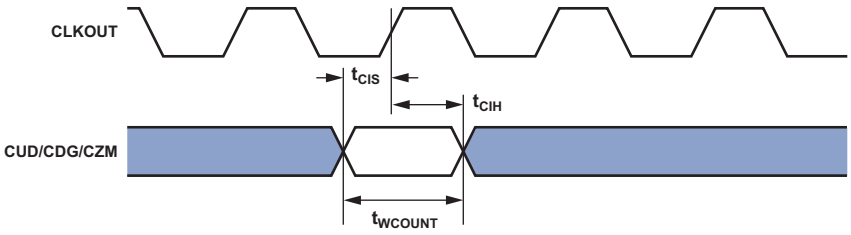


Figure 43. Up/Down Counter/Rotary Encoder Timing

SD/SDIO Controller Timing

Table 50 and Figure 44 describe SD/SDIO controller timing.
Table 51 and Figure 45 describe SD/SDIO controller (high-speed mode) timing.

Table 50. SD/SDIO Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	SD_Dx and SD_CMD Input Setup Time	7.2		ns
t_{IH}	SD_Dx and SD_CMD Input Hold Time	2		ns
Switching Characteristics				
f_{PP}	SD_CLK Frequency During Data Transfer Mode[1]	0	20	MHz
f_{PP}	SD_CLK Frequency During Identification Mode[1]	100[2]	400	kHz
t_{WL}	SD_CLK Low Time	15		ns
t_{WH}	SD_CLK High Time	15		ns
t_{TLH}	SD_CLK Rise Time		10	ns
t_{THL}	SD_CLK Fall Time		10	ns
t_{ODLY}	SD_Dx and SD_CMD Output Delay Time During Data Transfer Mode	–1	+14	ns
	SD_Dx and SD_CMD Output Delay Time During Identification Mode	–1	+50	ns

[1] $t_{PP}=1/f_{PP}$.
[2] Spec can be 0 kHz, meaning to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

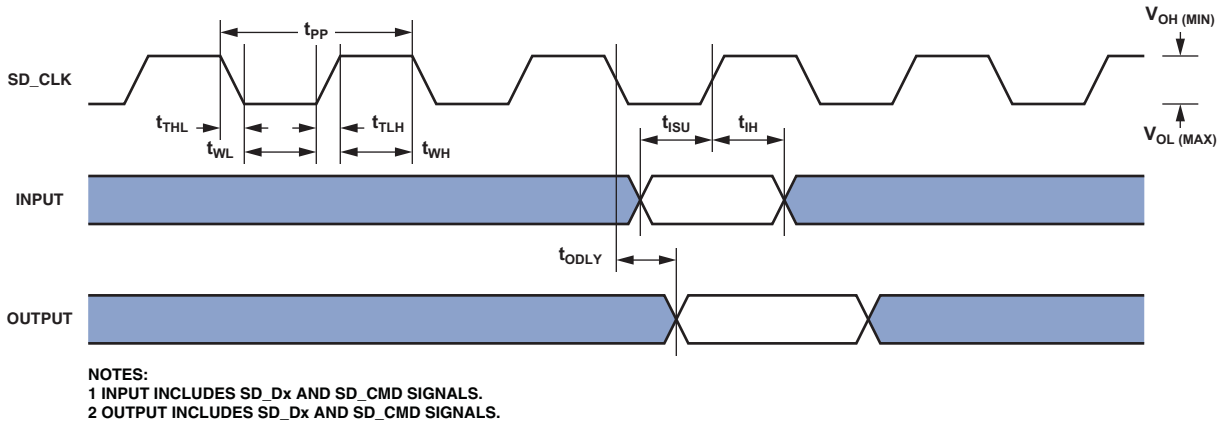


Figure 44. SD/SDIO Controller Timing

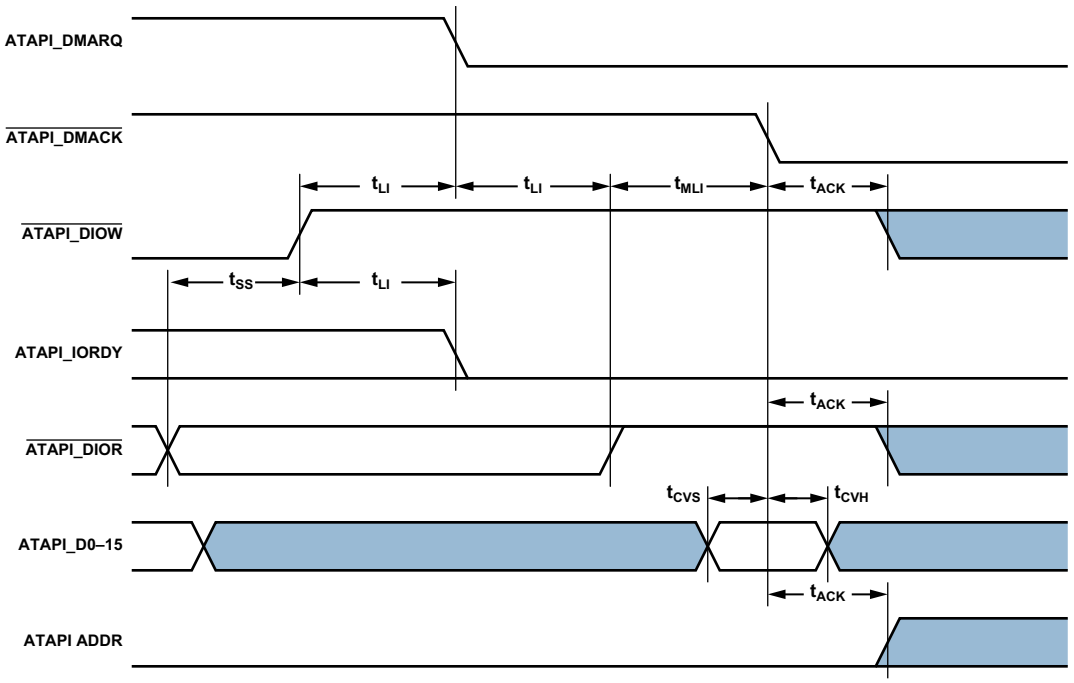


Figure 59. Host terminating an Ultra DMA Data-Out Burst

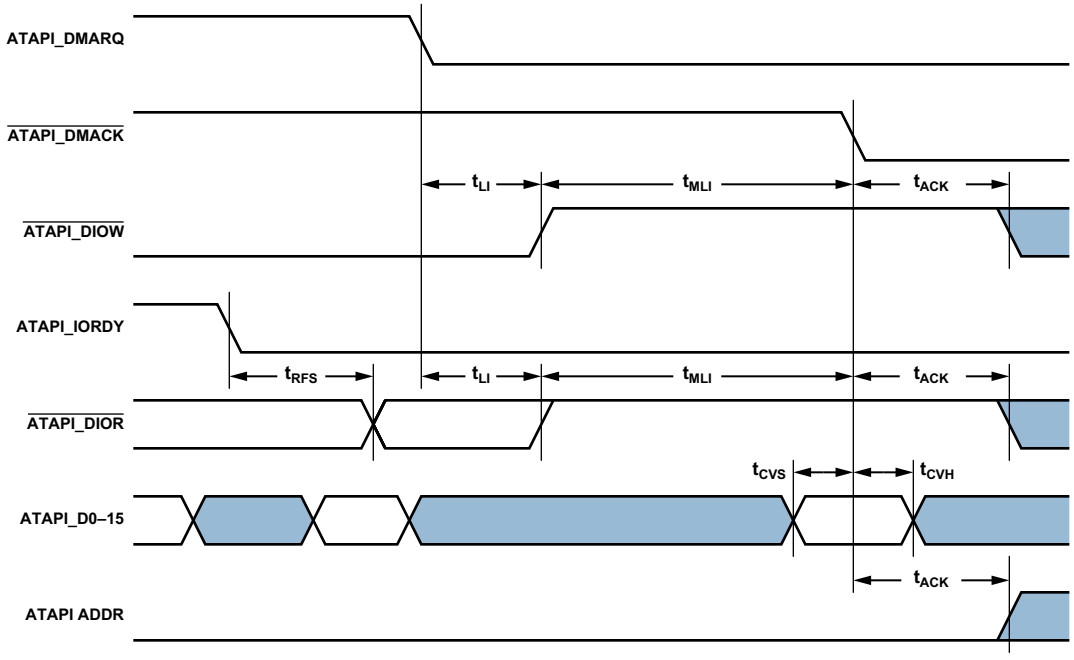


Figure 60. Device Terminating an Ultra DMA Data-Out Burst

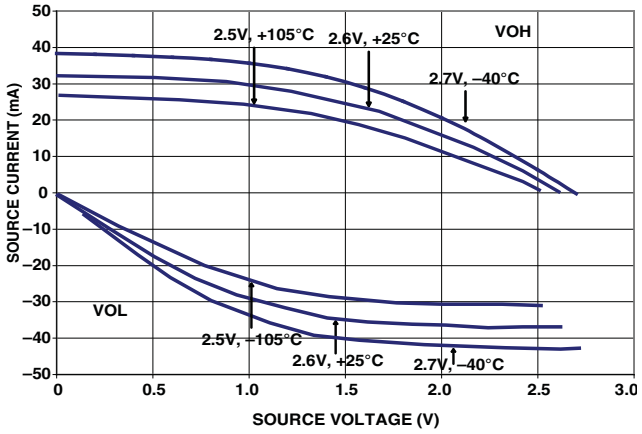


Figure 68. Drive Current D (DDR SDRAM)

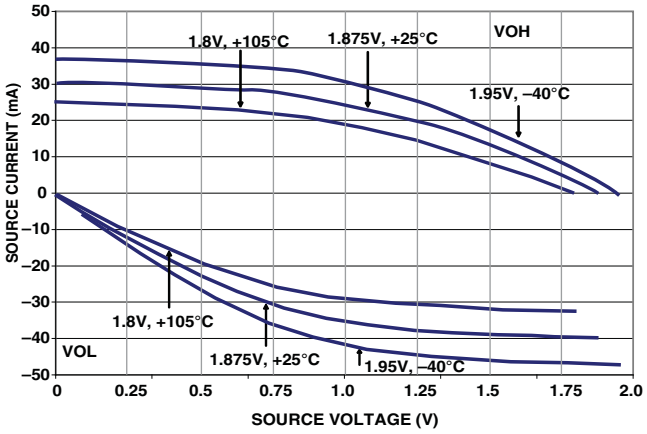


Figure 69. Drive Current D (Mobile DDR SDRAM)

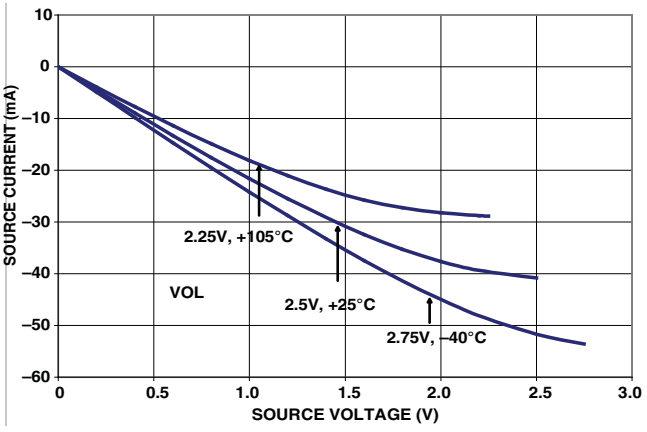


Figure 70. Drive Current E (Low V_{DDEXT})

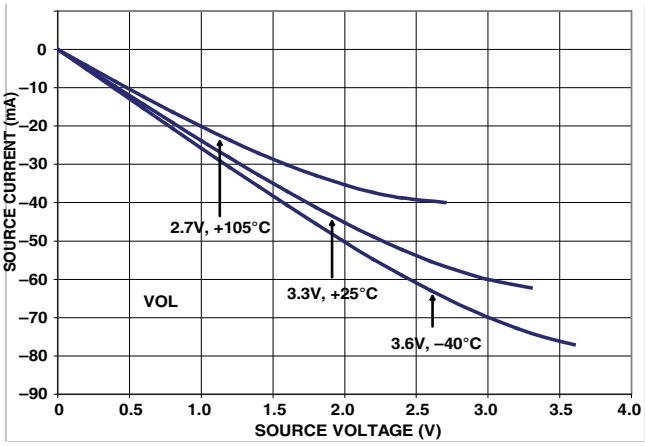


Figure 71. Drive Current E (High V_{DDEXT})

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 72 shows the measurement point for AC measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DDEXT}/2$ or $V_{DDDDR}/2$, depending on the pin under test.

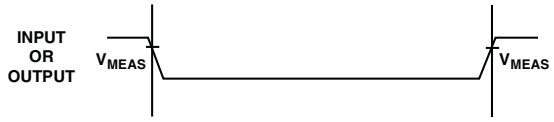


Figure 72. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown in the output enable/disable diagram (Figure 73). The time, $t_{ENA\_MEASURED}$, is the interval from the point when the reference signal switches to the point when the output voltage reaches either 1.75 V (output high) or 1.25 V (output low). Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the 1.25 V or 1.75 V trip voltage. Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown in Figure 73. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V.

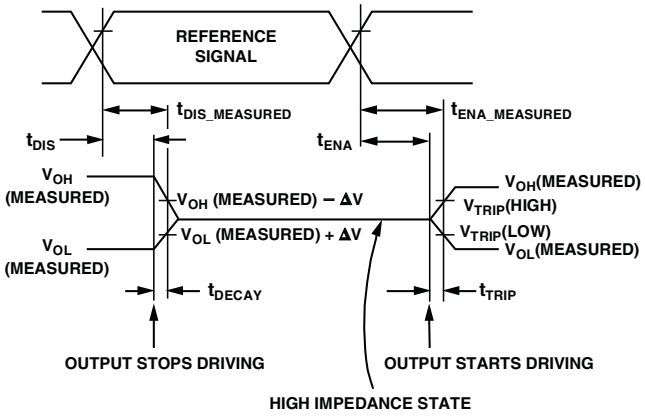


Figure 73. Output Enable/Disable

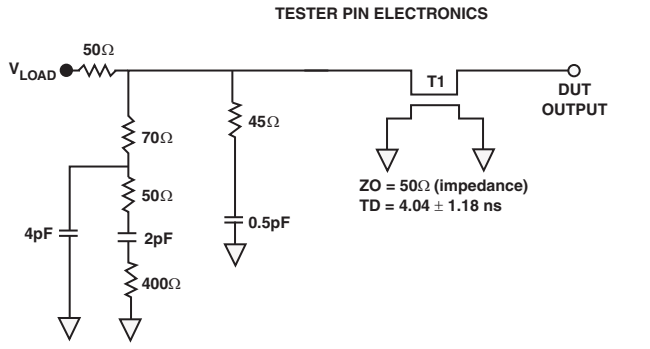
Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF54x Blackfin processors' output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (for example, t_{DDAT} for an asynchronous memory write cycle).

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 74).

V_{LOAD} is equal to $V_{DDEXT}/2$ or $V_{DDDDR}/2$, depending on the pin under test.



NOTES:
THE WORST-CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 74. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Table 65. 400-Ball CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
MLF_P	E4	PC5	G1	PE15	W17	PH7	H4
MXI	C2	PC6	J5	PF0	K3	PH8	D5
MXO	C1	PC7	H3	PF1	J1	PH9	C4
$\overline{\text{NMI}}$	C11	PC8	Y14	PF2	K2	PH10	C7
PA0	U12	PC9	V13	PF3	K1	PH11	C5
PA1	V12	PC10	U13	PF4	L2	PH12	D7
PA2	W12	PC11	W14	PF5	L1	PH13	C6
PA3	Y12	PC12	Y15	PF6	L4	PI0	A3
PA4	W11	PC13	W15	PF7	K4	PI1	B4
PA5	V11	PD0	P3	PF8	L3	PI2	A4
PA6	Y11	PD1	P4	PF9	M1	PI3	B5
PA7	U11	PD2	R1	PF10	M2	PI4	A5
PA8	U10	PD3	R2	PF11	M3	PI5	B6
PA9	Y10	PD4	T1	PF12	M4	PI6	A6
PA10	Y9	PD5	R3	PF13	N4	PI7	B7
PA11	V10	PD6	T2	PF14	N1	PI8	A7
PA12	Y8	PD7	R4	PF15	N2	PI9	C8
PA13	W10	PD8	U1	PG0	J4	PI10	B8
PA14	Y7	PD9	U2	PG1	K5	PI11	A8
PA15	W9	PD10	T3	PG2	L5	PI12	A9
PB0	W5	PD11	V1	PG3	N3	PI13	C9
PB1	Y2	PD12	T4	PG4	P1	PI14	D8
PB2	T6	PD13	V2	PG5	V15	PI15	B9
PB3	U6	PD14	U4	PG6	Y17	PJ0	R20
PB4	Y4	PD15	U3	PG7	W16	PJ1	N18
PB5	Y3	PE0	V19	PG8	V16	PJ2	M16
PB6	W6	PE1	T17	PG9	Y19	PJ3	T20
PB7	V7	PE2	U18	PG10	Y18	PJ4	N17
PB8	W8	PE3	V14	PG11	U15	PJ5	U20
PB9	V8	PE4	Y16	PG12	P16	PJ6	P18
PB10	U7	PE5	W20	PG13	R18	PJ7	N16
PB11	W7	PE6	W19	PG14	Y13	PJ8	R19
PB12	Y6	PE7	R17	PG15	W13	PJ9	P17
PB13	V9	PE8	V20	PH0	W18	PJ10	T19
PB14	Y5	PE9	U19	PH1	U14	PJ11	M17
PC0	H2	PE10	T18	PH2	V17	PJ12	P20
PC1	J3	PE11	P2	PH3	V18	PJ13	N19
PC2	J2	PE12	M5	PH4	U17	$\overline{\text{RESET}}$	C12
PC3	H1	PE13	P5	PH5	C3	RTXI	A14
PC4	G2	PE14	U16	PH6	D6	RTXO	B14

Table 65. 400-Ball CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
TCK	V3	V_{DDDDR}	J14	V_{DDEXT}	N5	V_{DDINT}	G13
TDI	V5	V_{DDDDR}	J15	V_{DDEXT}	N15	V_{DDINT}	J6
TDO	V4	V_{DDDDR}	K14	V_{DDEXT}	P15	V_{DDINT}	J13
TMS	U5	V_{DDDDR}	K15	V_{DDEXT}	R6	V_{DDINT}	L6
$\overline{TRST}$	T5	V_{DDEXT}	E5	V_{DDEXT}	R7	V_{DDINT}	L15
USB_DM	E2	V_{DDEXT}	E9	V_{DDEXT}	R8	V_{DDINT}	P6
USB_DP	E1	V_{DDEXT}	E10	V_{DDEXT}	R15	V_{DDINT}	P7
USB_ID	G3	V_{DDEXT}	E11	V_{DDEXT}	T7	V_{DDINT}	P14
USB_RSET	D3	V_{DDEXT}	E12	V_{DDEXT}	T8	V_{DDINT}	R10
USB_VBUS	D2	V_{DDEXT}	F7	V_{DDEXT}	T9	V_{DDINT}	R11
USB_VREF	B1	V_{DDEXT}	F8	V_{DDEXT}	T10	V_{DDINT}	R12
USB_XI	F1	V_{DDEXT}	F13	V_{DDEXT}	T11	V_{DDINT}	U9
USB_XO	F2	V_{DDEXT}	G5	V_{DDEXT}	T12	V_{DDMP}	E8
V_{DDDDR}	F10	V_{DDEXT}	G6	V_{DDEXT}	T13	V_{DDRTC}	E13
V_{DDDDR}	F11	V_{DDEXT}	G7	V_{DDEXT}	T14	V_{DDUSB}	F5
V_{DDDDR}	F12	V_{DDEXT}	G14	V_{DDEXT}	T15	V_{DDUSB}	G4
V_{DDDDR}	G15	V_{DDEXT}	H5	V_{DDEXT}	T16	V_{DDVR}	F15
V_{DDDDR}	H13	V_{DDEXT}	H6	V_{DDINT}	F9	VR_{OUT0}	A18
V_{DDDDR}	H14	V_{DDEXT}	K6	V_{DDINT}	G8	VR_{OUT1}	A19
V_{DDDDR}	H15	V_{DDEXT}	M15	V_{DDINT}	G12	XTAL	A12

Table 66 lists the CSP_BGA package by ball number for the ADSP-BF549. Table 65 on Page 94 lists the CSP_BGA package by signal.

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	C1	MXO	E1	USB_DP	G1	PC5
A2	A2	C2	MXI	E2	USB_DM	G2	PC4
A3	PI0	C3	PH5	E3	GND	G3	USB_ID
A4	PI2	C4	PH9	E4	MLF_P	G4	V_{DDUSB}
A5	PI4	C5	PH11	E5	V_{DDEXT}	G5	V_{DDEXT}
A6	PI6	C6	PH13	E6	MFS	G6	V_{DDEXT}
A7	PI8	C7	PH10	E7	GND_{MP}	G7	V_{DDEXT}
A8	PI11	C8	PI9	E8	V_{DDMP}	G8	V_{DDINT}
A9	PI12	C9	PI13	E9	V_{DDEXT}	G9	GND
A10	$\overline{AMS0}$	C10	$\overline{AOE}$	E10	V_{DDEXT}	G10	GND
A11	CLKIN	C11	$\overline{NMI}$	E11	V_{DDEXT}	G11	GND
A12	XTAL	C12	$\overline{RESET}$	E12	V_{DDEXT}	G12	V_{DDINT}
A13	GND	C13	D1	E13	V_{DDRTC}	G13	V_{DDINT}
A14	RTXI	C14	D8	E14	D14	G14	V_{DDEXT}
A15	D4	C15	D9	E15	D13	G15	V_{DDDDR}
A16	D6	C16	$\overline{ABE1}$	E16	$\overline{DCLK0}$	G16	DA4
A17	D10	C17	$\overline{ABE0}$	E17	$\overline{DRAS}$	G17	DA1
A18	$VROUT_0$	C18	DCLK1	E18	$\overline{DWE}$	G18	DA3
A19	$VROUT_1$	C19	$\overline{DCS0}$	E19	DA9	G19	DA0
A20	GND	C20	DA7	E20	DA2	G20	DQM0
B1	USB_VREF	D1	GND	F1	USB_XI	H1	PC3
B2	A1	D2	USB_VBUS	F2	USB_XO	H2	PC0
B3	A3	D3	USB_RSET	F3	GND	H3	PC7
B4	PI1	D4	GND	F4	MLF_M	H4	PH7
B5	PI3	D5	PH8	F5	V_{DDUSB}	H5	V_{DDEXT}
B6	PI5	D6	PH6	F6	GND	H6	V_{DDEXT}
B7	PI7	D7	PH12	F7	V_{DDEXT}	H7	GND
B8	PI10	D8	PI14	F8	V_{DDEXT}	H8	GND
B9	PI15	D9	$\overline{AMS1}$	F9	V_{DDINT}	H9	GND
B10	$\overline{AMS2}$	D10	$\overline{AMS3}$	F10	V_{DDDDR}	H10	GND
B11	GND	D11	CLKBUF	F11	V_{DDDDR}	H11	GND
B12	$\overline{ARE}$	D12	$\overline{AWE}$	F12	V_{DDDDR}	H12	GND
B13	D2	D13	D0	F13	V_{DDEXT}	H13	V_{DDDDR}
B14	RTXO	D14	D11	F14	GND	H14	V_{DDDDR}
B15	D3	D15	D12	F15	V_{DDVR}	H15	V_{DDDDR}
B16	D5	D16	DCLK0	F16	$\overline{DCAS}$	H16	DBA1
B17	D7	D17	D15	F17	DA11	H17	DBA0
B18	DCLKE	D18	$\overline{DCLK1}$	F18	DA8	H18	DQS1
B19	$\overline{DCS1}$	D19	DA12	F19	DA5	H19	DQM1
B20	DA10	D20	DA6	F20	DQS0	H20	DQ11