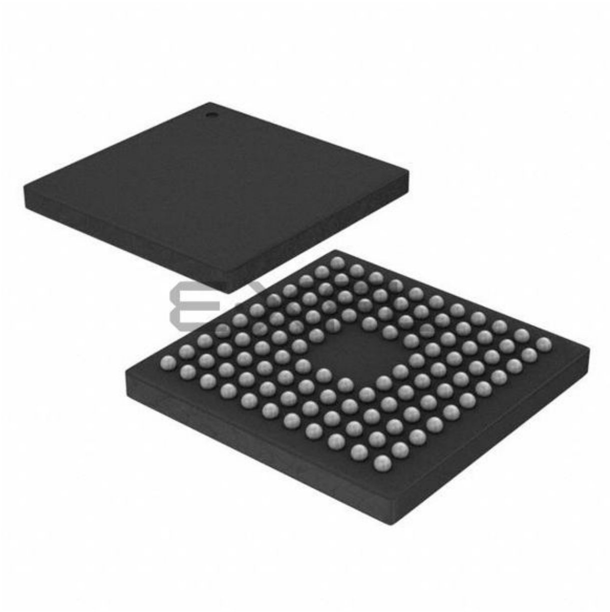

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

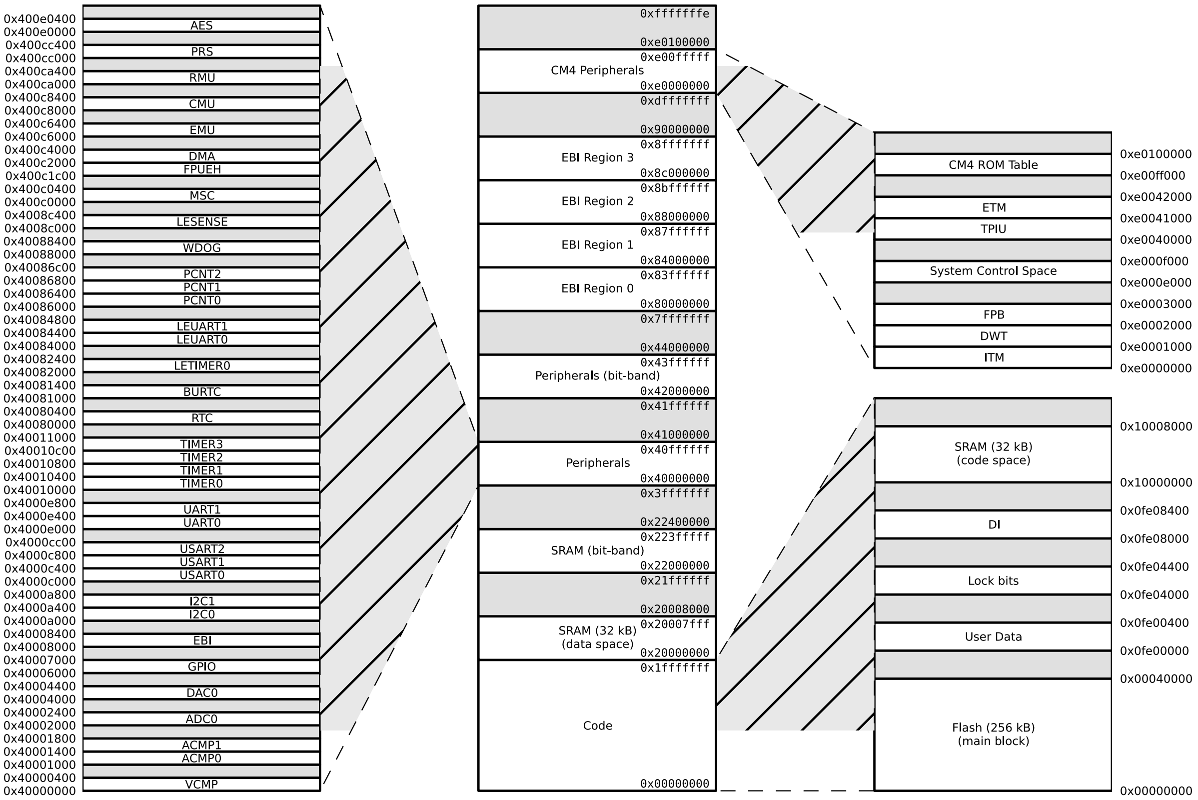
Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	90
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg290f256-bga112t

Module	Configuration	Pin Connections
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX. US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in Table 4.3 (p. 67)

2.3 Memory Map

The *EFM32WG290* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG290 Memory Map with largest RAM and Flash sizes



Symbol	Parameter	Condition	Min	Typ	Max	Unit
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85°C		3.0[1]	4.0[1]	µA
I_{EM3}	EM3 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.65	1.3	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		2.65	4.0	µA
I_{EM4}	EM4 current	V_{DD}= 3.0 V, T_{AMB}=25°C		0.02	0.055	µA
		V_{DD}= 3.0 V, T_{AMB}=85°C		0.44	0.9	µA

[1] Using backup RTC.

3.4.1 EM1 Current Consumption

Figure 3.1. EM1 Current consumption with all peripheral clocks disabled and HFXO running at 48MHz

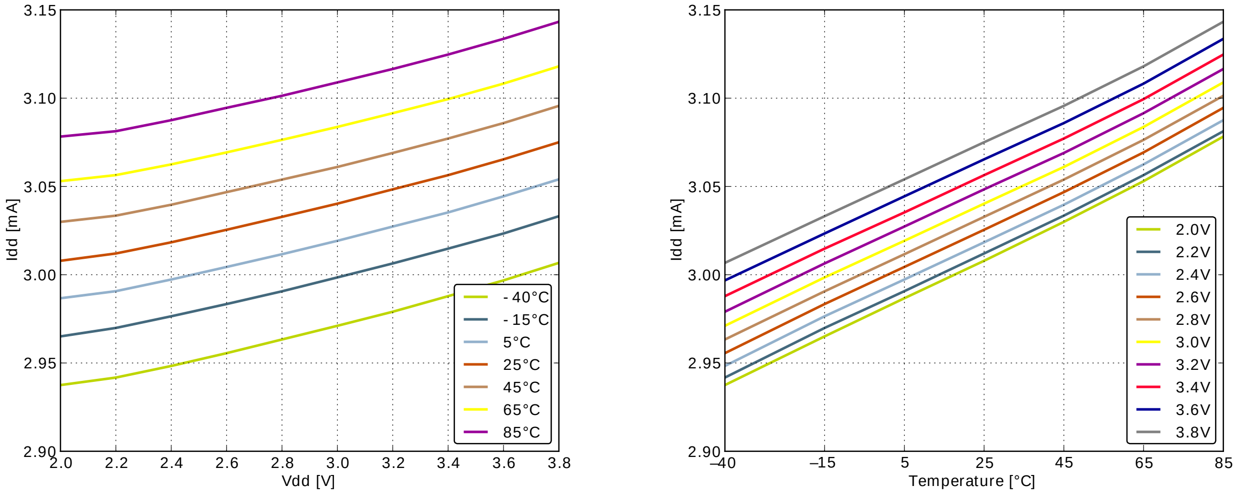


Figure 3.2. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 28MHz

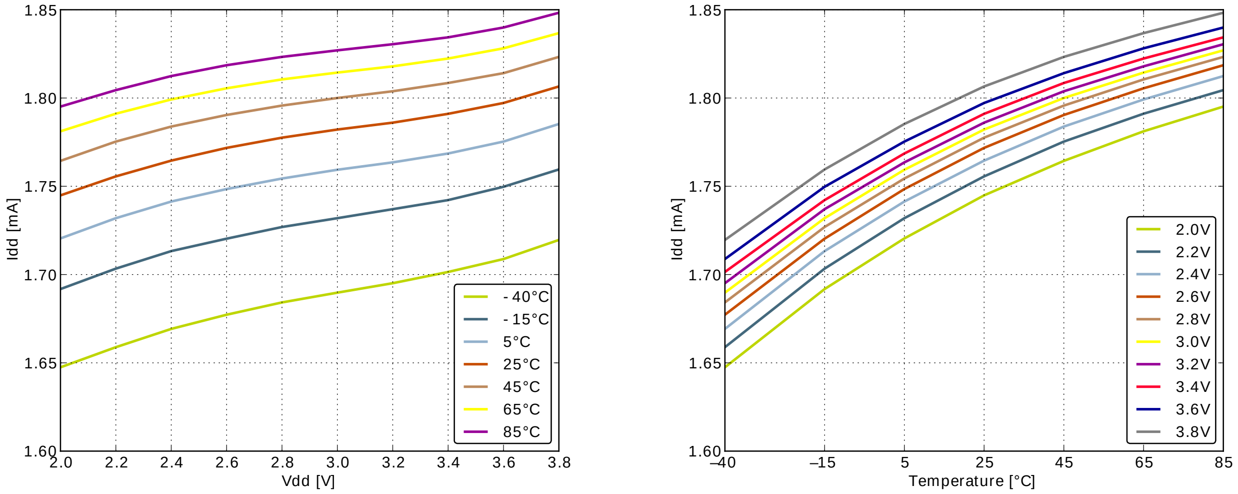


Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

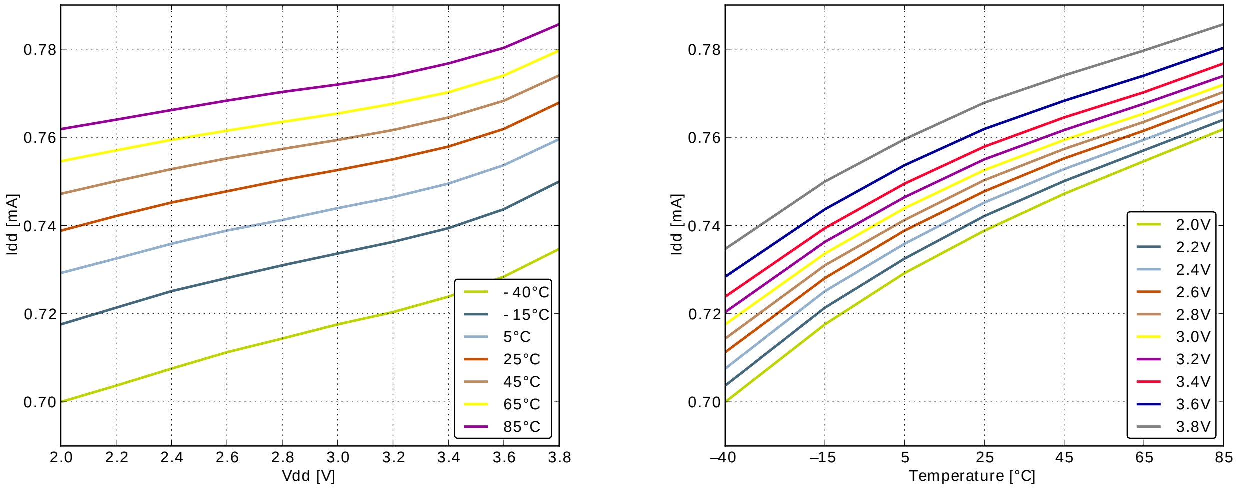
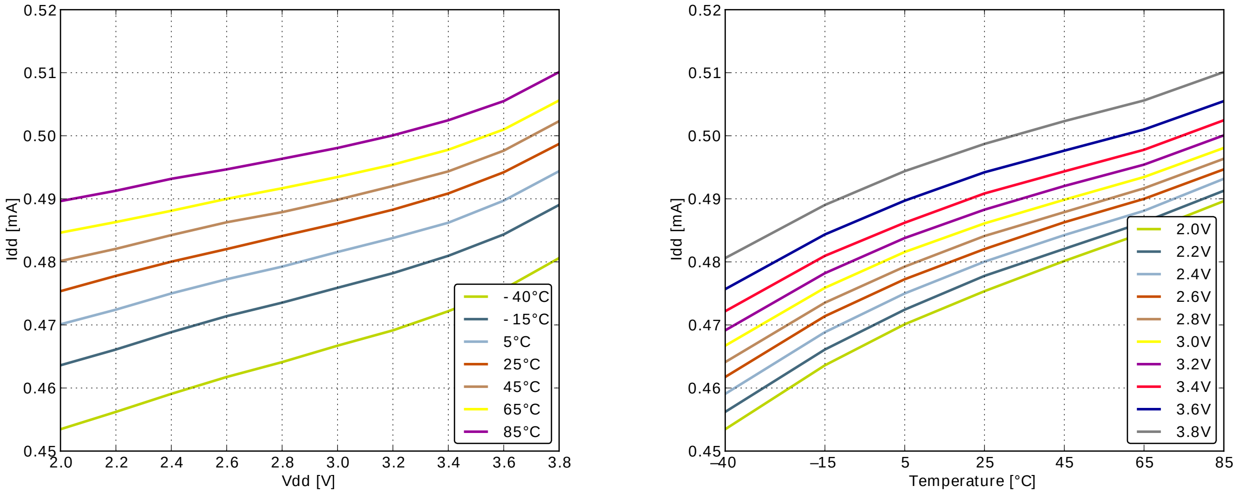


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz



3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.74		1.96	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		µF

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC_{FLASH}	Flash erase cycles before failure		20000			cycles
RET_{FLASH}	Flash data retention	T_{AMB}<150°C	10000			h
		T_{AMB}<85°C	10			years
		T_{AMB}<70°C	20			years
t_{W_PROG}	Word (32-bit) programming time		20			µs
t_{PERASE}	Page erase time		20	20.4	20.8	ms
t_{DERASE}	Device erase time		40	40.8	41.6	ms
I_{ERASE}	Erase current				7[1]	mA
I_{WRITE}	Write current				7[1]	mA
V_{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

[1] Measured at 25°C

Figure 3.19. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

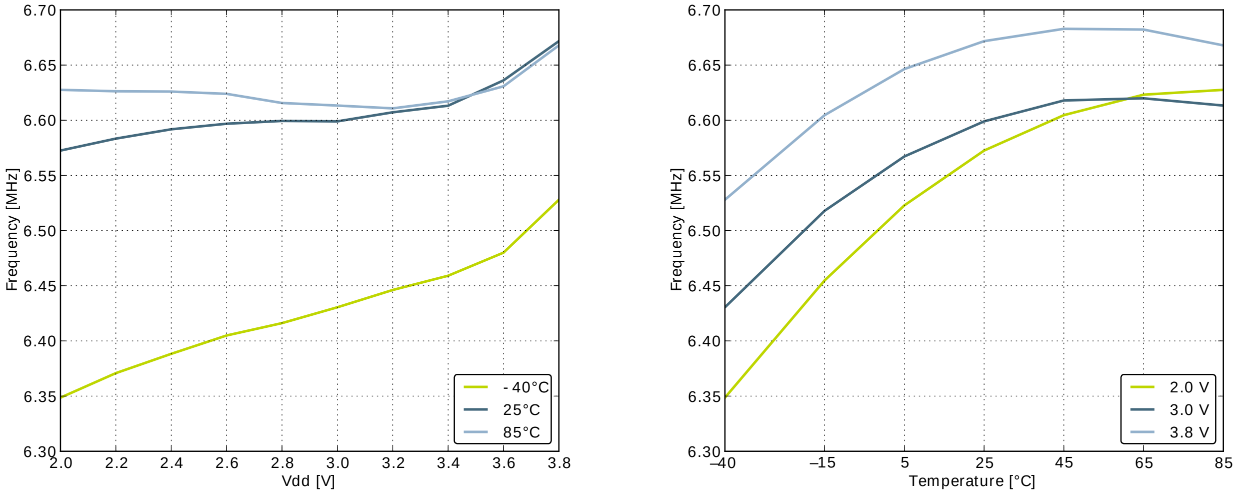


Figure 3.20. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

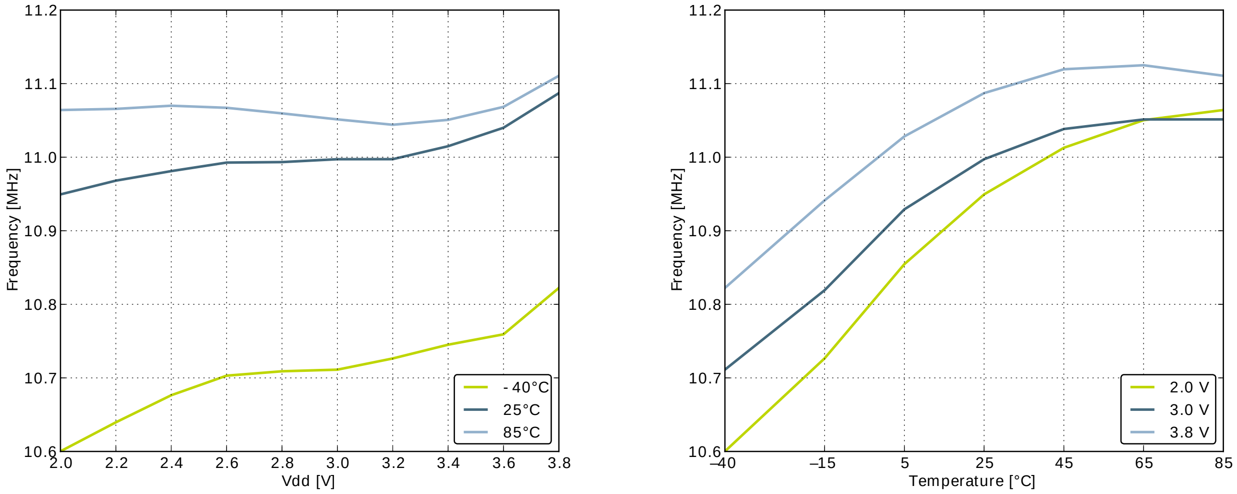


Figure 3.21. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

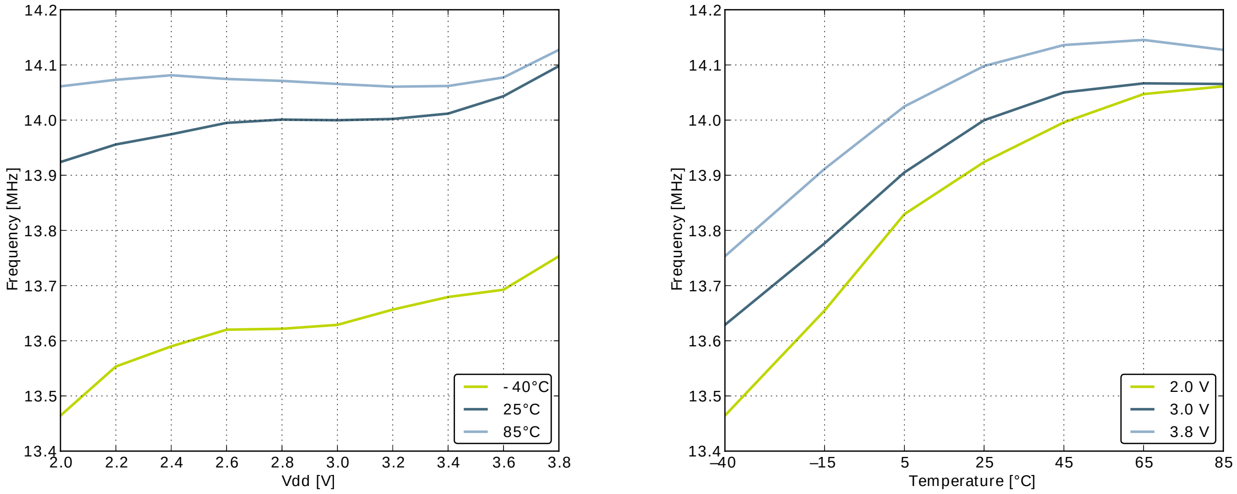


Figure 3.22. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

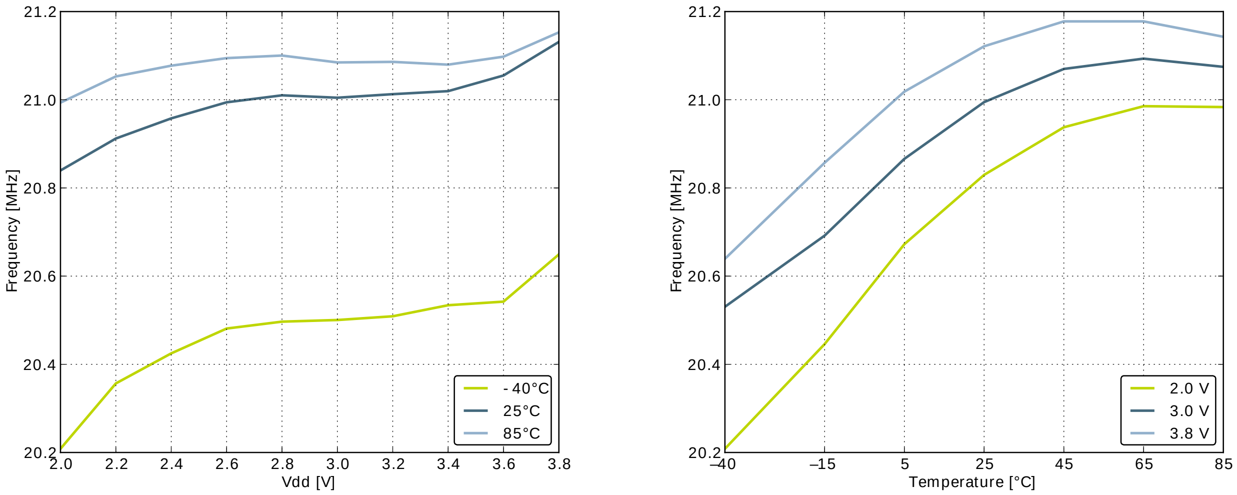
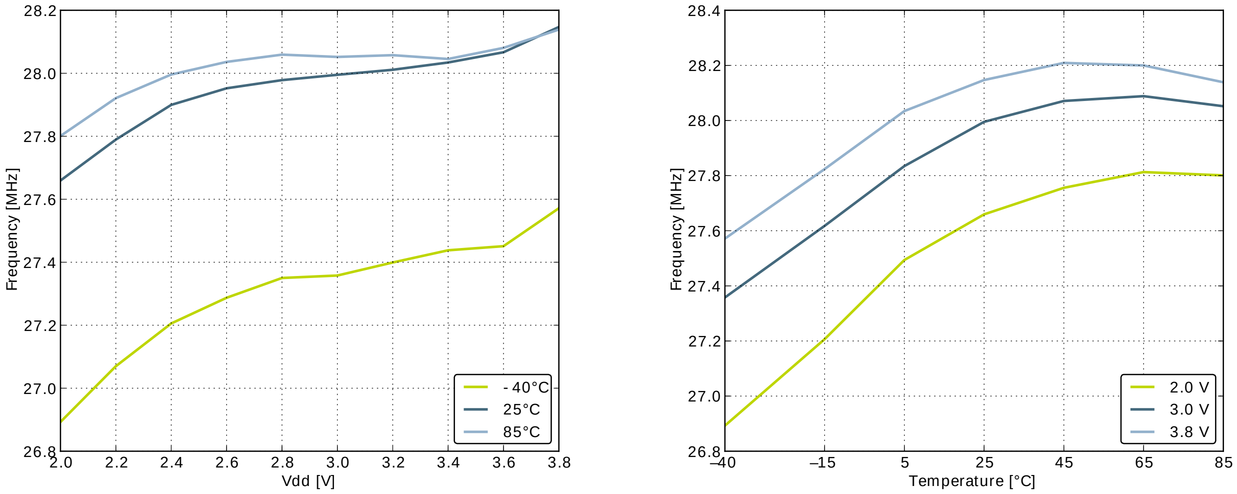


Figure 3.23. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature



Symbol	Parameter	Condition	Min	Typ	Max	Unit
	erence voltage on channel 6					
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		351		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00		67		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01		63		µA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10		64		µA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		µA
C_{ADCIN}	Input capacitance			2		pF
R_{ADCIN}	Input ON resistance		1			MOhm
$R_{ADCFILT}$	Input RC filter resistance			10		kOhm
$C_{ADCFILT}$	Input RC filter/decoupling capacitance			250		fF
f_{ADCCLK}	ADC Clock Frequency				13	MHz
$t_{ADCCONV}$	Conversion time	6 bit	7			ADCCLK Cycles
		8 bit	11			ADCCLK Cycles
		12 bit	13			ADCCLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1		256	ADCCLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2			µs
$t_{ADCSTART}$	Startup time of reference generator			5		µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	25	µA
G_{OL}	Open Loop Gain	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
GBW_{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
PM_{OPAMP}	Phase Margin	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C_L=75 pF		64		°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C_L=75 pF		58		°
R_{INPUT}	Input Resistance			100		Mohm
R_{LOAD}	Load Resistance		200			Ohm
I_{LOAD_DC}	DC Load Current				11	mA
V_{INPUT}	Input Voltage	OPAxHCMDIS=0	V_{SS}		V_{DD}	V
		OPAxHCMDIS=1	V_{SS}		V_{DD}-1.2	V
V_{OUTPUT}	Output Voltage		V_{SS}		V_{DD}	V
V_{OFFSET}	Input Offset Voltage	Unity Gain, V_{SS}<V_{in}<V_{DD}, OPAxHCMDIS=0	-13	0	11	mV
		Unity Gain, V_{SS}<V_{in}<$_{DD}$-1.2, OPAxHCMDIS=1		1		mV
V_{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR_{OPAMP}	Slew Rate	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/µs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/µs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/µs
N_{OPAMP}	Voltage Noise	V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0		101		μV_{RMS}
		V_{out}=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1		141		μV_{RMS}

Figure 3.34. OPAMP Negative Power Supply Rejection Ratio

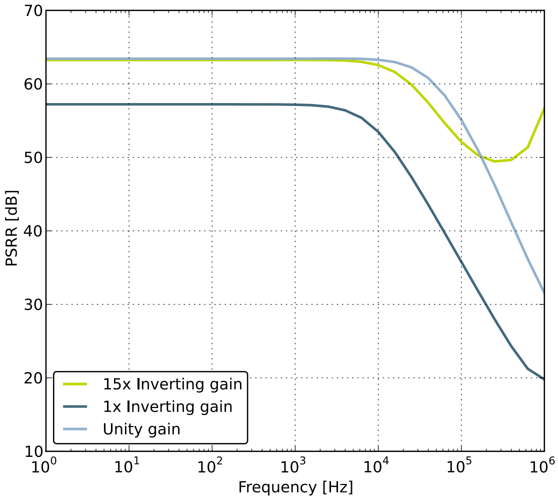


Figure 3.35. OPAMP Voltage Noise Spectral Density (Unity Gain) V_{out}=1V

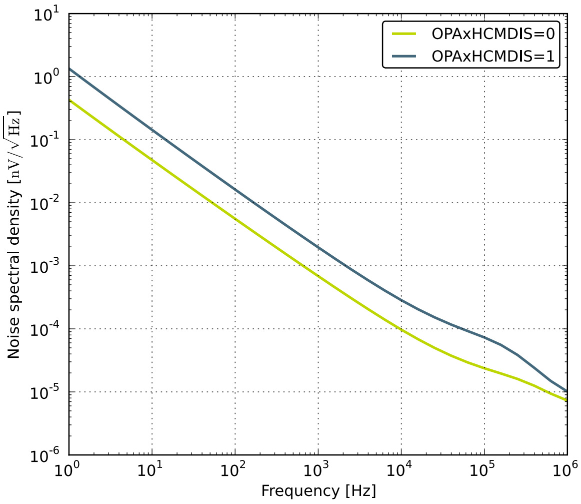
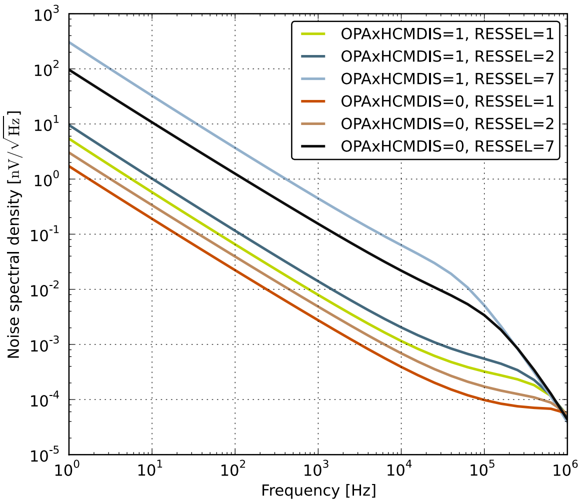


Figure 3.36. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



3.13 Analog Comparator (ACMP)

Table 3.18. ACMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	µA
		BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	µA
		BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	µA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		µA
		Internal voltage reference		5		µA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	µs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 47) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \tag{3.1}$$

Table 3.20. EBI Write Enable Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_WEn} [1] [2] [3] [4]	Output hold time, from trailing EBI_WEn/ EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	-6.00 + (WRHOLD * $t_{HFCORECLK}$)			ns
t_{OSU_WEn} [1] [2] [3] [4] [5]	Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn/ EBI_NANDWEn edge	-14.00 + (WRSETUP * $t_{HFCORECLK}$)			ns
t_{WIDTH_WEn} [1] [2] [3] [4] [5]	EBI_WEn/EBI_NANDWEn pulse width	-7.00 + ((WRSTRB +1) * $t_{HFCORECLK}$)			ns

[1] Applies for all addressing modes (figure only shows D16 addressing mode)

[2] Applies for both EBI_WEn and EBI_NANWEn (figure only shows EBI_WEn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by 1/2 * $t_{HFCLKNODIV}$.

Figure 3.39. EBI Address Latch Enable Related Output Timing

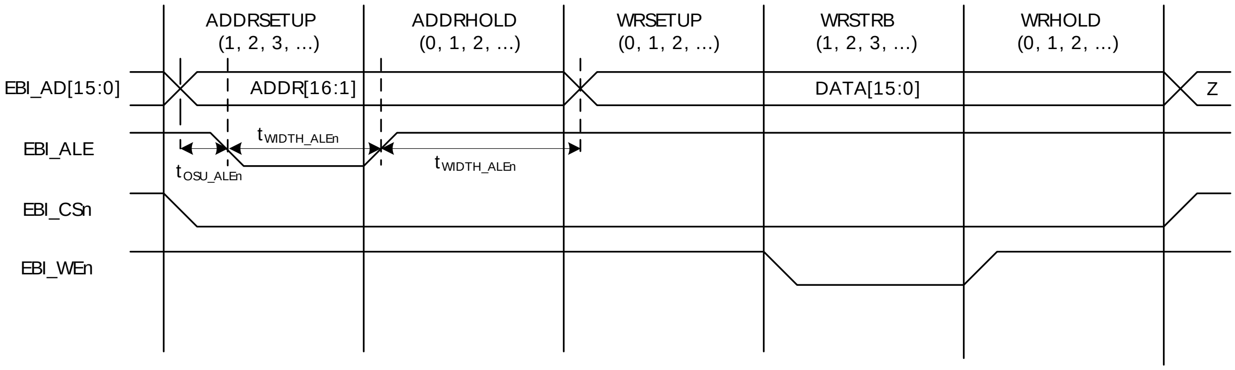


Table 3.21. EBI Address Latch Enable Related Output Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{OH_ALEn} [1] [2] [3] [4]	Output hold time, from trailing EBI_ALE edge to EBI_AD invalid	-6.00 + (ADDRHOLD[5] * $t_{HFCORECLK}$)			ns
t_{OSU_ALEn} [1] [2] [4]	Output setup time, from EBI_AD valid to leading EBI_ALE edge	-13.00 + (0 * $t_{HFCORECLK}$)			ns
t_{WIDTH_ALEn} [1] [2] [3] [4]	EBI_ALEn pulse width	-7.00 + (ADDRSETUP+1) * $t_{HFCORECLK}$)			ns

[1] Applies to addressing modes D8A24ALE and D16A16ALE (figure only shows D16A16ALE)

[2] Applies for all polarities (figure only shows active low signals)

[3] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALE can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of tOH_ALEn by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.

[4] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of $_{VDD}$)

[5] Figure only shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

Table 3.27. I2C Fast-mode Plus (Fm+)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		1000[1]	kHz
t_{LOW}	SCL clock low time	0.5			µs
t_{HIGH}	SCL clock high time	0.26			µs
$t_{SU,DAT}$	SDA set-up time	50			ns
$t_{HD,DAT}$	SDA hold time	8			ns
$t_{SU,STA}$	Repeated START condition set-up time	0.26			µs
$t_{HD,STA}$	(Repeated) START condition hold time	0.26			µs
$t_{SU,STO}$	STOP condition set-up time	0.26			µs
t_{BUF}	Bus free time between a STOP and a START condition	0.5			µs

[1] For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32WG Reference Manual.

3.17 USART SPI

Figure 3.43. SPI Master Timing

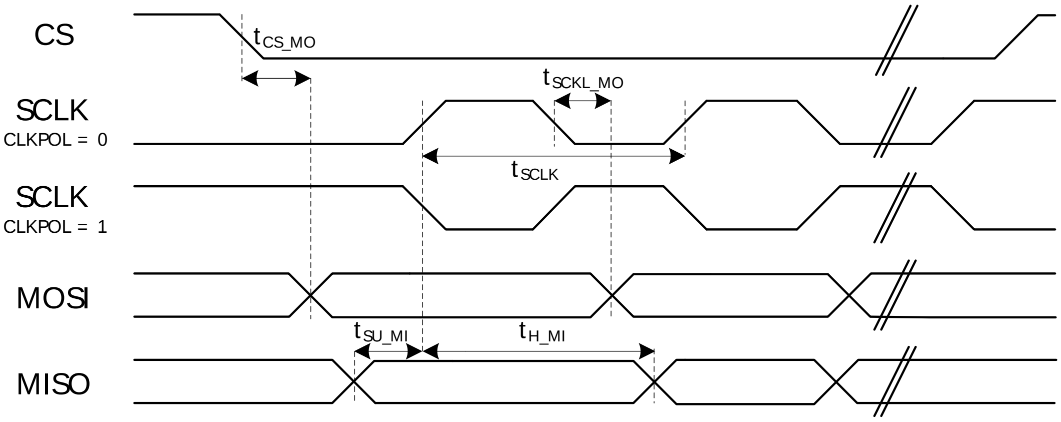


Table 3.28. SPI Master Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK} [1,2]	SCLK period		$2 * t_{HFPERCLK}$			ns
t_{CS_MO} [1,2]	CS to MOSI		-2.00		2.00	ns
t_{SCLK_MO} [1,2]	SCLK to MOSI		-1.00		3.00	ns
t_{SU_MI} [1,2]	MISO setup time	IOVDD = 3.0 V	36.00			ns
t_{H_MI} [1,2]	MISO hold time		-6.00			ns

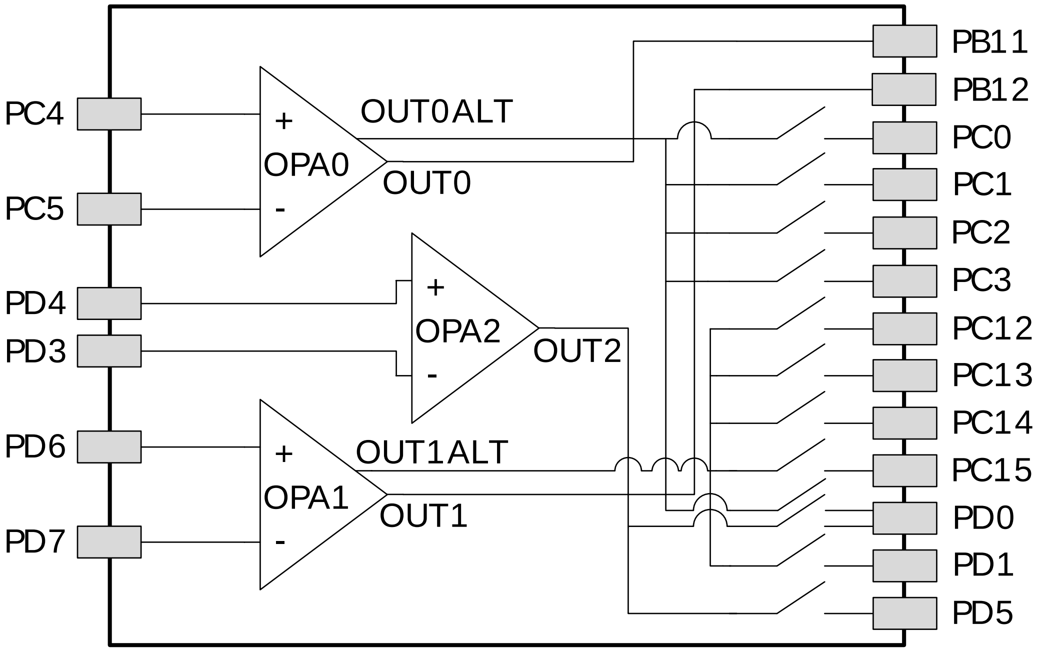
[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
						ETM_TD1 #3
D2	PA2		EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
D3	PB15					ETM_TD2 #1
D4	VSS	Ground				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9		EBI_CS0 #0/1/2			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
D9	PE7		EBI_A14 #0/1/2		US0_TX #1	
D10	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
D11	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
E1	PA6		EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
E2	PA5		EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
E3	PA4		EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
E4	PB0		EBI_A16 #0/1/2	TIM1_CC0 #2		
E8	PF0			TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
E9	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
E10	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
E11	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
F1	PB1		EBI_A17 #0/1/2	TIM1_CC1 #2		
F2	PB2		EBI_A18 #0/1/2	TIM1_CC2 #2		
F3	PB3		EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
F4	PB4		EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
G1	PB5		EBI_A21 #0/1/2		US2_CLK #1	
G2	PB6		EBI_A22 #0/1/2		US2_CS #1	
G3	VSS	Ground				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground				
G10	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2

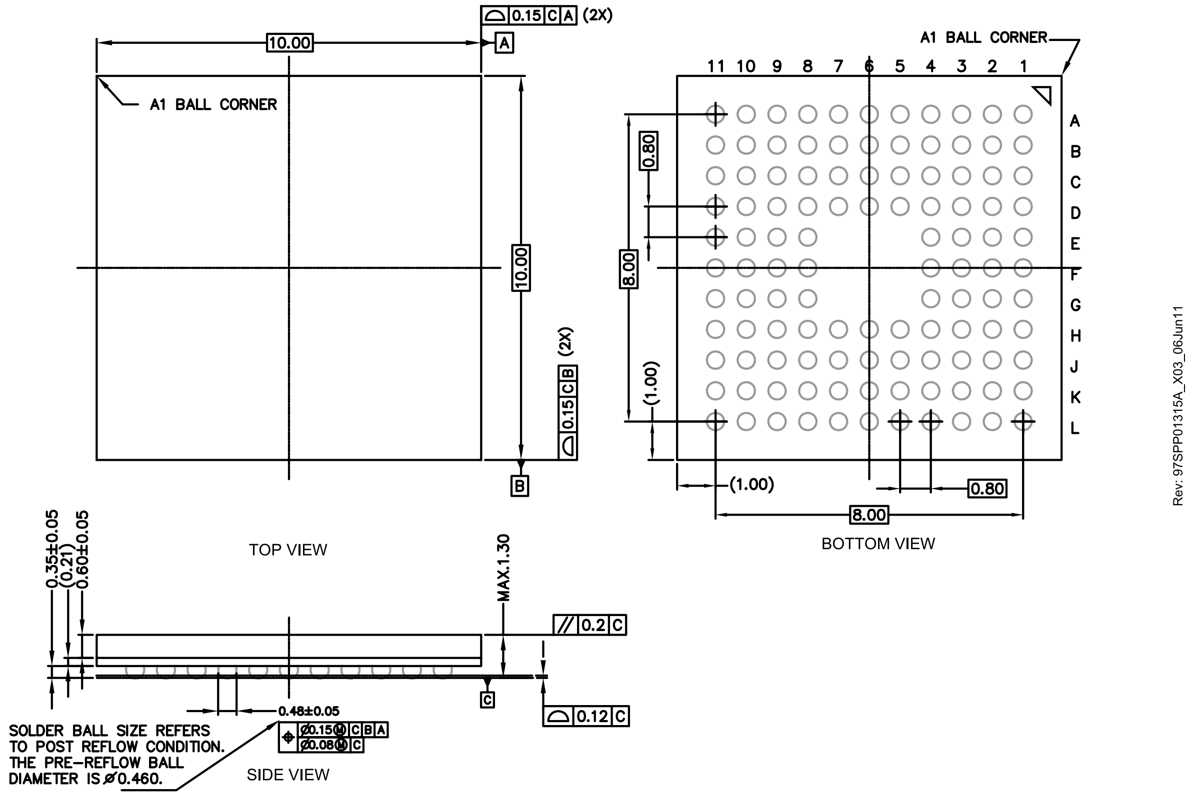
Alternate	LOCATION							
Functionality	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**Description**
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.

Figure 4.2. Opamp Pinout



4.5 BGA112 Package

Figure 4.3. BGA112



Note:

1. The dimensions in parenthesis are reference.
2. Datum 'C' and seating plane are defined by the crown of the solder balls.
3. All dimensions are in millimeters.

The BGA112 Package uses SAC105 solderballs.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:
http://www.silabs.com/support/quality/pages/default.aspx

Updated the EM0 and EM1 current consumption numbers. Updated the the EM1 plots and removed the EM0 plots.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.4 Revision 1.20

June 28th, 2013

Updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.5 Revision 1.10

May 6th, 2013

Updated current consumption table and figures in Electrical characteristics section.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

Other minor corrections.

7.7 Revision 0.95

May 3rd, 2012

Updated EM2/EM3 current consumption at 85°C.

7.8 Revision 0.90

February 27th, 2012

Initial preliminary release.

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