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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Floating Point
Interface	EBI/EMI, DAI, I ² C, SPI, SPORT, UART/USART
Clock Rate	266MHz
Non-Volatile Memory	External
On-Chip RAM	2Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21488wbswz1b02

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- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

Non-SDRAM external memory address space is shown in [Table 5](#).

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	6M	0x0020 0000–0x007F FFFF
Bank 1	8M	0x0400 0000–0x047F FFFF
Bank 2	8M	0x0800 0000–0x087F FFFF
Bank 3	8M	0x0C00 0000–0x0C7F FFFF

External Port

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 176-lead LQFP, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and banks 1, 2, and 3 occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices at speeds up to f_{SDCLK} . Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$ – $\overline{MS3}$), and can be configured to contain between 4M bytes and 256M bytes of memory. SDRAM external memory address space is shown in [Table 6](#). NOTE: this feature is not available on the ADSP-21486 model.

Table 6. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on the SDRAM and AMI interfaces.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This removes the need to explicitly access the complimentary registers when the data is in external SDRAM memory.

VISA and ISA Access to External Memory

The SDRAM controller on the ADSP-2148x processors supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. [Table 7](#) shows the address ranges for instruction fetch in each mode.

Table 7. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000–0x005F FFFF
VISA (SW)	10M	0x0060 0000–0x00FF FFFF

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

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Details on power consumption and Static and Dynamic current consumption can be found at [Total Power Dissipation on Page 20](#). Also see [Operating Conditions on Page 18](#) for more information.

The following are SVS features.

- SVS is applicable only to 450 MHz models (not applicable to 400 MHz or lower frequency models).
- Each individual SVS device includes a register (SVS_DAT) containing the unique SVS voltage set at the factory, known as SVS_{NOM}.
- The SVS_{NOM} value is the intended set voltage for the V_{DD_INT} voltage regulator.
- No dedicated pins are required for SVS. The TWI serial bus is used to communicate SVS_{NOM} to the voltage regulator.
- Analog Devices recommends a specific voltage regulator design and initialization code sequence that optimizes the power-up sequence.

The Engineer-to-Engineer Note [Static Voltage Scaling for ADSP-2148x SHARC Processors \(EE-357\)](#) contains the details of the regulator design and the initialization requirements.

- Any differences from the Analog Devices recommended programmable regulator design must be reviewed by Analog Devices to ensure that it meets the voltage accuracy and range requirements.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2148x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore[®] Embedded Studio and/or VisualDSP++[®]), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

CrossCore Embedded Studio is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating sys-

tems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite[®] evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders[®], which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the Product Download area of the product web page.

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Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see [Analog Devices JTAG Emulation Technical Reference \(EE-68\)](#). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2148x architecture and functionality. For detailed information on the ADSP-2148x family core architecture and instruction set, refer to the programming reference manual.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (<http://www.analog.com/circuits>) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

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Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{SDRAS}}$	O/T (ipu)	High-Z/ driven high	SDRAM Row Address Strobe. Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (ipu)	High-Z/ driven high	SDRAM Column Address Select. Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (ipu)	High-Z/ driven high	SDRAM Write Enable. Connect to SDRAM's WE or W buffer pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
SDCKE	O/T (ipu)	High-Z/ driven high	SDRAM Clock Enable. Connect to SDRAM's CE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (ipu)	High-Z/ driven high	SDRAM A10 Pin. Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's ADDR10 pin only during SDRAM accesses.
SDDQM	O/T (ipu)	High-Z/ driven high	DQM Data Mask. SDRAM Input mask signal for write accesses and output mask signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The SDRAM output buffers are placed in a High-Z state when DQM is sampled high during a read cycle. SDDQM is driven high from reset de-assertion until SDRAM initialization completes. Afterwards it is driven low irrespective of whether any SDRAM accesses occur or not.
SDCLK	O/T (ipd)	High-Z/ driving	SDRAM Clock Output. Clock driver for this pin differs from all other clock drivers. See Figure 41 on Page 55 . For models in the 100-lead package, the SDRAM interface should be disabled to avoid unnecessary power switching by setting the DSDCTL bit in SDCTL register. For more information, see the hardware reference.
DAI_P20-1	I/O/T (ipu)	High-Z	Digital Applications Interface. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins.
DPI_P14-1	I/O/T (ipu)	High-Z	Digital Peripheral Interface. These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins.
WDT_CLKIN	I		Watchdog Timer Clock Input. This pin should be pulled low when not used.
WDT_CLKO	O		Watchdog Resonator Pad Output.
$\overline{\text{WDRSTO}}$	O (ipu)		Watchdog Timer Reset Out.
THD_P	I		Thermal Diode Anode. When not used, this pin can be left floating.
THD_M	O		Thermal Diode Cathode. When not used, this pin can be left floating.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 k Ω –63 k Ω . The range of an ipd resistor can be between 31 k Ω –85k Ω . The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTTL compliant with the exception of the thermal diode pins.

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TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See [Figure 43 on Page 55](#) for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, the processor core, and the serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1-0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see [Figure 4](#)). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

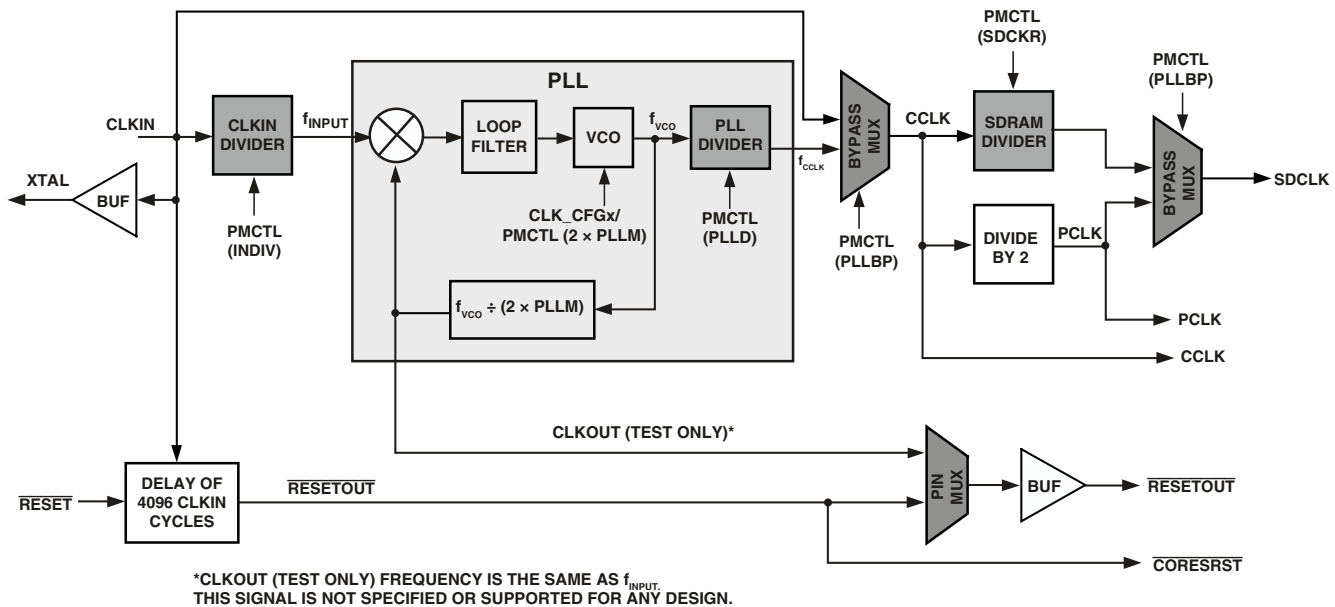


Figure 4. Core Clock and System Clock Relationship to CLKIN

Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in [Table 20](#).

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in [Table 20](#) if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in [Table 20](#) if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$

$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} = is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN \div 2 when the input divider is enabled

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Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 23. Interrupts

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{IPW} $\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{\text{PCLK}} + 2$		ns

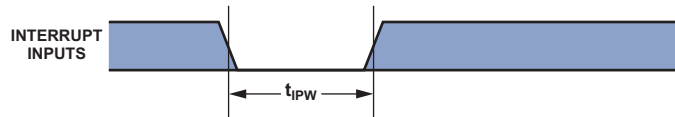


Figure 10. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
t_{WCTIM} TMREXP Pulse Width	$4 \times t_{\text{PCLK}} - 1$		ns



Figure 11. Core Timer

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Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14-1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14-1 pins.

Table 25. Timer PWM_OUT Timing

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
t_{PWMO} Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

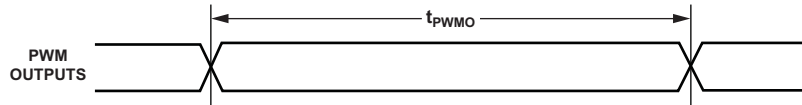


Figure 12. Timer PWM_OUT Timing

Timer WDT_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDT_CAP (pulse-width count and capture) mode. Timer signals are routed to the DPI_P14-1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14-1 pins.

Table 26. Timer Width Capture Timing

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{PWI} Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

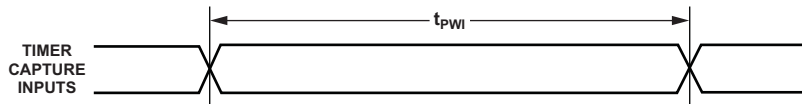


Figure 13. Timer Width Capture Timing

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Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's

inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 29. Precision Clock Generator (Direct Pin Routing)

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{PCGIW} Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG} PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG} PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
<i>Switching Characteristics</i>			
t_{DPCGIO} PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$ PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$ PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}^1 Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the "Precision Clock Generators" chapter in the hardware reference.

¹Normal mode of operation.

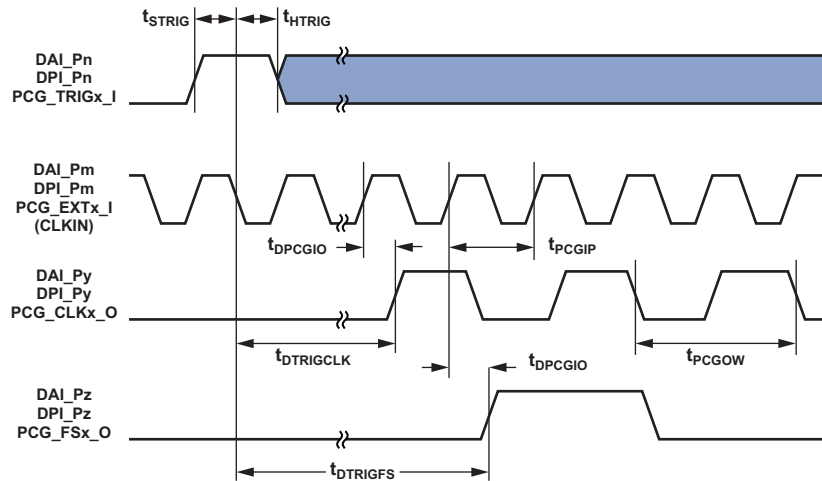


Figure 16. Precision Clock Generator (Direct Pin Routing)

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Flags

The timing specifications provided below apply to the DPI_P14-1, ADDR7-0, ADDR23-8, DATA7-0, and FLAG3-0 pins when configured as FLAGS. See [Table 11 on Page 14](#) for more information on flag use.

Table 30. Flags

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{FIPW}^1 FLAGs IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
<i>Switching Characteristic</i>			
t_{FOPW}^1 FLAGs OUT Pulse Width	$2 \times t_{PCLK} - 3$		ns

¹This is applicable when the Flags are connected to DPI_P14-1, ADDR7-0, ADDR23-8, DATA7-0 and FLAG3-0 pins.

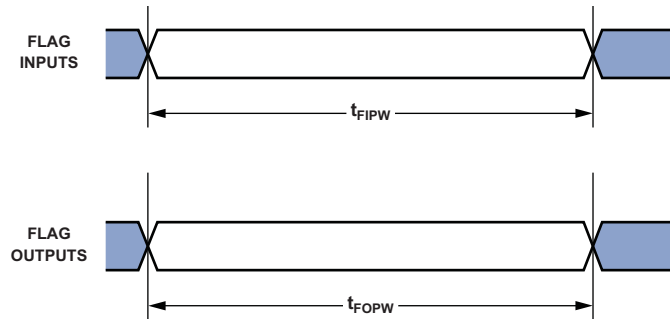


Figure 17. Flags

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Table 37. Serial Ports—Enable and Three-State

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t_{DDTEN}^1 Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}^1 Data Disable from External Transmit SCLK		11.5	ns
t_{DDTIN}^1 Data Enable from Internal Transmit SCLK	-1.5		ns

¹Referenced to drive edge.

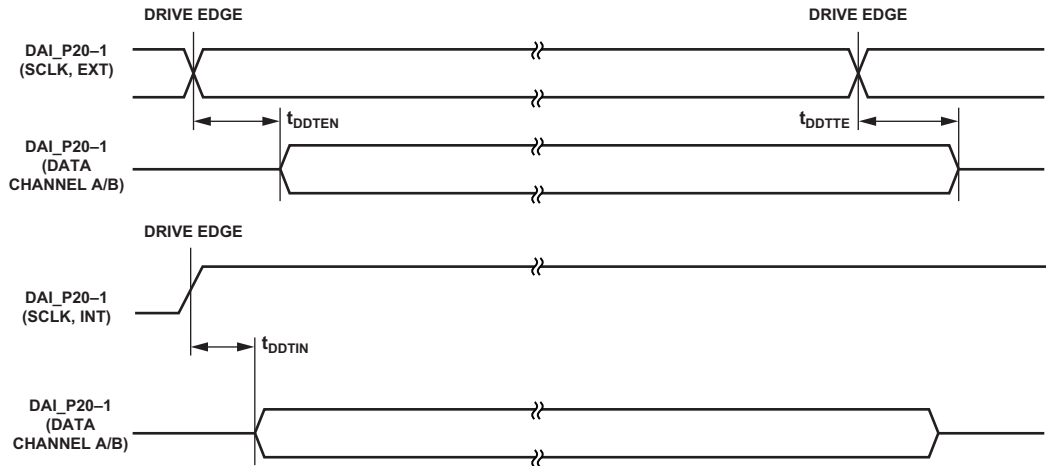


Figure 23. Serial Ports—Enable and Three-State

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Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in [Table 40](#). PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the

PDAP chapter of the hardware reference. Note that the 20 bits of external PDAP data can be provided through the ADDR23–4 pins or over the DAI pins.

Table 40. Parallel Data Acquisition Port (PDAP)

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SPHOLD}^1			ns
PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		
t_{HPHOLD}^1			ns
PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		
t_{PDS}^1			ns
PDAP_DAT Setup Before PDAP_CLK Sample Edge	3.85		
t_{PDHD}^1			ns
PDAP_DAT Hold After PDAP_CLK Sample Edge	2.5		
t_{PDCLKW}			ns
Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		
t_{PDCLK}			ns
Clock Period	$t_{PCLK} \times 4$		
<i>Switching Characteristics</i>			
t_{PDHLDD}			ns
Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		
t_{PDSTRB}			ns
PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$		

¹ Source pins of PDAP_DATA are ADDR23–4 or DAI pins. Source pins for PDAP_CLK and PDAP_HOLD are 1) DAI pins; 2) CLKIN through PCG; 3) DAI pins through PCG; or 4) ADDR3–2 pins.

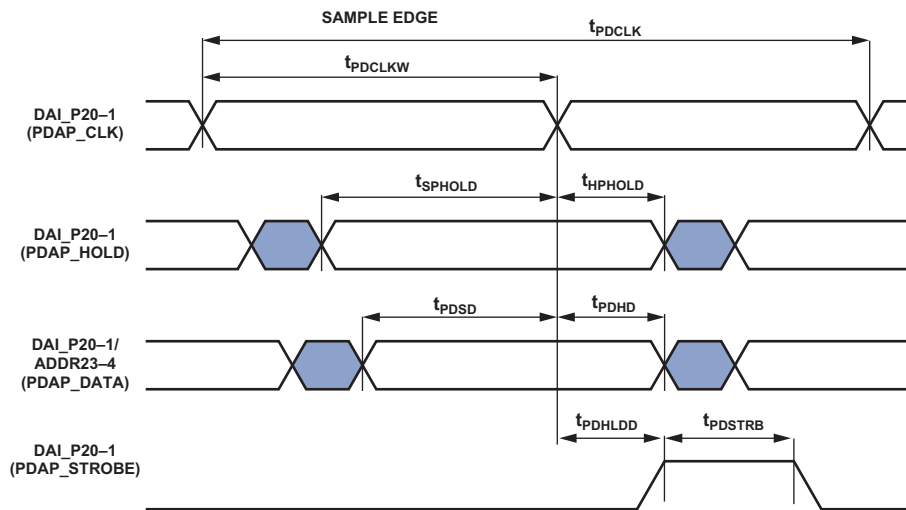


Figure 26. PDAP Timing

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

Sample Rate Converter—Serial Output Port

For the serial output port, the frame sync is an input, and it should meet setup and hold times with regard to SCLK on the output port. The serial data output has a hold time and delay

specification with regard to serial clock. Note that serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

Table 42. ASRC, Serial Output Port

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SRCSFS}^1 Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}^1 Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCLKW} Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCLLK} Clock Period	$t_{PCLK} \times 4$		ns
<i>Switching Characteristics</i>			
t_{SRCTDD}^1 Transmit Data Delay After Serial Clock Falling Edge		9.9	ns
t_{SRCTDH}^1 Transmit Data Hold After Serial Clock Falling Edge	1		ns

¹The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

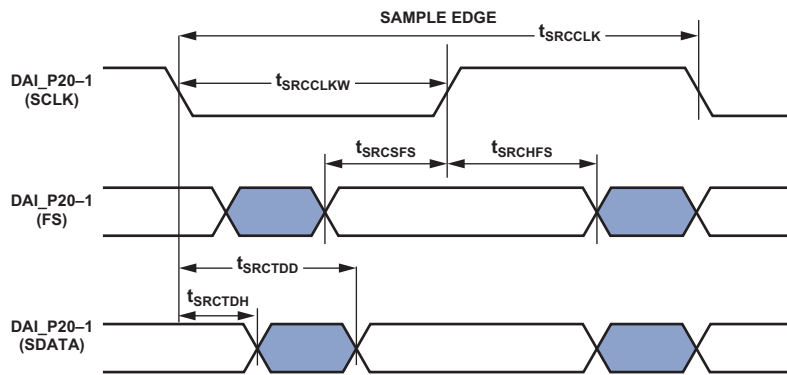


Figure 28. ASRC Serial Output Port Timing



Figure 38. MLB Timing (5-Pin Interface)

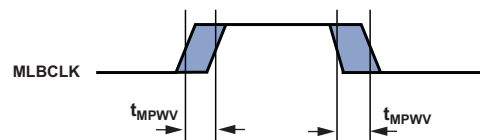


Figure 39. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the hardware reference.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the hardware reference.

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OUTPUT DRIVE CURRENTS

Figure 41 shows typical I-V characteristics for the output drivers of the ADSP-2148x, and Table 55 shows the pins associated with each driver. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 55. Driver Types

Driver Type	Associated Pins
A	FLAG[0-3], AMI_ADDR[0-23], DATA[0-15], AMI_RD, AMI_WR, AMI_ACK, MS[1-0], SDRAS, SDCAS, SDWE, SDDQM, SDCKE, SDA10, EMU, TDO, RESETOUT, DPI[1-14], DAI[1-20], WDTRSTO, MLBDAT, MLBSIG, MLBSO, MLBDO, MLBCLK
B	SDCLK



Figure 41. Typical Drive at Junction Temperature

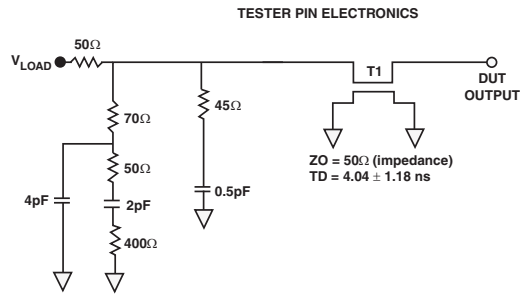
TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 21 on Page 26 through Table 54 on Page 54. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 42.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 43. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.



Figure 43. Voltage Reference Levels for AC Measurements



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 42. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 42). Figure 46 and Figure 47 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 44 through Figure 47 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.



Figure 44. Typical Output Rise/Fall Time (20% to 80%, $V_{DD_EXT} = Max$)

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Figure 48 shows the top view of the 100-lead LQFP_EP lead configuration. Figure 49 shows the bottom view of the 100-lead LQFP_EP lead configuration.

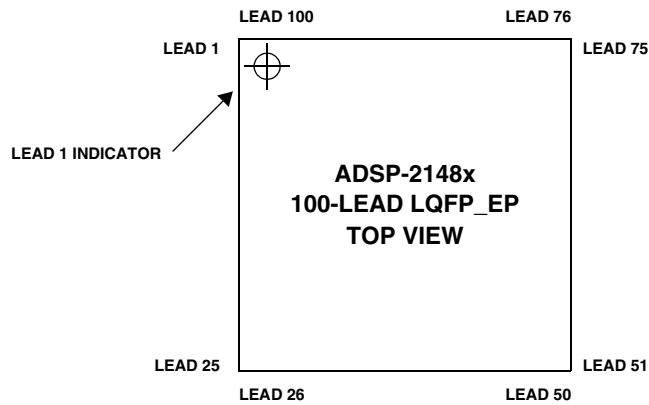


Figure 48. 100-Lead LQFP_EP Lead Configuration (Top View)

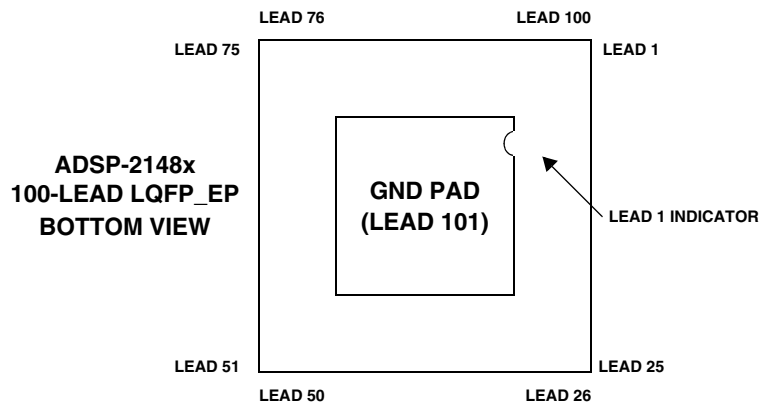


Figure 49. 100-Lead LQFP_EP Lead Configuration (Bottom View)

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
NC	1	V _{DD_EXT}	45	DAI_P10	89	V _{DD_INT}	133
$\overline{MS0}$	2	DPI_P08	46	V _{DD_INT}	90	FLAG0	134
NC	3	DPI_P07	47	V _{DD_EXT}	91	FLAG1	135
V _{DD_INT}	4	V _{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V _{DD_INT}	93	GND	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	GND	139
V _{DD_EXT}	8	DPI_P12	52	DAI_P04	96	GND	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V _{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	GND	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V _{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	\overline{TRST}	144
ADDR5	13	V _{DD_EXT}	57	DAI_P15	101	GND	145
BOOT_CFG1	14	NC	58	V _{DD_INT}	102	\overline{EMU}	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V _{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V _{DD_INT}	105	DATA2	149
NC	18	V _{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V _{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V _{DD_INT}	65	GND	109	V _{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V _{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V _{DD_INT}	68	V _{DD_THD}	112	V _{DD_INT}	156
XTAL	25	NC	69	V _{DD_INT}	113	DATA7	157
ADDR10	26	$\overline{WDTRSTO}$	70	V _{DD_INT}	114	TDI	158
NC	27	NC	71	$\overline{MS1}$	115	NC	159*
V _{DD_EXT}	28	V _{DD_EXT}	72	V _{DD_INT}	116	V _{DD_EXT}	160
V _{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V _{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V _{DD_INT}	34	V _{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V _{DD_INT}	123	DATA14	167
$\overline{RESETOUT}/\overline{RUNRSTIN}$	36	NC	80	ADDR20	124	DATA13	168
V _{DD_INT}	37	NC	81	ADDR19	125	V _{DD_INT}	169
DPI_P01	38	NC	82	V _{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	NC	171
DPI_P03	40	V _{DD_EXT}	84	ADDR15	128	NC	172
V _{DD_INT}	41	V _{DD_INT}	85	V _{DD_INT}	129	\overline{RESET}	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	$\overline{AMI_WR}$	131	NC	175
DPI_P06	44	DAI_P09	88	$\overline{AMI_RD}$	132	V _{DD_INT}	176
						GND	177**

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

Table 62. Automotive Models ADSP-21488, and ADSP-21489 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
SDDQM	1	V _{DD_EXT}	45	DAI_P10	89	V _{DD_INT}	133
$\overline{MS0}$	2	DPI_P08	46	V _{DD_INT}	90	FLAG0	134
SDCKE	3	DPI_P07	47	V _{DD_EXT}	91	FLAG1	135
V _{DD_INT}	4	V _{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V _{DD_INT}	93	MLBCLK	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	MLBDAT	139
V _{DD_EXT}	8	DPI_P12	52	DAI_P04	96	MLBDO	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V _{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	MLBSIG	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V _{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	\overline{TRST}	144
ADDR5	13	V _{DD_EXT}	57	DAI_P15	101	MLBSO	145
BOOT_CFG1	14	NC	58	V _{DD_INT}	102	EMU	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V _{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V _{DD_INT}	105	DATA2	149
NC	18	V _{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V _{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V _{DD_INT}	65	GND	109	V _{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V _{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V _{DD_INT}	68	V _{DD_THD}	112	V _{DD_INT}	156
XTAL	25	NC	69	V _{DD_INT}	113	DATA7	157
ADDR10	26	$\overline{WDTRSTO}$	70	V _{DD_INT}	114	TDI	158
SDA10	27	NC	71	$\overline{MS1}$	115	SDCLK	159
V _{DD_EXT}	28	V _{DD_EXT}	72	V _{DD_INT}	116	V _{DD_EXT}	160
V _{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V _{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V _{DD_INT}	34	V _{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V _{DD_INT}	123	DATA14	167
$\overline{RESETOUT}/\overline{RUNRSTIN}$	36	NC	80	ADDR20	124	DATA13	168
V _{DD_INT}	37	NC	81	ADDR19	125	V _{DD_INT}	169
DPI_P01	38	NC	82	V _{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	\overline{SDWE}	171
DPI_P03	40	V _{DD_EXT}	84	ADDR15	128	\overline{SDRAS}	172
V _{DD_INT}	41	V _{DD_INT}	85	V _{DD_INT}	129	RESET	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	$\overline{AMI_WR}$	131	\overline{SDCAS}	175
DPI_P06	44	DAI_P09	88	$\overline{AMI_RD}$	132	V _{DD_INT}	176
						GND	177*

* Lead no. 177 (exposed pad) is the GND supply (see [Figure 50](#) and [Figure 51](#)) for the processor; this pad must be **robustly** connected to GND.

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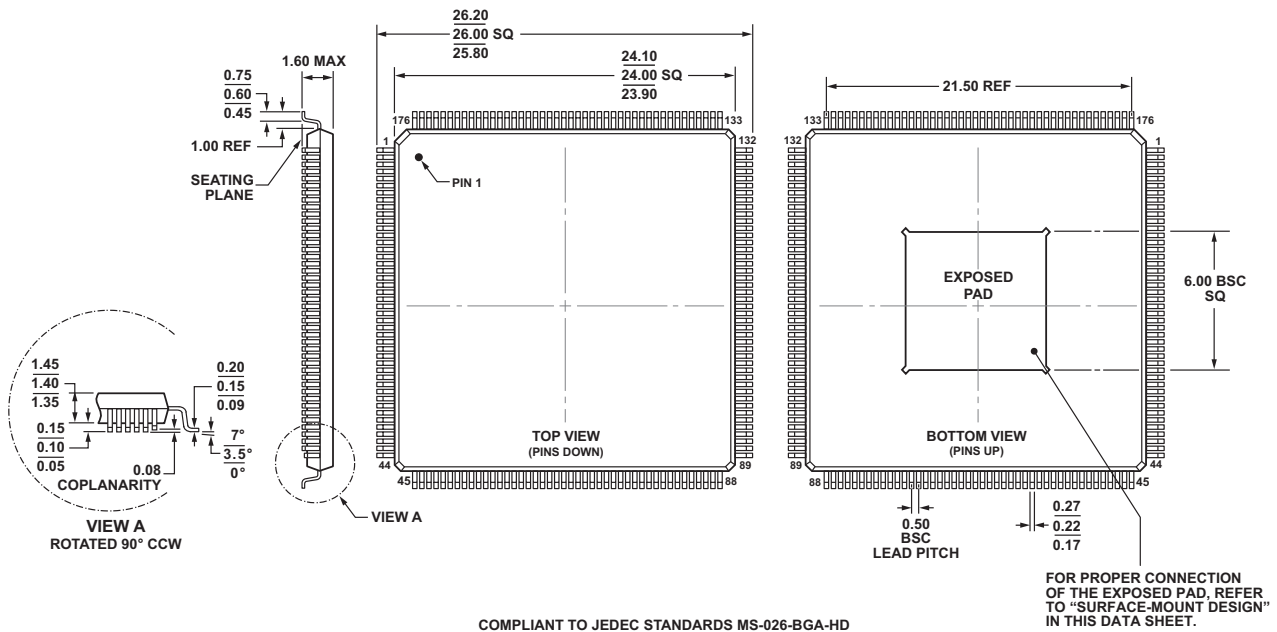


Figure 53. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]¹
(SW-176-2)

Dimensions shown in millimeters

¹For information relating to the exposed pad on the SW-176-2 package, see the table endnote on Page 60.

SURFACE-MOUNT DESIGN

The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be robustly connected to the GND plane in the PCB for best electrical and thermal performance. No separate GND pins are provided in the package.

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product [Specifications on](#)

[Page 18](#) section of this data sheet carefully. Only the automotive grade products shown in [Table 63](#) are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 63. Automotive Products

Model ^{1, 2, 3, 4}	Notes	Temperature Range ⁵	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
AD21486WBSWZ4Axx	⁶	-40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Axx	⁶	-40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Bxx	⁶	-40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ1Axx		-40°C to +85°C	3 Mbit	266 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ2Axx		-40°C to +85°C	3 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ1Bxx		-40°C to +85°C	2 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ2Bxx		-40°C to +85°C	3 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ4Bxx		-40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21489WBSWZ4xx		-40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4xxRL		-40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4Bxx		-40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2

¹Z =RoHS Compliant Part.

²W = automotive applications.

³xx denotes the current die revision.

⁴RL = Tape and Reel.

⁵Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see [Operating Conditions on Page 18](#) for junction temperature (T_j) specification which is the only temperature specification.

⁶This product contains IP from Dolby, DTS and DTLA. Proper software licenses required. Contact Analog Devices, Inc. for information.

ORDERING GUIDE

Model ¹	Notes	Temperature Range ²	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21483KSWZ-2B	³	0°C to +70°C	3 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3B	³	0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3AB	³	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21483KSWZ-4B	³	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2A	³	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2B	³	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2AB	³	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2BB	³	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3A	³	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3B	³	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3AB	³	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3BB	³	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-4A	³	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-4AB	³	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

Model ¹	Notes	Temperature Range ²	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21487KSWZ-2B	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-2BB	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3B	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3BB	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4B	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4BB	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5B	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5BB	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP21487KSWZ5BBRL	5	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3A		-40°C to +85°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A		0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A1	6	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3B		0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3B		-40°C to +85°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4A		0°C to +70°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488BSWZ-4A		-40°C to +85°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-4B		0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-4B		-40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4B1	6	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-3A		0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-3A		-40°C to +85°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-3B		0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-3B		-40°C to +85°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-4A		0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-4A		-40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-4B		0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-4B		-40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-5B	4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2

¹Z = RoHS compliant part.

²Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see [Operating Conditions on Page 18](#) for junction temperature (T_j) specification, which is the only temperature specification.

³The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

⁴See Engineer-to-Engineer Note [Static Voltage Scaling for ADSP-2148x SHARC Processors \(EE-357\)](#) for operating ADSP-2148x processors at 450 MHz.

⁵RL = Tape and Reel.

⁶This product contains a -140 dB sample rate converter.