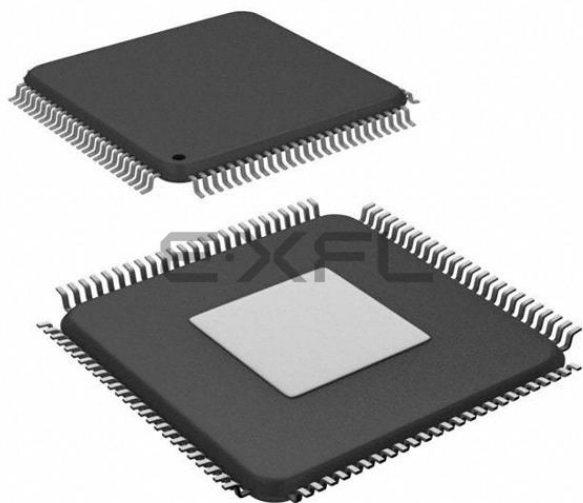




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Obsolete
Type	Floating Point
Interface	EBI/EMI, DAI, I ² C, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21488wbswz402

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

The diagram on [Page 1](#) shows the two clock domains that make up the ADSP-2148x processors. The core clock domain contains the following features:

- Two processing elements (PE_x, PE_y), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (5 Mbit) and mask-programmable ROM (4 Mbit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-2148x on [Page 1](#) also shows the peripheral clock domain (also known as the I/O processor) which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 memory-to-memory (MTM) unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP/PDAP) for serial and parallel interconnects, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface (TWI), one UART, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG), pulse width modulation (PWM), and a flexible signal routing unit (DPI SRU2).

As shown in the SHARC core block diagram on [Page 5](#), the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz.

FAMILY CORE ARCHITECTURE

The ADSP-2148x is code compatible at the assembly level with the ADSP-2147x, ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2148x shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x and ADSP-2116x SIMD SHARC processors, as shown in [Figure 2](#) and detailed in the following sections.

SIMD Computational Engine

The ADSP-2148x contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. SIMD mode allows the processor to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

SIMD mode also affects the way data is transferred between memory and the processing elements because twice the data bandwidth is required to sustain computational operation in the processing elements. Therefore, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each memory or register file access.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle and are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Timer

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

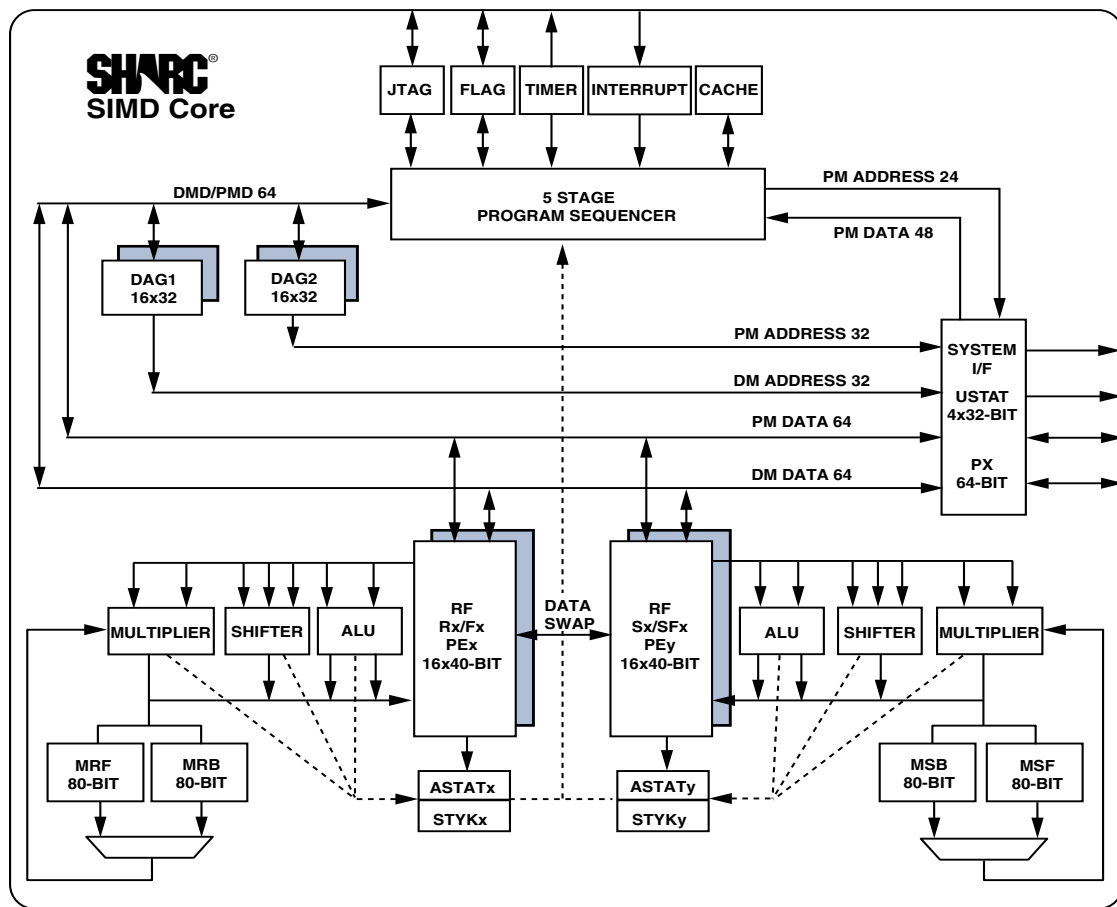


Figure 2. SHARC Core Block Diagram

Universal Registers

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all peripheral registers (control/status).

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2148x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data. With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose

fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processor can conditionally execute a multiply, an add, and a

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subtract in both processing elements while branching and fetching up to four 32-bit values from memory, all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the ADSP-2148x supports new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external

SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The ADSP-21483 and the ADSP-21488 processors contain 3 Mbits of internal RAM (Table 3) and the ADSP-21486, ADSP-21487, and ADSP-21489 processors contain 5 Mbits of internal RAM (Table 4). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor.

Table 3. Internal Memory Space (3 MBits—ADSP-21483/ADSP-21488)¹

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	Extended Precision Normal or Instruction Word (48 Bits)	Normal Word (32 Bits)	Short Word (16 Bits)
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 CFFF	Block 0 SRAM 0x0008 C000–0x0009 1554	Block 0 SRAM 0x0009 2000–0x0009 9FFF	Block 0 SRAM 0x0012 4000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 FFFF	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 CFFF	Block 1 SRAM 0x000A C000–0x000B 1554	Block 1 SRAM 0x000B 2000–0x000B 9FFF	Block 1 SRAM 0x0016 4000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0x000B FFFF	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000–0x0006 FFFF	Reserved 0x000C 2AAA–0x000D FFFF	Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF	Reserved 0x000E 2AAA–0x000F FFFF	Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF

¹ Some ADSP-2148x processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are

most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 3 and Table 4 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an

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Table 4. Internal Memory Space (5 MBits—ADSP-21486/ADSP-21487/ADSP-21489)¹

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	Extended Precision Normal or Instruction Word (48 Bits)	Normal Word (32 Bits)	Short Word (16 Bits)
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 EFFF	Block 0 SRAM 0x0008 C000–0x0009 3FFF	Block 0 SRAM 0x0009 2000–0x0009 DFFF	Block 0 SRAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 EFFF	Block 1 SRAM 0x000A C000–0x000B 3FFF	Block 1 SRAM 0x000B 2000–0x000B DFFF	Block 1 SRAM 0x0016 4000–0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 3FFF	Block 2 SRAM 0x000C 0000–0x000C 5554	Block 2 SRAM 0x000C 0000–0x000C 7FFF	Block 2 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0006 FFFF	Reserved 0x000C 5555–0x000D FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 3FFF	Block 3 SRAM 0x000E 0000–0x000E 5554	Block 3 SRAM 0x000E 0000–0x000E 7FFF	Block 3 SRAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x000F FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

¹ Some ADSP-2148x processors include a customer-definable ROM block and are not reserved as shown on this table. Please contact your Analog Devices sales representative for additional details.

instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

ROM Based Security

The ADSP-2148x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features are available after the correct key is scanned.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2×64 -bits, CCLK speed) and the IOD0/1 buses (2×32 -bit, PCLK speed).

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2148x family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Memory

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 6M words of external memory in bank 0 and 8M words of external memory in bank 1, bank 2, and bank 3.
- A SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in bank 0, and 64M words of external memory in bank 1, bank 2, and bank 3. NOTE: This feature is not available on the ADSP-21486 product.

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Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from non contiguous memory blocks.

FFT Accelerator

The FFT accelerator implements a radix-2 complex/real input, complex output FFT with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watchdog Timer

The watchdog timer is used to supervise the stability of the system software. When used in this way, software reloads the watchdog timer in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset, if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer. The watchdog timer resets both the core and the internal peripherals. Note that this feature is available on the 176-lead package only.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2148x boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2-0) pins in [Table 9](#) for the 176-lead package and [Table 10](#) for the 100-lead package.

Table 9. Boot Mode Selection, 176-Lead Package

BOOT_CFG2-0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI User Boot (for 8-bit Flash Boot)
011	No boot (processor executes from internal ROM after reset)
1xx	Reserved

Table 10. Boot Mode Selection, 100-Lead Package

BOOT_CFG1-0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Reserved
11	No boot (processor executes from internal ROM after reset)

The “Running Reset” feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the RESETOUT/RUNRSTIN pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the hardware reference.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal supply must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Static Voltage Scaling (SVS)

Some models of the ADSP-2148x feature Static Voltage Scaling (SVS) on the V_{DD_INT} power supply. (See the [Ordering Guide on Page 66](#) for model details.) This voltage specification technique can provide significant performance benefits including 450 MHz core frequency operation without a significant increase in power.

SVS optimizes the required V_{DD_INT} voltage for each individual device to enable enhanced operating frequency up to 450 MHz. The optimized SVS voltage results in a reduction of maximum I_{DD_INT} which enables 450 MHz operation at the same or lower maximum power than 400 MHz operation at a fixed voltage supply. Implementation of SVS requires a specific voltage regulator circuit design and initialization code.

Refer to the Engineer-to-Engineer Note [Static Voltage Scaling for ADSP-2148x SHARC Processors \(EE-357\)](#) for further information. The EE-Note details the requirements and process to implement a SVS power supply system to enable operation up to 450 MHz. This applies only to specific products within the ADSP-2148x family which are capable of supporting 450 MHz operation.

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Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{SDRAS}}$	O/T (ipu)	High-Z/ driven high	SDRAM Row Address Strobe. Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (ipu)	High-Z/ driven high	SDRAM Column Address Select. Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (ipu)	High-Z/ driven high	SDRAM Write Enable. Connect to SDRAM's WE or W buffer pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
SDCKE	O/T (ipu)	High-Z/ driven high	SDRAM Clock Enable. Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (ipu)	High-Z/ driven high	SDRAM A10 Pin. Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's ADDR10 pin only during SDRAM accesses.
SDDQM	O/T (ipu)	High-Z/ driven high	DQM Data Mask. SDRAM Input mask signal for write accesses and output mask signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The SDRAM output buffers are placed in a High-Z state when DQM is sampled high during a read cycle. SDDQM is driven high from reset de-assertion until SDRAM initialization completes. Afterwards it is driven low irrespective of whether any SDRAM accesses occur or not.
SDCLK	O/T (ipd)	High-Z/ driving	SDRAM Clock Output. Clock driver for this pin differs from all other clock drivers. See Figure 41 on Page 55 . For models in the 100-lead package, the SDRAM interface should be disabled to avoid unnecessary power switching by setting the DSDCTL bit in SDCTL register. For more information, see the hardware reference.
DAI_P20-1	I/O/T (ipu)	High-Z	Digital Applications Interface. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins.
DPI_P14-1	I/O/T (ipu)	High-Z	Digital Peripheral Interface. These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins.
WDT_CLKIN	I		Watchdog Timer Clock Input. This pin should be pulled low when not used.
WDT_CLKO	O		Watchdog Resonator Pad Output.
$\overline{\text{WDTRSTO}}$	O (ipu)		Watchdog Timer Reset Out.
THD_P	I		Thermal Diode Anode. When not used, this pin can be left floating.
THD_M	O		Thermal Diode Cathode. When not used, this pin can be left floating.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 k Ω –63 k Ω . The range of an ipd resistor can be between 31 k Ω –85k Ω . The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTTL compliant with the exception of the thermal diode pins.

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ELECTRICAL CHARACTERISTICS

Parameter ¹	Description	Test Conditions	300 MHz / 350 MHz / 400 MHz / 450 MHz			Unit
			Min	Typ	Max	
V _{OH} ²	High Level Output Voltage	@ V _{DD_EXT} = Min, I _{OH} = -1.0 mA ³	2.4			V
V _{OL} ²	Low Level Output Voltage	@ V _{DD_EXT} = Min, I _{OL} = 1.0 mA ³			0.4	V
I _{IH} ^{4,5}	High Level Input Current	@ V _{DD_EXT} = Max, V _{IN} = V _{DD_EXT} Max			10	μA
I _{IL} ⁴	Low Level Input Current	@ V _{DD_EXT} = Max, V _{IN} = 0 V			10	μA
I _{ILPU} ⁵	Low Level Input Current Pull-up	@ V _{DD_EXT} = Max, V _{IN} = 0 V			200	μA
I _{OZH} ^{6,7}	Three-State Leakage Current	@ V _{DD_EXT} = Max, V _{IN} = V _{DD_EXT} Max			10	μA
I _{OZL} ⁶	Three-State Leakage Current	@ V _{DD_EXT} = Max, V _{IN} = 0 V			10	μA
I _{OZLPU} ⁷	Three-State Leakage Current Pull-up	@ V _{DD_EXT} = Max, V _{IN} = 0 V			200	μA
I _{OZHPD} ⁸	Three-State Leakage Current Pull-down	@ V _{DD_EXT} = Max, V _{IN} = V _{DD_EXT} Max			200	μA
I _{DD_INT} ⁹	Supply Current (Internal)	f _{CLK} > 0 MHz			Table 14 + Table 15 × ASF	mA
I _{DD_INT}	Supply Current (Internal)	V _{DDINT} = 1.1 V, ASF = 1, T _J = 25°C		410 / 450 / 500 / 550		mA
C _{IN} ^{10, 11}	Input Capacitance	T _{CASE} = 25°C			5	pF

¹ Specifications subject to change without notice.

² Applies to output and bidirectional pins: ADDR23-0, DATA15-0, AMI_RD, AMI_WR, FLAG3-0, DAI_Px, DPI_Px, EMU, TDO, RESETOUT, MLBSIG, MLBDAT, MLBDO, MLBSO, SDRAS, SDCAS, SDWE, SDCKE, SDA10, SDDQM, MS0-I.

³ See [Output Drive Currents on Page 55](#) for typical drive current capabilities.

⁴ Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, RESET, CLKIN.

⁵ Applies to input pins with internal pull-ups: TRST, TMS, TDI.

⁶ Applies to three-statable pin: TDO.

⁷ Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, EMU.

⁸ Applies to three-statable pin with pull-down: SDCLK.

⁹ See Engineer-to-Engineer Note [Estimating Power for ADSP-214xx SHARC Processors \(EE-348\)](#) for further information.

¹⁰ Applies to all signal pins.

¹¹ Guaranteed, but not tested.

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TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See [Figure 43 on Page 55](#) for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, the processor core, and the serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1-0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see [Figure 4](#)). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

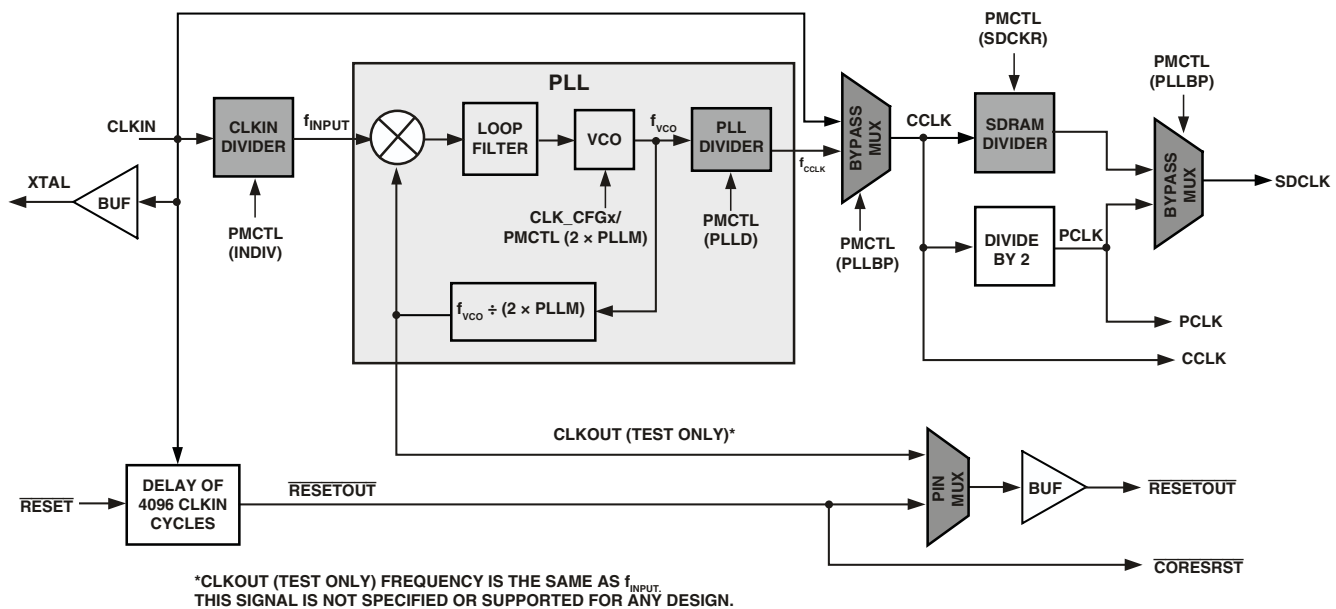


Figure 4. Core Clock and System Clock Relationship to CLKIN

Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in [Table 20](#).

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in [Table 20](#) if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in [Table 20](#) if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$

$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} = is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN $\div$ 2 when the input divider is enabled

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Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 23. Interrupts

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{IPW} $\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{\text{CLK}} + 2$		ns

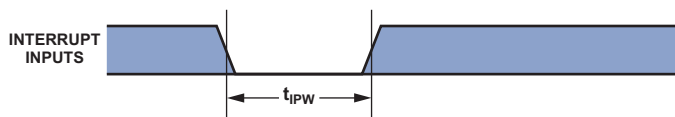


Figure 10. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
t_{WCTIM} TMREXP Pulse Width	$4 \times t_{\text{CLK}} - 1$		ns

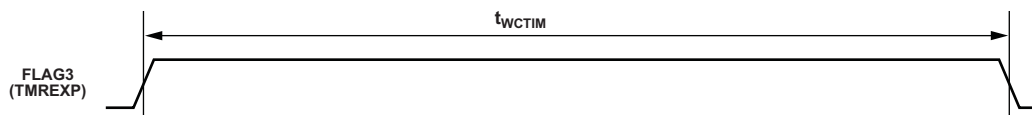


Figure 11. Core Timer

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Flags

The timing specifications provided below apply to the DPI_P14-1, ADDR7-0, ADDR23-8, DATA7-0, and FLAG3-0 pins when configured as FLAGS. See [Table 11 on Page 14](#) for more information on flag use.

Table 30. Flags

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{FIPW}^1 FLAGS IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
<i>Switching Characteristic</i>			
t_{FOPW}^1 FLAGS OUT Pulse Width	$2 \times t_{PCLK} - 3$		ns

¹This is applicable when the Flags are connected to DPI_P14-1, ADDR7-0, ADDR23-8, DATA7-0 and FLAG3-0 pins.



Figure 17. Flags

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SDRAM Interface Timing (166 MHz SDCLK)

The maximum frequency for SDRAM is 166 MHz. For information on SDRAM frequency and programming, see the hardware reference, Engineer-to-Engineer Note [Interfacing SDRAM Memories to SHARC Processors \(EE-286\)](#), and the SDRAM vendor data sheet.

Table 31. SDRAM Interface Timing

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SSDAT} DATA Setup Before SDCLK	0.7		ns
t_{HSDAT} DATA Hold After SDCLK	1.23		ns
<i>Switching Characteristics</i>			
t_{SDCLK}^1 SDCLK Period	6		ns
t_{SDCLKH} SDCLK Width High	2.2		ns
t_{SDCLKL} SDCLK Width Low	2.2		ns
t_{DCAD}^2 Command, ADDR, Data Delay After SDCLK		4	ns
t_{HCAD}^2 Command, ADDR, Data Hold After SDCLK	1		ns
t_{DSDAT} Data Disable After SDCLK		5.3	ns
t_{ENSDAT} Data Enable After SDCLK	0.3		ns

¹Systems should use the SDRAM model with a speed grade higher than the desired SDRAM controller speed. For example, to run the SDRAM controller at 166 MHz the SDRAM model with a speed grade of 183 MHz or above should be used. See Engineer-to-Engineer Note [Interfacing SDRAM Memories to SHARC Processors \(EE-286\)](#) for more information on hardware design guidelines for the SDRAM interface.

²Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, $\overline{SDA10}$, $\overline{SDCKE}$.

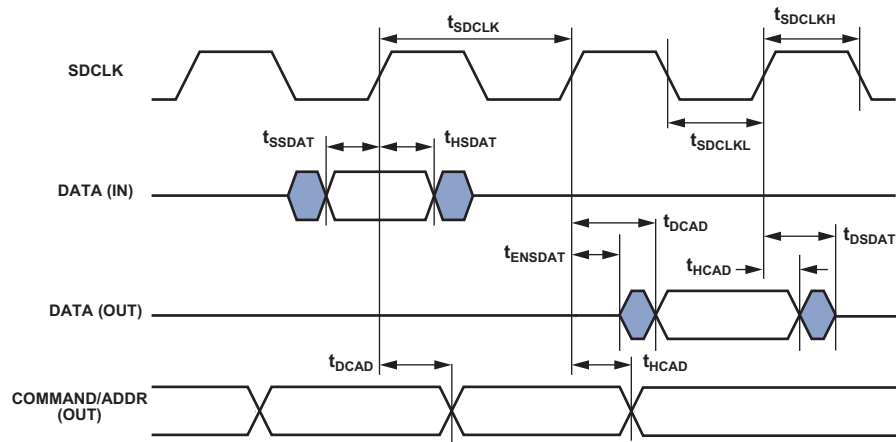


Figure 18. SDRAM Interface Timing

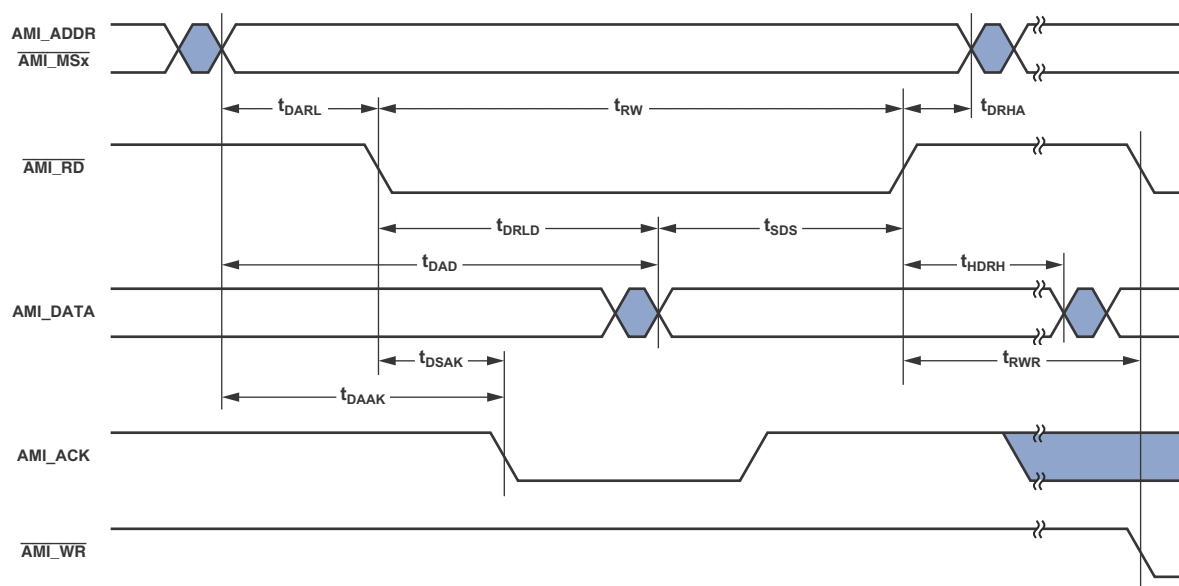


Figure 19. AMI Read

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Table 37. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
<i>Switching Characteristics</i>				
t_{DDTEN}^1	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}^1	Data Disable from External Transmit SCLK		11.5	ns
t_{DDTIN}^1	Data Enable from Internal Transmit SCLK	-1.5		ns

¹Referenced to drive edge.

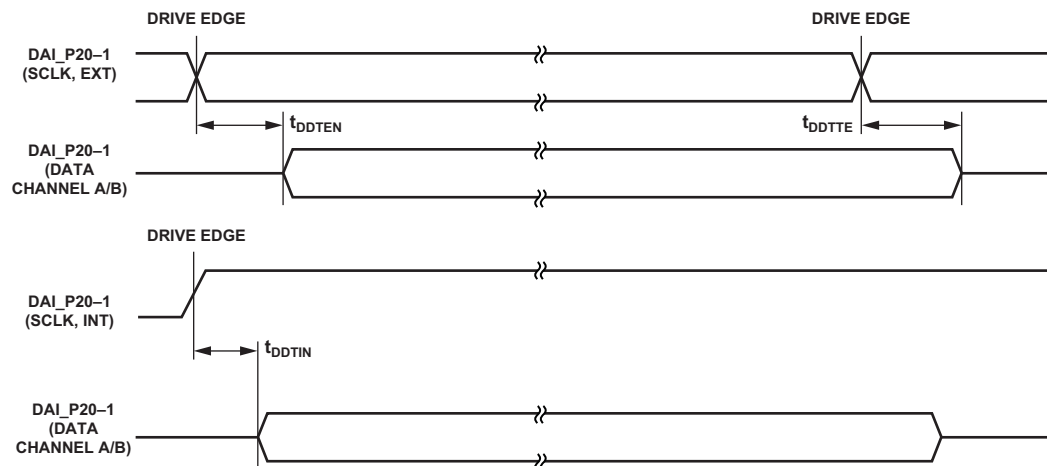


Figure 23. Serial Ports—Enable and Three-State

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S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 47. Input signals are routed to the DAI_P20-1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20-1 pins.

Table 47. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{SISFS}^1	Frame Sync Setup Before Serial Clock Rising Edge	3		ns
t_{SIHFS}^1	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}^1	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}^1	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

¹ The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

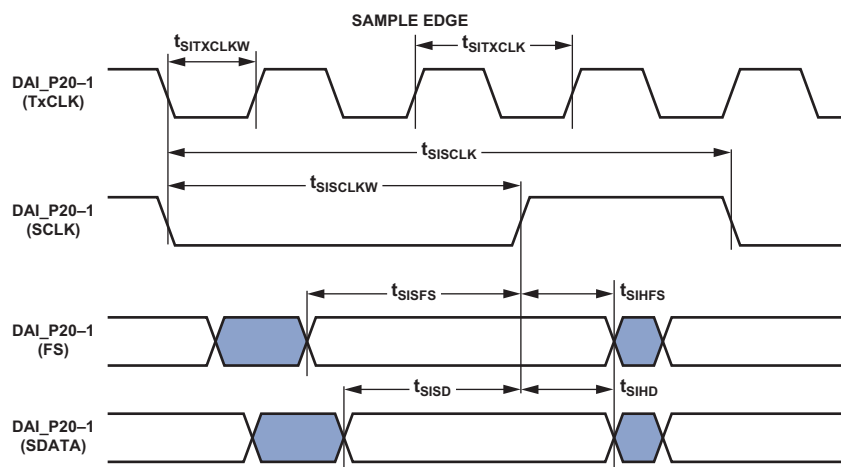


Figure 33. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 48. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Max	Unit
Frequency for TxCLK = $384 \times$ Frame Sync	Oversampling Ratio $\times$ Frame Sync $\leq 1/t_{SITXCLK}$	MHz
Frequency for TxCLK = $256 \times$ Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

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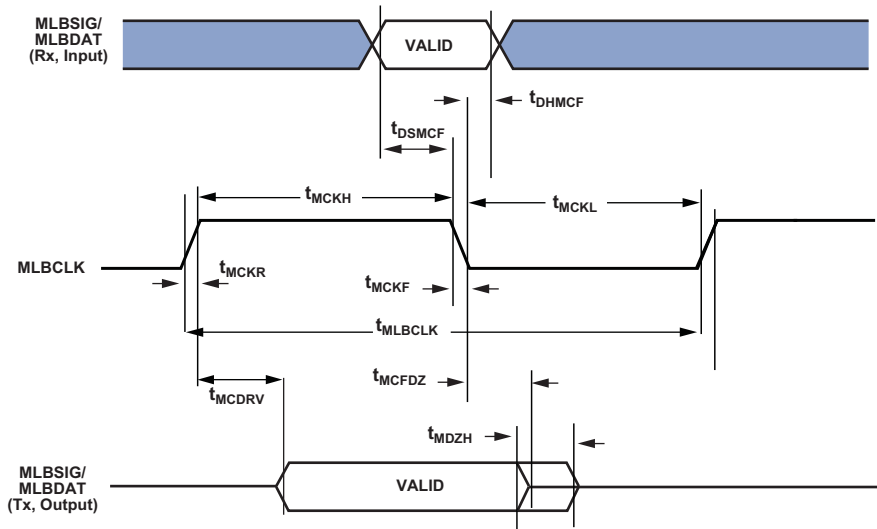


Figure 37. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV} ¹	MLBCLK Pulse Width Variation			2	nspp
t_{DSMCF} ²	DAT/SIG Input Setup Time	3			ns
t_{DHMCf}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL} ³	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{MLB}	DS/DO Pin Load			40	pf

¹Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).

²Gate Delays due to OR'ing logic on the pins must be accounted for.

³When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

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JTAG Test Access Port and Emulation

Table 54. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}^1	System Inputs Setup Before TCK High	7		ns
t_{HSYS}^1	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
<i>Switching Characteristics</i>				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}^2	System Outputs Delay After TCK Low		$t_{TCK} \div 2 + 7$	ns

¹System Inputs = DATA15–0, CLK_CFG1–0, $\overline{RESET}$, BOOT_CFG2–0, DAI_Px, DPI_Px, and FLAG3–0.

²System Outputs = DAI_Px, DPI_Px ADDR23–0, $\overline{AMI_RD}$, $\overline{AMI_WR}$, FLAG3–0, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDDQM, SDCLK and EMU.

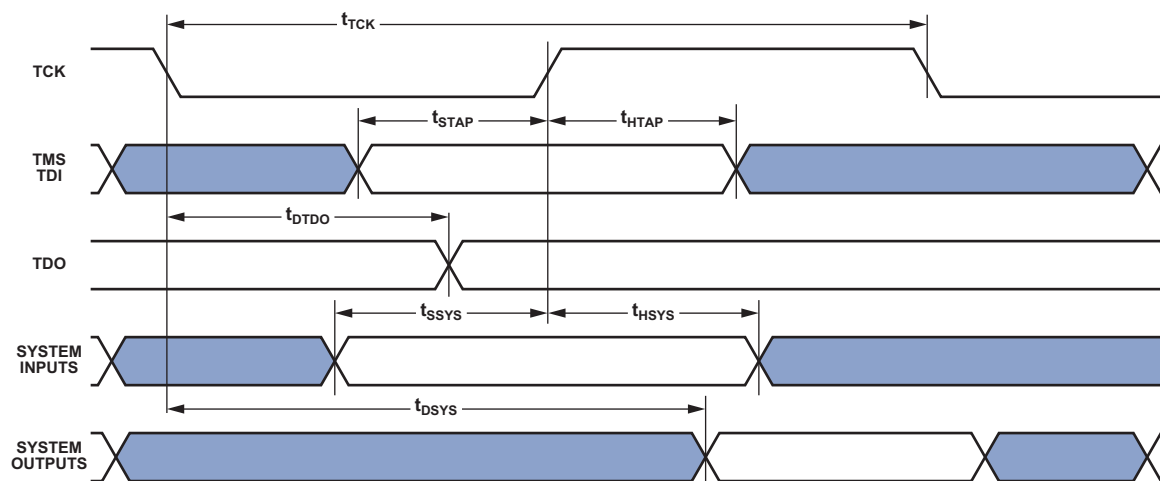


Figure 40. IEEE 1149.1 JTAG Test Access Port

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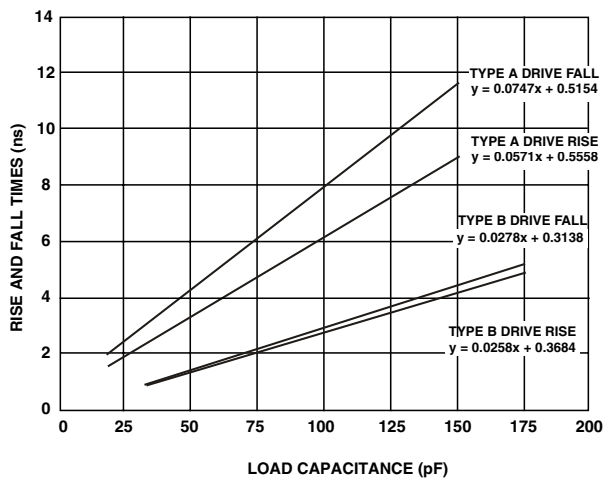


Figure 45. Typical Output Rise/Fall Time
(20% to 80%, $V_{DD_EXT} = \text{Min}$)

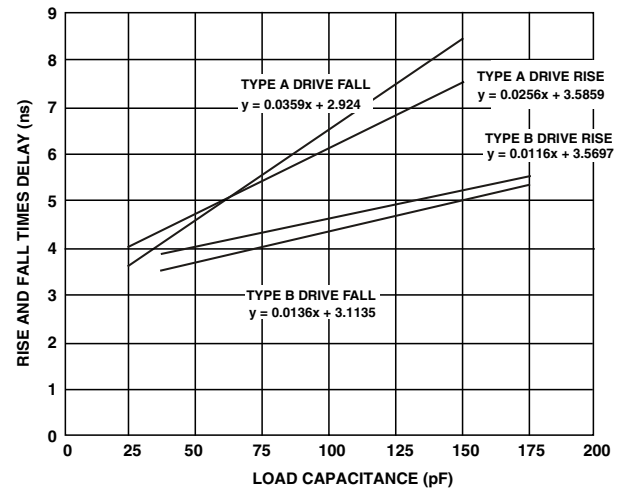


Figure 47. Typical Output Rise/Fall Delay
($V_{DD_EXT} = \text{Min}$)

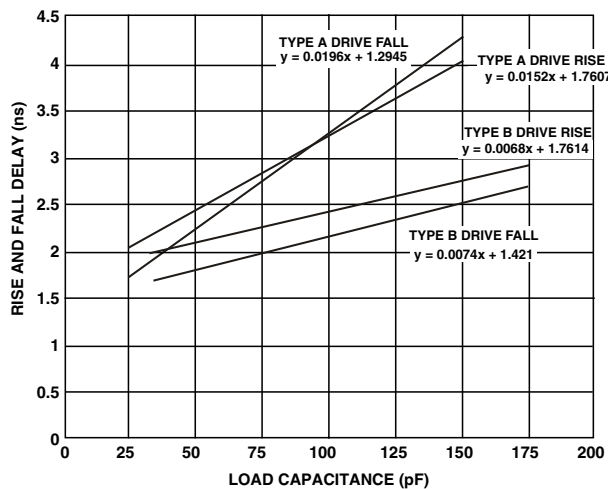


Figure 46. Typical Output Rise/Fall Delay
($V_{DD_EXT} = \text{Max}$)

THERMAL CHARACTERISTICS

The ADSP-2148x processor is rated for performance over the temperature range specified in [Operating Conditions on Page 18](#).

[Table 57](#) airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (LQFP_EP). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from [Table 57](#).

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

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Figure 48 shows the top view of the 100-lead LQFP_EP lead configuration. Figure 49 shows the bottom view of the 100-lead LQFP_EP lead configuration.

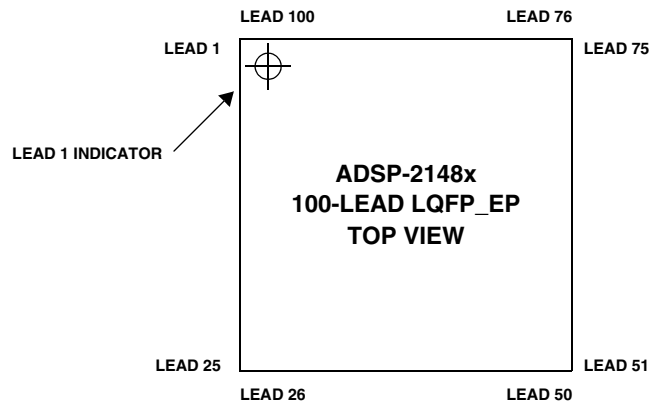


Figure 48. 100-Lead LQFP_EP Lead Configuration (Top View)

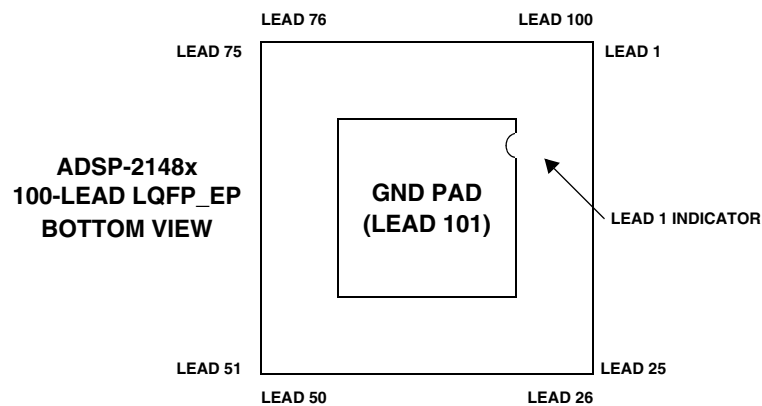


Figure 49. 100-Lead LQFP_EP Lead Configuration (Bottom View)

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176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
NC	1	V _{DD_EXT}	45	DAI_P10	89	V _{DD_INT}	133
$\overline{\text{MS0}}$	2	DPI_P08	46	V _{DD_INT}	90	FLAG0	134
NC	3	DPI_P07	47	V _{DD_EXT}	91	FLAG1	135
V _{DD_INT}	4	V _{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V _{DD_INT}	93	GND	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	GND	139
V _{DD_EXT}	8	DPI_P12	52	DAI_P04	96	GND	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V _{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	GND	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V _{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	$\overline{\text{TRST}}$	144
ADDR5	13	V _{DD_EXT}	57	DAI_P15	101	GND	145
BOOT_CFG1	14	NC	58	V _{DD_INT}	102	$\overline{\text{EMU}}$	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V _{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V _{DD_INT}	105	DATA2	149
NC	18	V _{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V _{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V _{DD_INT}	65	GND	109	V _{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V _{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V _{DD_INT}	68	V _{DD_THD}	112	V _{DD_INT}	156
XTAL	25	NC	69	V _{DD_INT}	113	DATA7	157
ADDR10	26	$\overline{\text{WDTRSTO}}$	70	V _{DD_INT}	114	TDI	158
NC	27	NC	71	$\overline{\text{MST}}$	115	NC	159*
V _{DD_EXT}	28	V _{DD_EXT}	72	V _{DD_INT}	116	V _{DD_EXT}	160
V _{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V _{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V _{DD_INT}	34	V _{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V _{DD_INT}	123	DATA14	167
$\overline{\text{RESETOUT}}/\text{RUNRSTIN}$	36	NC	80	ADDR20	124	DATA13	168
V _{DD_INT}	37	NC	81	ADDR19	125	V _{DD_INT}	169
DPI_P01	38	NC	82	V _{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	NC	171
DPI_P03	40	V _{DD_EXT}	84	ADDR15	128	NC	172
V _{DD_INT}	41	V _{DD_INT}	85	V _{DD_INT}	129	$\overline{\text{RESET}}$	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	$\overline{\text{AMI_WR}}$	131	NC	175
DPI_P06	44	DAI_P09	88	$\overline{\text{AMI_RD}}$	132	V _{DD_INT}	176
						GND	177**

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see [Figure 50](#) and [Figure 51](#)) for the processor; this pad must be **robustly** connected to GND.

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AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product [Specifications on](#)

[Page 18](#) section of this data sheet carefully. Only the automotive grade products shown in [Table 63](#) are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 63. Automotive Products

Model ^{1, 2, 3, 4}	Notes	Temperature Range ⁵	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
AD21486WBSWZ4Axx	⁶	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Axx	⁶	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Bxx	⁶	–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ1Axx		–40°C to +85°C	3 Mbit	266 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ2Axx		–40°C to +85°C	3 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ1Bxx		–40°C to +85°C	2 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ2Bxx		–40°C to +85°C	3 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ4Bxx		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21489WBSWZ4xx		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4xxRL		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4Bxx		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2

¹Z = RoHS Compliant Part.

²W = automotive applications.

³xx denotes the current die revision.

⁴RL = Tape and Reel.

⁵Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see [Operating Conditions on Page 18](#) for junction temperature (T_j) specification which is the only temperature specification.

⁶This product contains IP from Dolby, DTS and DTLA. Proper software licenses required. Contact Analog Devices, Inc. for information.

ORDERING GUIDE

Model ¹	Notes	Temperature Range ²	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21483KSWZ-2B	³	0°C to +70°C	3 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3B	³	0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3AB	³	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21483KSWZ-4B	³	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2A	³	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2B	³	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2AB	³	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2BB	³	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3A	³	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3B	³	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3AB	³	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3BB	³	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-4A	³	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-4AB	³	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2