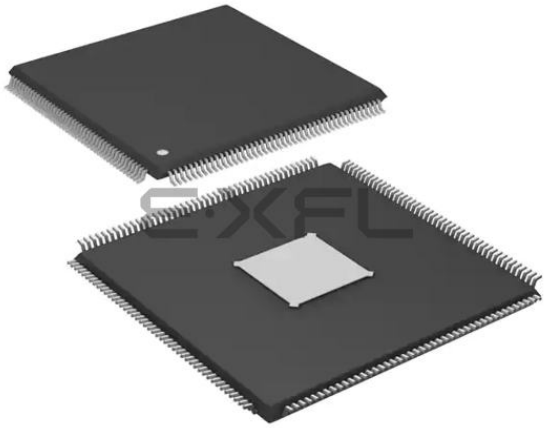

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	E/ ICENI, DAI, IBM, SPI, SP² OT, UAOTCUSAOT
Mlock Oate	R44N Hz
5on-0olatile Nemory	External
² n-Mhip OAN	VN bit
0oltage - IC²	1.140
0oltage - More	6.640
² perating Temperature	-R43M° 6~V3M (T7)
Nounting Type	Surface Nount
Package CMase	6: 2-L@FP Exposed Pad
Supplier Device Package	6: 2-L@FP-EP (~Rx~R)
Purchase UOL	httpsXCCwww.e-xfl.comCproduct-detailCanalog-devicesCad~6RWKwbswzRb4~

The diagram on Page 1 shows the two clock domains that make up the ADSP-2148x processors. The core clock domain contains the following features:

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (5 Mbit) and mask-programmable ROM (4 Mbit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-2148x on Page 1 also shows the peripheral clock domain (also known as the I/O processor) which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 memory-to-memory (MTM) unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP/PDAP) for serial and parallel interconnects, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface (TWI), one UART, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG), pulse width modulation (PWM), and a flexible signal routing unit (DPI SRU2).

As shown in the SHARC core block diagram on Page 5, the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz.

FAMILY CORE ARCHITECTURE

The ADSP-2148x is code compatible at the assembly level with the ADSP-2147x, ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2148x shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The ADSP-2148x contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEx is always active, and PEy may be enabled by setting the PEYEN mode bit in the MODE1 register. SIMD mode allows the processor to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

SIMD mode also affects the way data is transferred between memory and the processing elements because twice the data bandwidth is required to sustain computational operation in the processing elements. Therefore, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each memory or register file access.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle and are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Timer

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single-update mode or double-update mode. In single-update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double-update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

MediaLB

The automotive models of the ADSP-2148x processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive models, see Automotive Products on Page 66.

Digital Applications Interface (DAI)

The digital applications interface (DAI) allows the connection of various peripherals to any of the DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes eight serial ports, four precision clock generators (PCG), a S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports (SPORTs)

The ADSP-2148x features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^2S or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, or the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter (SRC)

The asynchronous sample rate converter contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode.

The IDP also provides a parallel data acquisition port (PDAP), which can be used for receiving parallel data. The PDAP port has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from non contiguous memory blocks.

FFT Accelerator

The FFT accelerator implements a radix-2 complex/real input, complex output FFT with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watchdog Timer

The watchdog timer is used to supervise the stability of the system software. When used in this way, software reloads the watchdog timer in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset, if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer. The watchdog timer resets both the core and the internal peripherals. Note that this feature is available on the 176-lead package only.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2148x boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2–0) pins in Table 9 for the 176-lead package and Table 10 for the 100-lead package.

Table 9. Boot Mode Selection, 176-Lead Package

BOOT_CFG2–0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI User Boot (for 8-bit Flash Boot)
011	No boot (processor executes from internal ROM after reset)
1xx	Reserved

Table 10. Boot Mode Selection, 100-Lead Package

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Reserved
11	No boot (processor executes from internal ROM after reset)

The "Running Reset" feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the RESETOUT/RUNRSTIN pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the hardware reference.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal supply must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Static Voltage Scaling (SVS)

Some models of the ADSP-2148x feature Static Voltage Scaling (SVS) on the V_{DD_INT} power supply. (See the Ordering Guide on Page 66 for model details.) This voltage specification technique can provide significant performance benefits including 450 MHz core frequency operation without a significant increase in power.

SVS optimizes the required V_{DD_INT} voltage for each individual device to enable enhanced operating frequency up to 450 MHz. The optimized SVS voltage results in a reduction of maximum I_{DD_INT} which enables 450 MHz operation at the same or lower maximum power than 400 MHz operation at a fixed voltage supply. Implementation of SVS requires a specific voltage regulator circuit design and initialization code.

Refer to the Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for further information. The EE-Note details the requirements and process to implement a SVS power supply system to enable operation up to 450 MHz. This applies only to specific products within the ADSP-2148x family which are capable of supporting 450 MHz operation.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{SDRAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
SDCKE	O/T (ipu)	High-Z/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (ipu)	High-Z/ driven high	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's ADDR10 pin only during SDRAM accesses.
SDDQM	O/T (ipu)	High-Z/ driven high	**DQM Data Mask.** SDRAM Input mask signal for write accesses and output mask signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The SDRAM output buffers are placed in a High-Z state when DQM is sampled high during a read cycle. SDDQM is driven high from reset de-assertion until SDRAM initialization completes. Afterwards it is driven low irrespective of whether any SDRAM accesses occur or not.
SDCLK	O/T (ipd)	High-Z/ driving	**SDRAM Clock Output.** Clock driver for this pin differs from all other clock drivers. See Figure 41 on Page 55. For models in the 100-lead package, the SDRAM interface should be disabled to avoid unnecessary power switching by setting the DSDCTL bit in SDCTL register. For more information, see the hardware reference.
DAI _P_{20-1}	I/O/T (ipu)	High-Z	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins.
DPI _P_{14-1}	I/O/T (ipu)	High-Z	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins.
WDT_CLKIN	I		**Watchdog Timer Clock Input.** This pin should be pulled low when not used.
WDT_CLKO	O		**Watchdog Resonator Pad Output.**
$\overline{\text{WDTRSTO}}$	O (ipu)		**Watchdog Timer Reset Out.**
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
MLBCLK[1]	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS=48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT[1]	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG[1]	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO[1]	O/T	High-Z	**Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
MLBSO[1]	O/T	High-Z	**Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{\text{EMU}}$	O (O/D, ipu)	High-Z	**Emulation Status.** Must be connected to the ADSP-2148x Analog Devices DSP Tools product line of JTAG emulators target board connector only.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	300 MHz / 350 MHz / 400 MHz			450 MHz			Unit
		Min	Nominal	Max	Min	Nominal	Max	
V_{DD_INT}[2]	Internal (Core) Supply Voltage	1.05	1.1	1.15	SVS_{NOM} – 25 mV	1.0 – 1.15	SVS_{NOM} + 25 mV	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13		3.47	3.13		3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13		3.47	3.13		3.47	V
V_{IH}[3]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0		3.6	2.0		3.6	V
V_{IL}[3]	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		0.8	–0.3		0.8	V
V_{IH_CLKIN}[4]	High Level Input Voltage @ V_{DD_EXT} = Max	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		+0.8	–0.3		+0.8	V
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C

[1] Specifications subject to change without notice.

[2] SVS_{NOM} refers to the nominal SVS voltage which is set between 1.0 V and 1.15 V at the factory for each individual device. Only the unique SVS_{NOM} value in each chip may be used for 401 MHz to 450 MHz operation of that chip. This spec lists the possible range of the SVS_{NOM} values for all devices. The initial VDD_INT voltage at power on is 1.1 V nominal and it transitions to SVS programmed voltage as outlined in Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357).

[3] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[4] Applies to input pins CLKIN, WDT_CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	300 MHz / 350 MHz / 400 MHz / 450 MHz Min	Typ	Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]			0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			200	µA
I_{OZHPD}[8]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			200	µA
I_{DD_INT}[9]	Supply Current (Internal)	f_{CCLK} > 0 MHz			Table 14 + Table 15 × ASF	mA
I_{DD_INT}	Supply Current (Internal)	V_{DDINT} = 1.1 V, ASF = 1, T_J = 25°C		410 / 450 / 500 / 550		mA
C_{IN}[10, 11]	Input Capacitance	T_{CASE} = 25°C			5	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23–0, DATA15–0, $\overline{AMI\_RD}$, $\overline{AMI\_WR}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{EMU}$, TDO, $\overline{RESETOUT}$ MLBSIG, MLBDAT, MLBDO, MLBSO, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDDQM, $\overline{MS0\text{-}1}$.
[3] See Output Drive Currents on Page 55 for typical drive current capabilities.
[4] Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pin: TDO.
[7] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{EMU}$.
[8] Applies to three-statable pin with pull-down: SDCLK.
[9] See Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for further information.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

Total Power Dissipation

The information in this section should be augmented with the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348).

Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature (T_J) and core voltage (V_{DD_INT}).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13).

     Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

Table 13. Activity Scaling Factors (ASF)[1]

Activity	Scaling Factor (ASF)
Idle	0.29
Low	0.53
Medium Low	0.61
Medium High	0.77
Peak Typical (50:50)[2]	0.85
Peak Typical (60:40)[2]	0.93
Peak Typical (70:30)[2]	1.00
High Typical	1.16
High	1.25
Peak	1.31

[1] See the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for more information on the explanation of the power vectors specific to the ASF table.

[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]

	V_{DD_INT} (V)								
T_J (°C)	0.975 V	1.0 V	1.025 V	1.05 V	1.075 V	1.10 V	1.125 V	1.15 V	1.175 V
–45	68	77	86	96	107	118	131	144	159
–35	74	83	92	103	114	126	140	154	170
–25	82	92	101	113	125	138	153	168	185
–15	94	104	115	127	140	155	171	187	205
–5	109	121	133	147	161	177	194	212	233
+5	129	142	156	171	188	206	225	245	268
+15	152	168	183	201	219	240	261	285	309
+25	182	199	216	237	257	280	305	331	360
+35	217	237	256	279	303	329	358	388	420
+45	259	282	305	331	359	389	421	455	492
+55	309	334	361	391	423	458	495	533	576
+65	369	398	429	464	500	539	582	626	675
+75	437	471	506	547	588	633	682	731	789
+85	519	559	599	645	693	746	802	860	926
+95	615	662	707	761	816	877	942	1007	1083
+105	727	779	833	897	958	1026	1103	1179	1266
+115	853	914	975	1047	1119	1198	1285	1372	1473
+125	997	1067	1138	1219	1305	1397	1498	1601	1716

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 43 on Page 55 for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, the processor core, and the serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 4). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

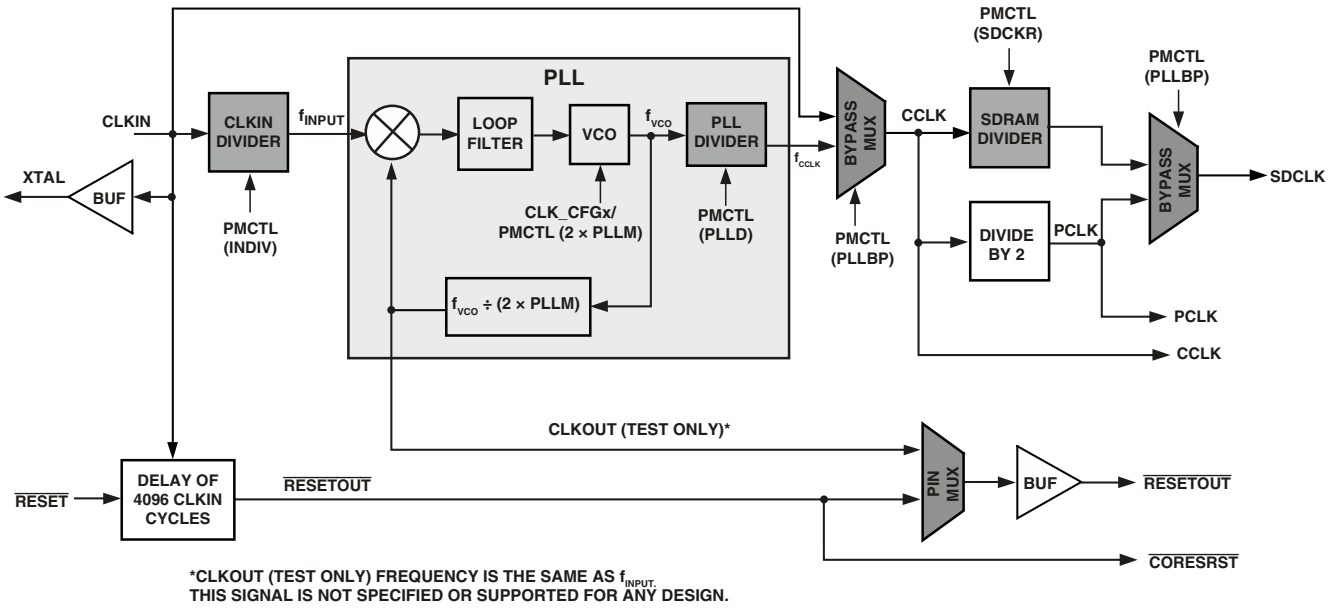

Figure 4. Core Clock and System Clock Relationship to CLKIN

Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 20.

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in Table 20 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 20 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$
$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} = is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 18. All of the timing specifications for the ADSP-2148x peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information.

Table 18. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}
t_{SDCLK}	SDRAM Clock Period = (t_{CCLK}) × SDCKR

Figure 4 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the hardware reference.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 19. While no specific power-up sequencing is required between V_{DD_EXT} and V_{DD_INT}, there are some considerations that system designs should take into account.

- No power supply should be powered up for an extended period of time (> 200 ms) before another supply starts to ramp up.
- If the V_{DD_INT} power supply comes up after V_{DD_EXT}, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the V_{DD_INT} rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the V_{DD_INT} power supply comes up after V_{DD_EXT}, a leakage current of the order of three-state leakage current pull-up, pull-down may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DD_INT} rail has powered up.

Table 19. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_EXT} or V_{DD_INT} On	0		ms
$t_{IVDDEVDD}$	V_{DD_INT} On Before V_{DD_EXT}	–200	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DD_INT} and V_{DD_EXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristic				
$t_{CORERST}$[4, 5]	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	4096 × t_{CK} + 2 × t_{CCLK}		

[1] Valid V_{DD_INT} and V_{DD_EXT} assumes that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 21. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

Watchdog Timer Timing

Table 27. Watchdog Timer Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{WDTCLKPER}$		100	1000	ns
Switching Characteristics				
t_{RST}	WDT Clock Rising Edge to Watchdog Timer $\overline{\text{RESET}}$ Falling Edge	3	6.4	ns
t_{RSTPW}	Reset Pulse Width	$64 \times t_{WDTCLKPER}$		ns

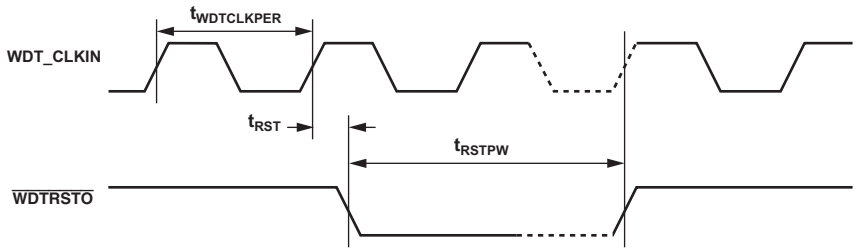

Figure 14. Watchdog Timer Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 28. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

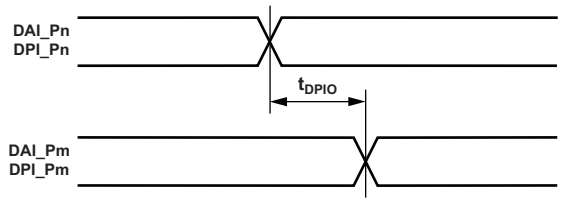

Figure 15. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 29. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the "Precision Clock Generators" chapter in the hardware reference.

[1] Normal mode of operation.

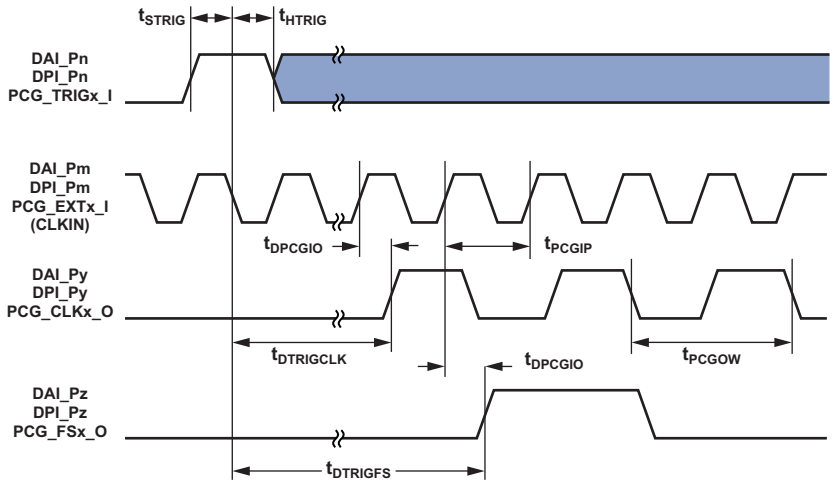

Figure 16. Precision Clock Generator (Direct Pin Routing)

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		W + t_{SDCLK} –5.4	ns
t_{DRLD}[1, 3]	$\overline{\text{AMI\_RD}}$ Low to Data Valid		W – 3.2	ns
t_{SDS}	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.5		ns
t_{HDRH}[4, 5]	Data Hold from $\overline{\text{AMI\_RD}}$ High	0		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address, Selects		t_{SDCLK} –9.5 + W	ns
t_{DSAK}[4]	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low		W – 7	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RHC + 0.20		ns
t_{DARL}[2]	Address Selects to $\overline{\text{AMI\_RD}}$ Low	t_{SDCLK} – 3.8		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	HI + t_{SDCLK} – 1		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
Where PREDIS = 0
HI = RHC (if IC=0): Read to Read from same bank
HI = RHC + t_{SDCLK} (if IC>0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{SDCLK}): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × tSDCLK

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 55 for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).

Serial Ports

In slave transmitter mode and master receiver mode, the maximum serial port frequency is $f_{PCLK}/8$. In master transmitter mode and slave receiver mode, the maximum serial port clock frequency is $f_{PCLK}/4$. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold; 2) data delay and data setup and hold; and 3) SCLK width.

Serial port signals (SCLK, frame sync, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		10.25	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 35. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–2		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Sample Rate Converter—Serial Input Port

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 41 are valid at the DAI_P20–1 pins.

Table 41. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

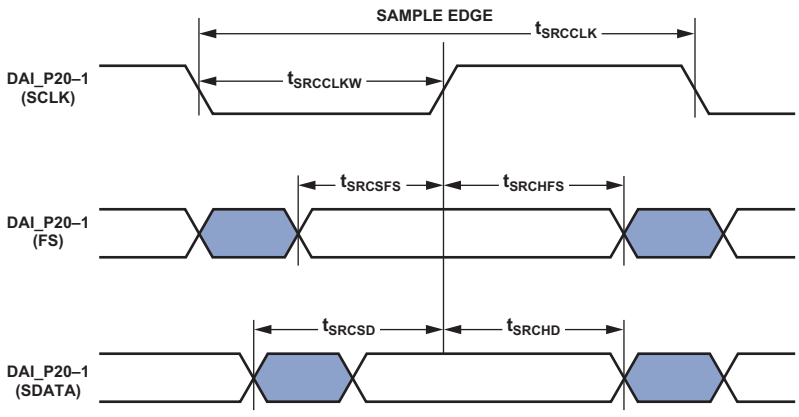

Figure 27. ASRC Serial Input Port Timing

Media Local Bus

All the numbers given are applicable for all speed modes (1024 FS, 512 FS and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin), unless otherwise specified. Please refer to the MediaLB specification document revision 3.0 for more details.

Table 52. MLB Interface, 3-Pin Specifications

Parameter		Min	Typ	Max	Unit
3-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024 FS		20.3		ns
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024 FS	6.1			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	1024 FS	9.3			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024 FS			0.7	nspp
	512 FS/256			2.0	nspp
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	2			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-state	0		15	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024 FS	2			ns
	512 FS/256	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024 FS			40	pf
	512 FS/256			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] The board must be designed to ensure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

100-LQFP_EP LEAD ASSIGNMENT

Table 59. 100-Lead LQFP_EP Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
V_{DD_INT}	1	V_{DD_EXT}	26	DAI_P10	51	V_{DD_INT}	76
CLK_CFG1	2	DPI_P08	27	V_{DD_INT}	52	FLAG0	77
BOOT_CFG0	3	DPI_P07	28	V_{DD_EXT}	53	V_{DD_INT}	78
V_{DD_EXT}	4	V_{DD_INT}	29	DAI_P20	54	V_{DD_INT}	79
V_{DD_INT}	5	DPI_P09	30	V_{DD_INT}	55	FLAG1	80
BOOT_CFG1	6	DPI_P10	31	DAI_P08	56	FLAG2	81
GND	7	DPI_P11	32	DAI_P04	57	FLAG3	82
NC	8	DPI_P12	33	DAI_P14	58	MLBCLK	83
NC	9	DPI_P13	34	DAI_P18	59	MLBDAT	84
CLK_CFG0	10	DAI_P03	35	DAI_P17	60	MLBDO	85
V_{DD_INT}	11	DPI_P14	36	DAI_P16	61	V_{DD_EXT}	86
CLKIN	12	V_{DD_INT}	37	DAI_P15	62	MLBSIG	87
XTAL	13	V_{DD_INT}	38	DAI_P12	63	V_{DD_INT}	88
V_{DD_EXT}	14	V_{DD_INT}	39	V_{DD_INT}	64	MLBSO	89
V_{DD_INT}	15	DAI_P13	40	DAI_P11	65	$\overline{TRST}$	90
V_{DD_INT}	16	DAI_P07	41	V_{DD_INT}	66	$\overline{EMU}$	91
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	17	DAI_P19	42	V_{DD_INT}	67	TDO	92
V_{DD_INT}	18	DAI_P01	43	GND	68	V_{DD_EXT}	93
DPI_P01	19	DAI_P02	44	THD_M	69	V_{DD_INT}	94
DPI_P02	20	V_{DD_INT}	45	THD_P	70	TDI	95
DPI_P03	21	V_{DD_EXT}	46	V_{DD_THD}	71	TCK	96
V_{DD_INT}	22	V_{DD_INT}	47	V_{DD_INT}	72	V_{DD_INT}	97
DPI_P05	23	DAI_P06	48	V_{DD_INT}	73	$\overline{RESET}$	98
DPI_P04	24	DAI_P05	49	V_{DD_INT}	74	TMS	99
DPI_P06	25	DAI_P09	50	V_{DD_INT}	75	V_{DD_INT}	100
						GND	101*

MLB pins (pins 83, 84, 85, 87, and 89) are available for automotive models only. For non-automotive models, these pins should be connected to ground (GND).

* Pin no. 101 (exposed pad) is the GND supply (see Figure 48 and Figure 49) for the processor; this pad must be **robustly** connected to GND.

Figure 48 shows the top view of the 100-lead LQFP_EP lead configuration. Figure 49 shows the bottom view of the 100-lead LQFP_EP lead configuration.

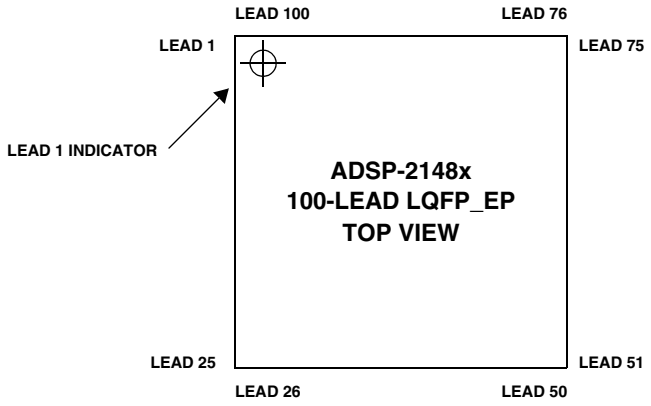

Figure 48. 100-Lead LQFP_EP Lead Configuration (Top View)

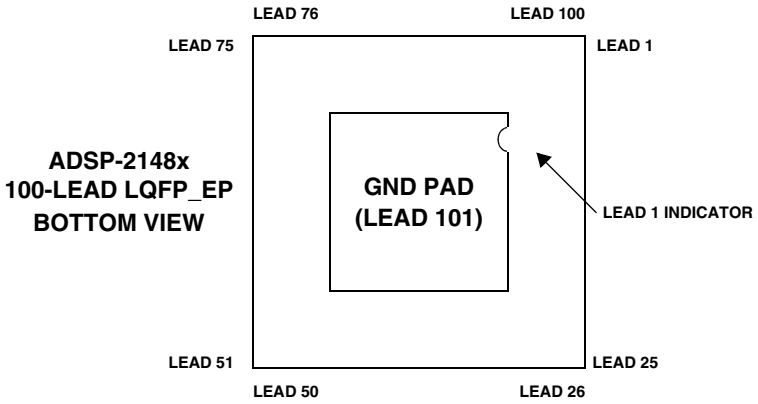

Figure 49. 100-Lead LQFP_EP Lead Configuration (Bottom View)

Figure 50 shows the top view of the 176-lead LQFP_EP lead configuration. Figure 51 shows the bottom view of the 176-lead LQFP_EP lead configuration.

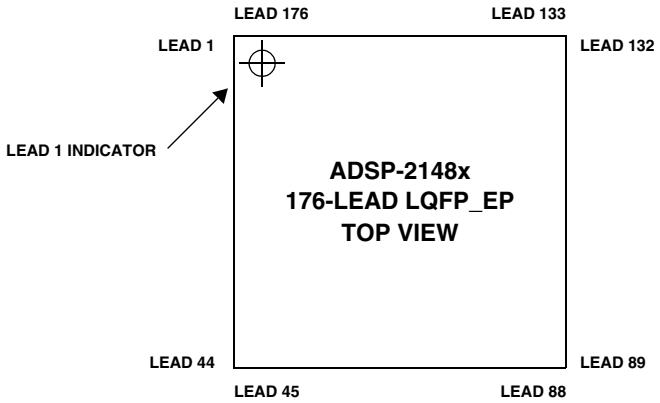

Figure 50. 176-Lead LQFP_EP Lead Configuration (Top View)

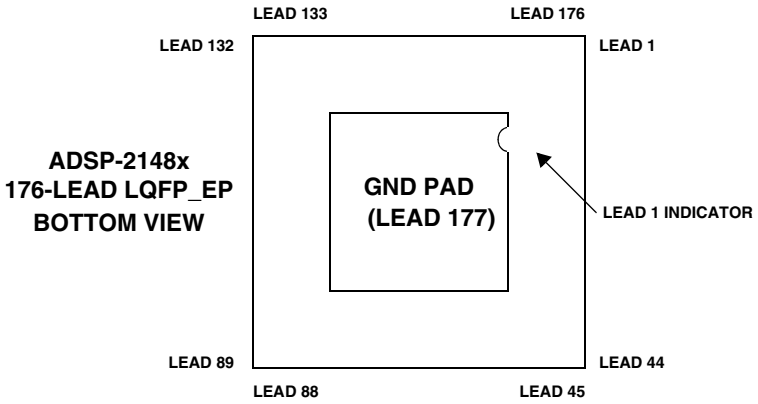

Figure 51. 176-Lead LQFP_EP Lead Configuration (Bottom View)

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21487KSWZ-2B	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-2BB	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3B	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3BB	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4B	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4BB	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5B	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5BB	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP21487KSWZ5BBRL	5	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3A		–40°C to +85°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A		0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A1	6	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3B		0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3B		–40°C to +85°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4A		0°C to +70°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488BSWZ-4A		–40°C to +85°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-4B		0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-4B		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4B1	6	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-3A		0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-3A		–40°C to +85°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-3B		0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-3B		–40°C to +85°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-4A		0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-4A		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-4B		0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-4B		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-5B	4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification, which is the only temperature specification.

[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

[4] See Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for operating ADSP-2148x processors at 450 MHz.

[5] RL = Tape and Reel.

[6] This product contains a –140 dB sample rate converter.