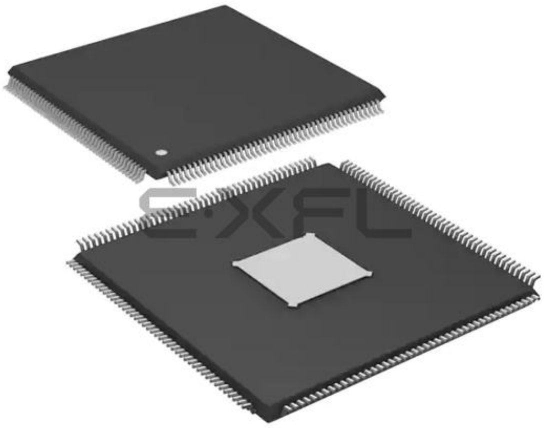

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	EBI/EMI, DAI, I²C, SPI, SPORT, UART/USART
Clock Rate	350MHz
Non-Volatile Memory	External
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21488bswz-3b

GENERAL DESCRIPTION

The ADSP-2148x SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x, ADSP-2147x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2148x processors are 32-bit/40-bit floating point processors optimized for high performance audio applications with large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1 shows performance benchmarks for the ADSP-2148x processors. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks

Benchmark Algorithm	Speed (at 400 MHz)	Speed (at 450 MHz)
1024 Point Complex FFT (Radix 4, with Reversal)	23 μs	20.44 μs
FIR Filter (per Tap)[1]	1.25 ns	1.1 ns
IIR Filter (per Biquad)[1]	5 ns	4.43 ns
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	11.25 ns	10.0 ns
[4 × 4] × [4 × 1]	20 ns	17.78 ns
Divide (y/x)	7.5 ns	6.67 ns
Inverse Square Root	11.25 ns	10.0 ns

[1] Assumes two files in multichannel SIMD mode

Table 2. ADSP-2148x Family Features

Feature	ADSP-21483	ADSP-21486	ADSP-21487	ADSP-21488	ADSP-21489
Maximum Instruction Rate	400 MHz	400 MHz	450 MHz	400 MHz	450 MHz
RAM	3 Mbits	5 Mbits		2/3 Mbits[1]	5 Mbits
ROM	4 Mbits			No	
Audio Decoders in ROM[2]	Yes			No	
Pulse-Width Modulation	4 Units (3 Units on 100-Lead Packages)				
DTCP Hardware Accelerator	Contact Analog Devices				
External Port Interface (SDRAM, AMI)[3]	Yes (16-bit)	AMI Only	Yes (16-bit)		
Serial Ports	8				
Direct DMA from SPORTs to External Port (External Memory)	Yes				
FIR, IIR, FFT Accelerator	Yes				
Watchdog Timer	Yes (176-Lead Package Only)				
MediaLB Interface	Automotive Models Only				
IDP/PDAP	Yes				
UART	1				
DAI (SRU)/DPI (SRU2)	Yes				
S/PDIF Transceiver	Yes				
SPI	Yes				
TWI	1				
SRC Performance[4]	–128 dB				
Thermal Diode	Yes				
VISA Support	Yes				
Package[3]	176-Lead LQFP EPAD 100-Lead LQFP EPAD		176-Lead LQFP EPAD	176-Lead LQFP EPAD 100-Lead LQFP EPAD[5]	

[1] See Ordering Guide on Page 66.
[2] ROM is factory programmed with latest multichannel audio decoding and post-processing algorithms from Dolby® Labs and DTS®. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.
[3] The 100-lead packages do not contain an external port. The SDRAM controller pins must be disabled when using this package. For more information, see Pin Function Descriptions on Page 14. The ADSP-21486 processor in the 176-lead package also does not contain a SDRAM controller. For more information, see 176-Lead LQFP_EP Lead Assignment on page 60.
[4] Some models have –140 dB performance. For more information, see Ordering Guide on page 66.
[5] Only available up to 400 MHz. See Ordering Guide on Page 66 for details.

subtract in both processing elements while branching and fetching up to four 32-bit values from memory, all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the ADSP-2148x supports new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The ADSP-21483 and the ADSP-21488 processors contain 3 Mbits of internal RAM (Table 3) and the ADSP-21486, ADSP-21487, and ADSP-21489 processors contain 5 Mbits of internal RAM (Table 4). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor.

Table 3. Internal Memory Space (3 MBits—ADSP-21483/ADSP-21488)[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 CFFF	Block 0 SRAM 0x0008 C000–0x0009 1554	Block 0 SRAM 0x0009 2000–0x0009 9FFF	Block 0 SRAM 0x0012 4000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 FFFF	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 CFFF	Block 1 SRAM 0x000A C000–0x000B 1554	Block 1 SRAM 0x000B 2000–0x000B 9FFF	Block 1 SRAM 0x0016 4000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0x000B FFFF	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000– 0x0006 FFFF	Reserved 0x000C 2AAA–0x000D FFFF	Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF	Reserved 0x000E 2AAA–0x000F FFFF	Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF

[1] Some ADSP-2148x processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 3 and Table 4 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an

- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

Non-SDRAM external memory address space is shown in Table 5.

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	6M	0x0020 0000–0x007F FFFF
Bank 1	8M	0x0400 0000–0x047F FFFF
Bank 2	8M	0x0800 0000–0x087F FFFF
Bank 3	8M	0x0C00 0000–0x0C7F FFFF

External Port

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 176-lead LQFP, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and banks 1, 2, and 3 occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices at speeds up to f_{SDCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 4M bytes and 256M bytes of memory. SDRAM external memory address space is shown in Table 6. NOTE: this feature is not available on the ADSP-21486 model.

Table 6. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on the SDRAM and AMI interfaces.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This removes the need to explicitly access the complimentary registers when the data is in external SDRAM memory.

VISA and ISA Access to External Memory

The SDRAM controller on the ADSP-2148x processors supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. Table 7 shows the address ranges for instruction fetch in each mode.

Table 7. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000–0x005F FFFF
VISA (SW)	10M	0x0060 0000–0x00FF FFFF

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

Details on power consumption and Static and Dynamic current consumption can be found at Total Power Dissipation on Page 20. Also see Operating Conditions on Page 18 for more information.

The following are SVS features.

- SVS is applicable only to 450 MHz models (not applicable to 400 MHz or lower frequency models).
- Each individual SVS device includes a register (SVS_DAT) containing the unique SVS voltage set at the factory, known as SVS_{NOM}.
- The SVS_{NOM} value is the intended set voltage for the V_{DD_INT} voltage regulator.
- No dedicated pins are required for SVS. The TWI serial bus is used to communicate SVS_{NOM} to the voltage regulator.
- Analog Devices recommends a specific voltage regulator design and initialization code sequence that optimizes the power-up sequence.

  The Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) contains the details of the regulator design and the initialization requirements.
- Any differences from the Analog Devices recommended programmable regulator design must be reviewed by Analog Devices to ensure that it meets the voltage accuracy and range requirements.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2148x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

CrossCore Embedded Studio is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the Product Download area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see Analog Devices JTAG Emulation Technical Reference (EE-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2148x architecture and functionality. For detailed information on the ADSP-2148x family core architecture and instruction set, refer to the programming reference manual.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
MLBCLK[1]	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS=48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT[1]	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG[1]	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO[1]	O/T	High-Z	**Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
MLBSO[1]	O/T	High-Z	**Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{\text{EMU}}$	O (O/D, ipu)	High-Z	**Emulation Status.** Must be connected to the ADSP-2148x Analog Devices DSP Tools product line of JTAG emulators target board connector only.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

Total Power Dissipation

The information in this section should be augmented with the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348).

Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature (T_J) and core voltage (V_{DD_INT}).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13).

     Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

Table 13. Activity Scaling Factors (ASF)[1]

Activity	Scaling Factor (ASF)
Idle	0.29
Low	0.53
Medium Low	0.61
Medium High	0.77
Peak Typical (50:50)[2]	0.85
Peak Typical (60:40)[2]	0.93
Peak Typical (70:30)[2]	1.00
High Typical	1.16
High	1.25
Peak	1.31

[1] See the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for more information on the explanation of the power vectors specific to the ASF table.

[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]

	V_{DD_INT} (V)								
T_J (°C)	0.975 V	1.0 V	1.025 V	1.05 V	1.075 V	1.10 V	1.125 V	1.15 V	1.175 V
–45	68	77	86	96	107	118	131	144	159
–35	74	83	92	103	114	126	140	154	170
–25	82	92	101	113	125	138	153	168	185
–15	94	104	115	127	140	155	171	187	205
–5	109	121	133	147	161	177	194	212	233
+5	129	142	156	171	188	206	225	245	268
+15	152	168	183	201	219	240	261	285	309
+25	182	199	216	237	257	280	305	331	360
+35	217	237	256	279	303	329	358	388	420
+45	259	282	305	331	359	389	421	455	492
+55	309	334	361	391	423	458	495	533	576
+65	369	398	429	464	500	539	582	626	675
+75	437	471	506	547	588	633	682	731	789
+85	519	559	599	645	693	746	802	860	926
+95	615	662	707	761	816	877	942	1007	1083
+105	727	779	833	897	958	1026	1103	1179	1266
+115	853	914	975	1047	1119	1198	1285	1372	1473
+125	997	1067	1138	1219	1305	1397	1498	1601	1716

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 43 on Page 55 for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, the processor core, and the serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 4). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

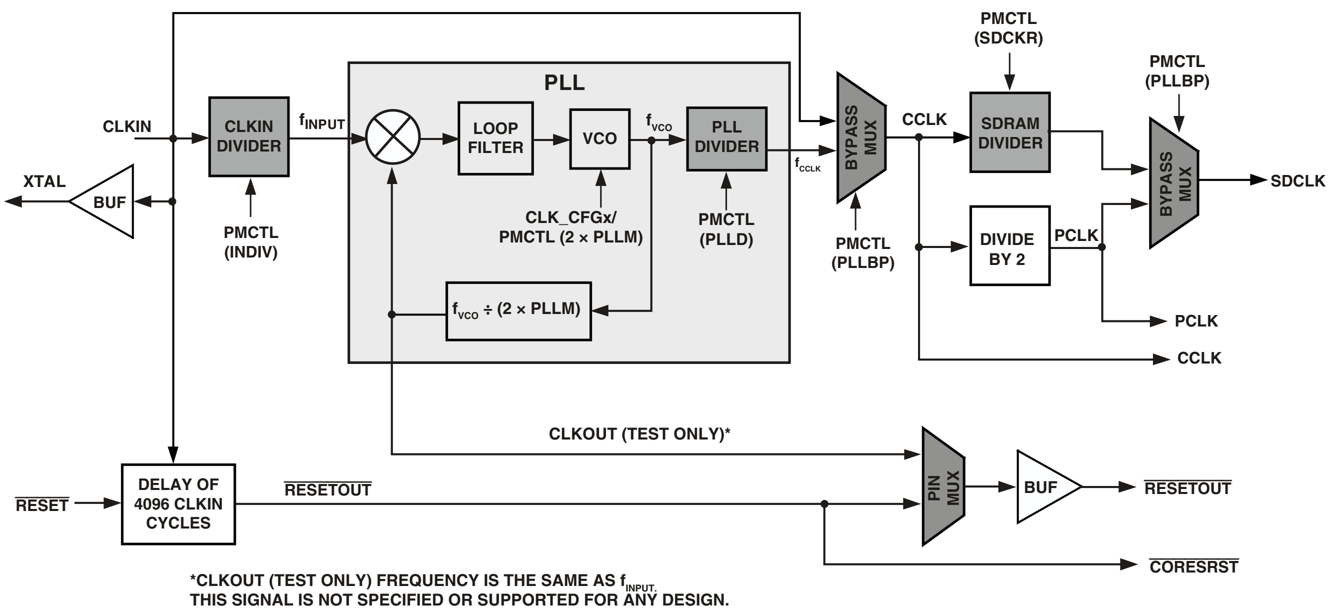

Figure 4. Core Clock and System Clock Relationship to CLKIN

Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 20.

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in Table 20 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 20 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$
$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} = is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled or

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

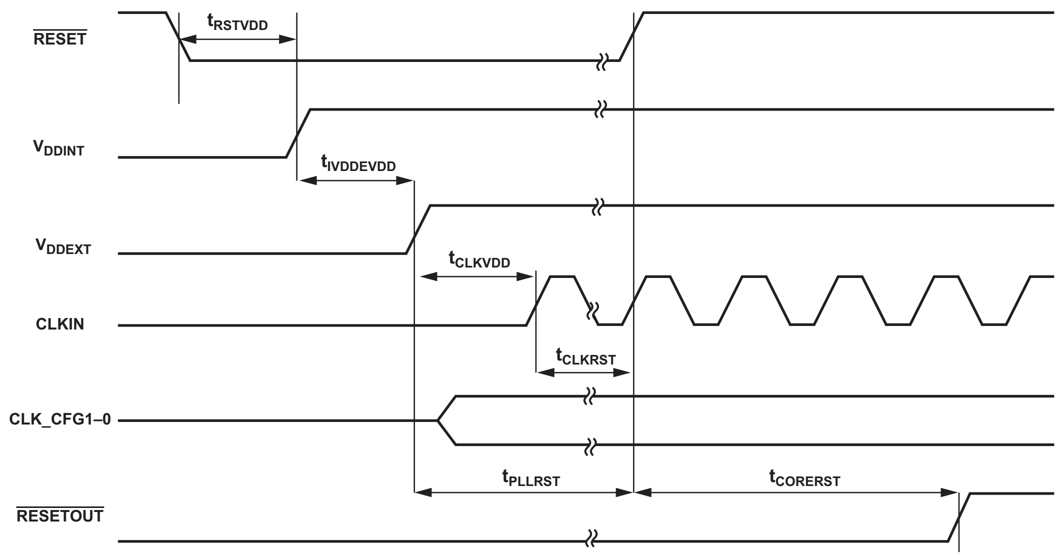

Figure 5. Power-Up Sequencing

Clock Input

Table 20. Clock Input

Parameter		300 MHz Min	300 MHz Max	350 MHz Min	350 MHz Max	400 MHz Min	400 MHz Max	450 MHz Min	450 MHz Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	26.66[1]	100[2]	22.8[1]	100[2]	20[1]	100[2]	17.75[1]	100[2]	ns
t_{CKL}	CLKIN Width Low	13	45	11	45	10	45	8.875	45	ns
t_{CKH}	CLKIN Width High	13	45	11	45	10	45	8.875	45	ns
t_{CKRF}[3]	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns
t_{CCLK}[4]	CCLK Period	3.33	10	2.85	10	2.5	10	2.22	10	ns
f_{VCO}[5]	VCO Frequency	200	800	200	800	200	800	200	900	MHz
t_{CKJ}[6, 7]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	–250	+250	ps

[1] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLK_CFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Guaranteed by simulation but not tested on silicon.
[4] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[5] See Figure 4 on Page 22 for VCO diagram.
[6] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[7] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

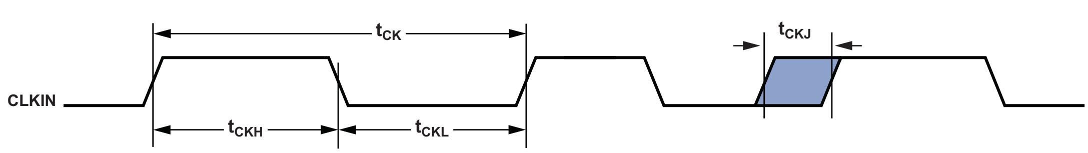

Figure 6. Clock Input

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, AMI_RD, AMI_WR, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		$W + t_{SDCLK} - 5.4$	ns
t_{DRLD}[1, 3]	AMI_RD Low to Data Valid		$W - 3.2$	ns
t_{SDS}	Data Setup to AMI_RD High	2.5		ns
t_{HDRH}[4, 5]	Data Hold from AMI_RD High	0		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address, Selects		$t_{SDCLK} - 9.5 + W$	ns
t_{DSAK}[4]	AMI_ACK Delay from AMI_RD Low		$W - 7$	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After AMI_RD High	$RHC + 0.20$		ns
t_{DARL}[2]	Address Selects to AMI_RD Low	$t_{SDCLK} - 3.8$		ns
t_{RW}	AMI_RD Pulse Width	$W - 1.4$		ns
t_{RWR}	AMI_RD High to AMI_RD Low	$HI + t_{SDCLK} - 1$		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.

RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}

Where PREDIS = 0

HI = RHC (if IC=0): Read to Read from same bank

HI = RHC + t_{SDCLK} (if IC>0): Read to Read from same bank

HI = RHC + IC: Read to Read from different bank

HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank

Where PREDIS = 1

HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank

HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank

HI = RHC + Max (IC, (3 × t_{SDCLK}): Read to Read from different bank

IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}

H = (number of hold cycles specified in AMICTLx register) × tSDCLK

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.

[2] The falling edge of MSx, is referenced.

[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.

[4] Note that timing for AMI_ACK, ADDR, DATA, AMI_RD, AMI_WR, and strobe timing parameters only apply to asynchronous access mode.

[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 55 for the calculation of hold times given capacitive and dc loads.

[6] AMI_ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPORTx-_TDV_O is asserted for communication with external devices.

Table 38. Serial Ports—TDV (Transmit Data Valid)

Parameter		Min	Max	Unit
Switching Characteristics[1]				
t_{DRDVEN}	TDV Assertion Delay from Drive Edge of External Clock	3		ns
t_{DFDVEN}	TDV Deassertion Delay from Drive Edge of External Clock		8	ns
t_{DRDVIN}	TDV Assertion Delay from Drive Edge of Internal Clock	–1		ns
t_{DFDVIN}	TDV Deassertion Delay from Drive Edge of Internal Clock		2	ns

[1] Referenced to drive edge.

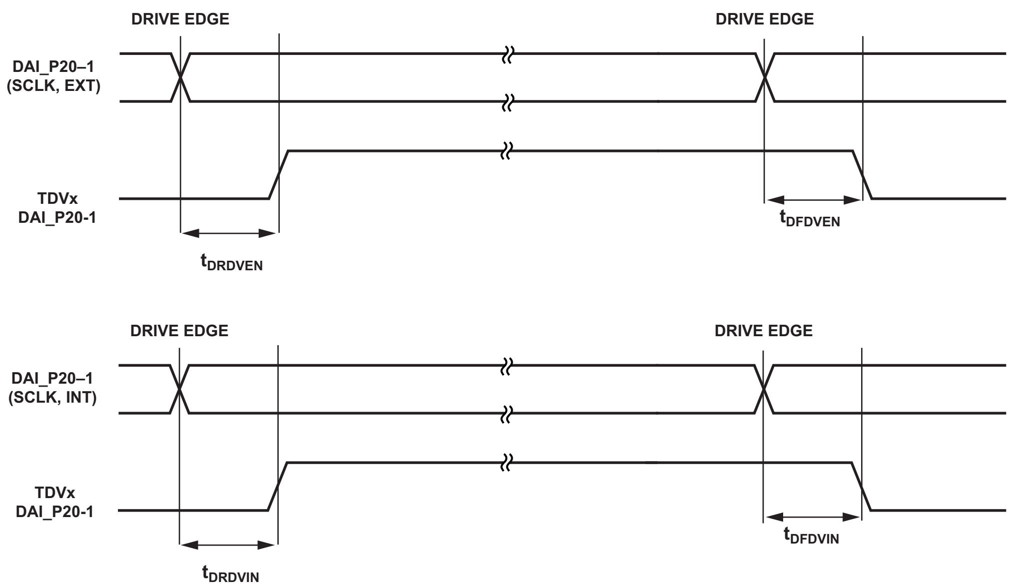

Figure 24. Serial Ports—TDM Internal and External Clock

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

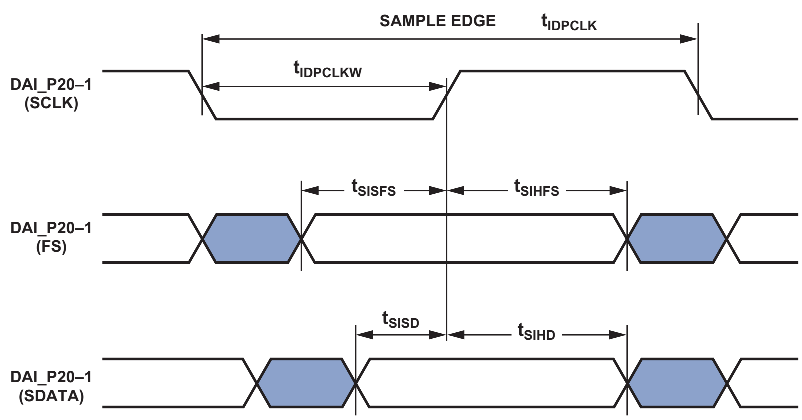

Figure 25. IDP Master Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the ADDR23–8/DPI_14–1 pins are configured as PWM.

Table 43. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

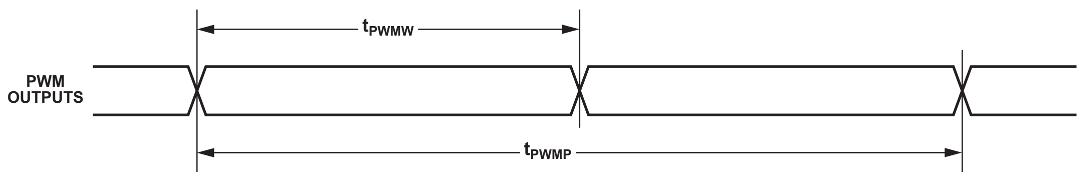

Figure 29. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I^2S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 30 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Table 44. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	Frame Sync to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

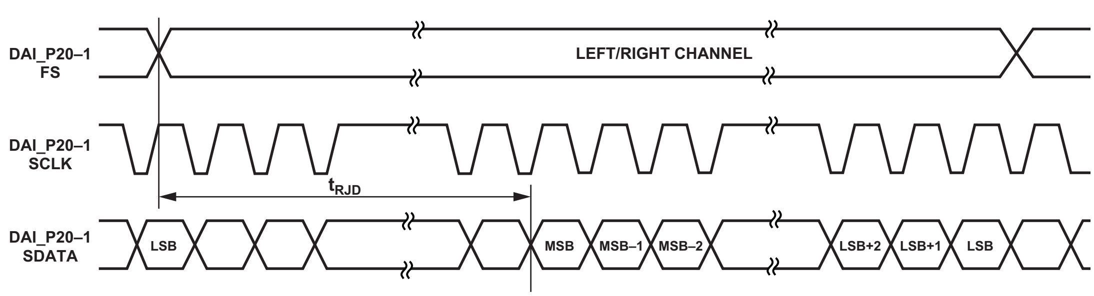

Figure 30. Right-Justified Mode

Media Local Bus

All the numbers given are applicable for all speed modes (1024 FS, 512 FS and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin), unless otherwise specified. Please refer to the MediaLB specification document revision 3.0 for more details.

Table 52. MLB Interface, 3-Pin Specifications

Parameter		Min	Typ	Max	Unit
3-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024 FS		20.3		ns
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024 FS	6.1			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	1024 FS	9.3			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024 FS			0.7	nspp
	512 FS/256			2.0	nspp
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	2			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-state	0		15	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024 FS	2			ns
	512 FS/256	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024 FS			40	pf
	512 FS/256			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] The board must be designed to ensure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

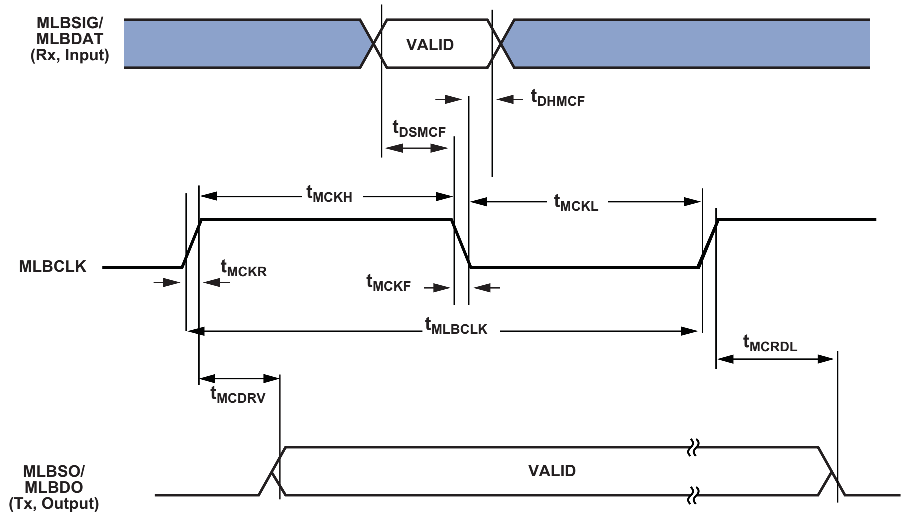

Figure 38. MLB Timing (5-Pin Interface)

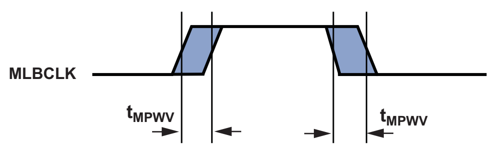

Figure 39. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the hardware reference.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the hardware reference.

Note that the thermal characteristics values provided in Table 56 and Table 57 are modeled values.

Table 56. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.8	°C/W
θ_{JMA}	Airflow = 1 m/s	15.4	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.24	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.37	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.51	°C/W

Table 57. Thermal Characteristics for 176-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	16.9	°C/W
θ_{JMA}	Airflow = 1 m/s	14.6	°C/W
θ_{JMA}	Airflow = 2 m/s	13.8	°C/W
θ_{JC}		2.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.21	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.32	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.41	°C/W

Thermal Diode

The ADSP-2148x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times \ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann's constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

Table 58 contains the thermal diode specifications using the transistor model.

Table 58. Thermal Diode Parameters – Transistor Model[1]

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}[2]	Forward Bias Current	10		300	μA
I_E	Emitter Current	10		300	μA
n_Q[3, 4]	Transistor Ideality	1.012	1.015	1.017	
R_T[3, 5]	Series Resistance	0.12	0.2	0.28	Ω

[1] See Engineer-to-Engineer Note Using the On-Chip Thermal Diode on Analog Devices Processors (EE-346).
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
[5] The series resistance (R_T) can be used for more accurate readings as needed.

Figure 48 shows the top view of the 100-lead LQFP_EP lead configuration. Figure 49 shows the bottom view of the 100-lead LQFP_EP lead configuration.

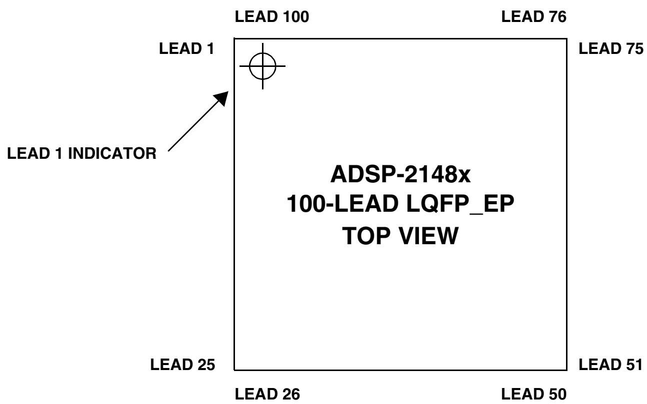

Figure 48. 100-Lead LQFP_EP Lead Configuration (Top View)

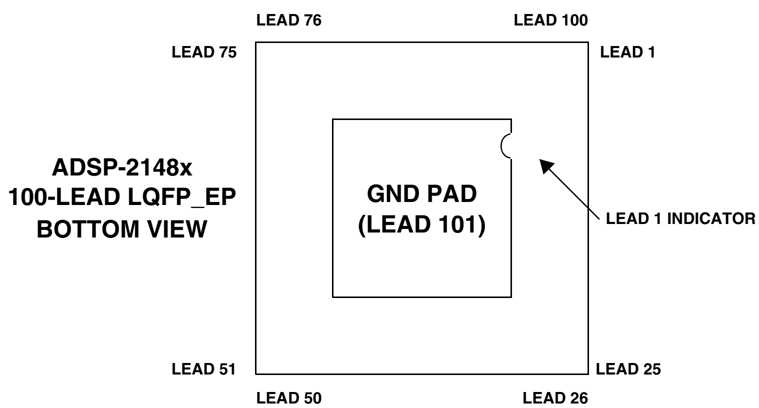

Figure 49. 100-Lead LQFP_EP Lead Configuration (Bottom View)

176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
NC	1	V_{DD_EXT}	45	DAI_P10	89	V_{DD_INT}	133
MS0	2	DPI_P08	46	V_{DD_INT}	90	FLAG0	134
NC	3	DPI_P07	47	V_{DD_EXT}	91	FLAG1	135
V_{DD_INT}	4	V_{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V_{DD_INT}	93	GND	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	GND	139
V_{DD_EXT}	8	DPI_P12	52	DAI_P04	96	GND	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V_{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	GND	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V_{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	TRST	144
ADDR5	13	V_{DD_EXT}	57	DAI_P15	101	GND	145
BOOT_CFG1	14	NC	58	V_{DD_INT}	102	EMU	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V_{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V_{DD_INT}	105	DATA2	149
NC	18	V_{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V_{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V_{DD_INT}	65	GND	109	V_{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V_{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V_{DD_INT}	68	V_{DD_THD}	112	V_{DD_INT}	156
XTAL	25	NC	69	V_{DD_INT}	113	DATA7	157
ADDR10	26	WDTRSTO	70	V_{DD_INT}	114	TDI	158
NC	27	NC	71	MS1	115	NC	159*
V_{DD_EXT}	28	V_{DD_EXT}	72	V_{DD_INT}	116	V_{DD_EXT}	160
V_{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V_{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V_{DD_INT}	34	V_{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V_{DD_INT}	123	DATA14	167
RESETOUT/RUNRSTIN	36	NC	80	ADDR20	124	DATA13	168
V_{DD_INT}	37	NC	81	ADDR19	125	V_{DD_INT}	169
DPI_P01	38	NC	82	V_{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	NC	171
DPI_P03	40	V_{DD_EXT}	84	ADDR15	128	NC	172
V_{DD_INT}	41	V_{DD_INT}	85	V_{DD_INT}	129	RESET	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	AMI_WR	131	NC	175
DPI_P06	44	DAI_P09	88	AMI_RD	132	V_{DD_INT}	176
						GND	177**

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21487KSWZ-2B	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-2BB	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3B	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3BB	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4B	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4BB	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5B	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5BB	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP21487KSWZ5BBRL	5	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3A		–40°C to +85°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A		0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A1	6	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3B		0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3B		–40°C to +85°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4A		0°C to +70°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488BSWZ-4A		–40°C to +85°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-4B		0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-4B		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4B1	6	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-3A		0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-3A		–40°C to +85°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-3B		0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-3B		–40°C to +85°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-4A		0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-4A		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-4B		0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-4B		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-5B	4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z = RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification, which is the only temperature specification.
[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.
[4] See Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for operating ADSP-2148x processors at 450 MHz.
[5] RL = Tape and Reel.
[6] This product contains a –140 dB sample rate converter.

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