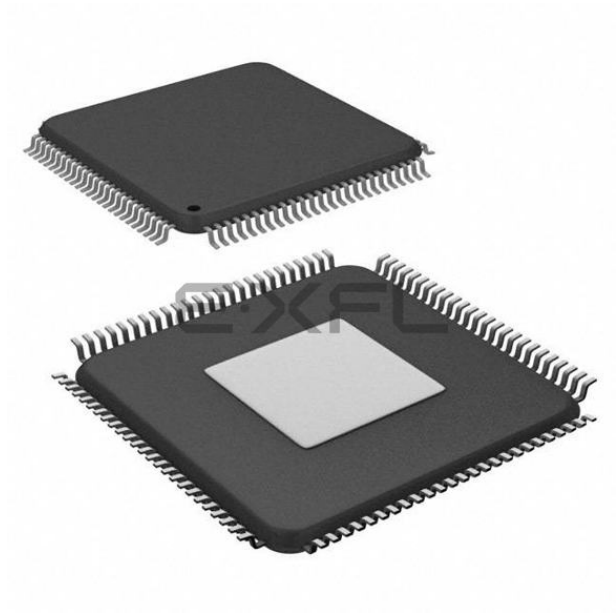

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Floating Point |
| Interface | EBI/EMI, DAI, I²C, SPI, SPORT, UART/USART |
| Clock Rate | 400MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 3Mbit |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.10V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | 100-LQFP-EP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-21488bswz-4a |

**Table 11. Pin Descriptions (Continued)**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| MLBCLK[1] | I | | **Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS=48 kHz. When the MLB controller is not used, this pin should be grounded. |
| MLBDAT[1] | I/O/T in 3 pin mode. I in 5 pin mode. | High-Z | **Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded. |
| MLBSIG[1] | I/O/T in 3 pin mode. I in 5 pin mode | High-Z | **Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded. |
| MLBDO[1] | O/T | High-Z | **Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground. |
| MLBSO[1] | O/T | High-Z | **Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground. |
| TDI | I (ipu) | | **Test Data Input (JTAG).** Provides serial data for the boundary scan logic. |
| TDO | O/T | High-Z | **Test Data Output (JTAG).** Serial scan output of the boundary scan path. |
| TMS | I (ipu) | | **Test Mode Select (JTAG).** Used to control the test state machine. |
| TCK | I | | **Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device. |
| $\overline{\text{TRST}}$ | I (ipu) | | **Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. |
| $\overline{\text{EMU}}$ | O (O/D, ipu) | High-Z | **Emulation Status.** Must be connected to the ADSP-2148x Analog Devices DSP Tools product line of JTAG emulators target board connector only. |

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full $V_{DD\_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

### *Total Power Dissipation*

The information in this section should be augmented with the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348).

Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature ($T_J$) and core voltage ($V_{DD\_INT}$).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13).

     Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

**Table 13. Activity Scaling Factors (ASF)[1]**

| Activity | Scaling Factor (ASF) |
|---|---|
| Idle | 0.29 |
| Low | 0.53 |
| Medium Low | 0.61 |
| Medium High | 0.77 |
| Peak Typical (50:50)[2] | 0.85 |
| Peak Typical (60:40)[2] | 0.93 |
| Peak Typical (70:30)[2] | 1.00 |
| High Typical | 1.16 |
| High | 1.25 |
| Peak | 1.31 |

[1] See the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for more information on the explanation of the power vectors specific to the ASF table.

[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

**Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]**

| | $V_{DD\_INT}$ (V) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $T_J$ (°C) | 0.975 V | 1.0 V | 1.025 V | 1.05 V | 1.075 V | 1.10 V | 1.125 V | 1.15 V | 1.175 V |
| –45 | 68 | 77 | 86 | 96 | 107 | 118 | 131 | 144 | 159 |
| –35 | 74 | 83 | 92 | 103 | 114 | 126 | 140 | 154 | 170 |
| –25 | 82 | 92 | 101 | 113 | 125 | 138 | 153 | 168 | 185 |
| –15 | 94 | 104 | 115 | 127 | 140 | 155 | 171 | 187 | 205 |
| –5 | 109 | 121 | 133 | 147 | 161 | 177 | 194 | 212 | 233 |
| +5 | 129 | 142 | 156 | 171 | 188 | 206 | 225 | 245 | 268 |
| +15 | 152 | 168 | 183 | 201 | 219 | 240 | 261 | 285 | 309 |
| +25 | 182 | 199 | 216 | 237 | 257 | 280 | 305 | 331 | 360 |
| +35 | 217 | 237 | 256 | 279 | 303 | 329 | 358 | 388 | 420 |
| +45 | 259 | 282 | 305 | 331 | 359 | 389 | 421 | 455 | 492 |
| +55 | 309 | 334 | 361 | 391 | 423 | 458 | 495 | 533 | 576 |
| +65 | 369 | 398 | 429 | 464 | 500 | 539 | 582 | 626 | 675 |
| +75 | 437 | 471 | 506 | 547 | 588 | 633 | 682 | 731 | 789 |
| +85 | 519 | 559 | 599 | 645 | 693 | 746 | 802 | 860 | 926 |
| +95 | 615 | 662 | 707 | 761 | 816 | 877 | 942 | 1007 | 1083 |
| +105 | 727 | 779 | 833 | 897 | 958 | 1026 | 1103 | 1179 | 1266 |
| +115 | 853 | 914 | 975 | 1047 | 1119 | 1198 | 1285 | 1372 | 1473 |
| +125 | 997 | 1067 | 1138 | 1219 | 1305 | 1397 | 1498 | 1601 | 1716 |

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 18. All of the timing specifications for the ADSP-2148x peripherals are defined in relation to $t_{PCLK}$. See the peripheral specific section for each peripheral's timing information.

**Table 18. Clock Periods**

| Timing Requirements | Description |
|---|---|
| $t_{CK}$ | CLKIN Clock Period |
| $t_{CCLK}$ | Processor Core Clock Period |
| $t_{PCLK}$ | Peripheral Clock Period = 2 × $t_{CCLK}$ |
| $t_{SDCLK}$ | SDRAM Clock Period = ($t_{CCLK}$) × SDCKR |

Figure 4 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the hardware reference.

### *Power-Up Sequencing*

The timing requirements for processor startup are given in Table 19. While no specific power-up sequencing is required between $V_{DD\_EXT}$ and $V_{DD\_INT}$, there are some considerations that system designs should take into account.

- No power supply should be powered up for an extended period of time (> 200 ms) before another supply starts to ramp up.
- If the $V_{DD\_INT}$ power supply comes up after $V_{DD\_EXT}$, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the $V_{DD\_INT}$ rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the $V_{DD\_INT}$ power supply comes up after $V_{DD\_EXT}$, a leakage current of the order of three-state leakage current pull-up, pull-down may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the $V_{DD\_INT}$ rail has powered up.

**Table 19. Power Up Sequencing Timing Requirements (Processor Startup)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{RSTVDD}$ | $\overline{\text{RESET}}$ Low Before $V_{DD\_EXT}$ or $V_{DD\_INT}$ On | 0 | | ms |
| $t_{IVDDEVDD}$ | $V_{DD\_INT}$ On Before $V_{DD\_EXT}$ | –200 | +200 | ms |
| $t_{CLKVDD}$[1] | CLKIN Valid After $V_{DD\_INT}$ and $V_{DD\_EXT}$ Valid | 0 | 200 | ms |
| $t_{CLKRST}$ | CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted | 10[2] | | µs |
| $t_{PLLRST}$ | PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted | 20[3] | | µs |
| *Switching Characteristic* | | | | |
| $t_{CORERST}$[4, 5] | Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted | 4096 × $t_{CK}$ + 2 × $t_{CCLK}$ | | |

[1] Valid $V_{DD\_INT}$ and $V_{DD\_EXT}$ assumes that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on $t_{SRST}$ specification in Table 21. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

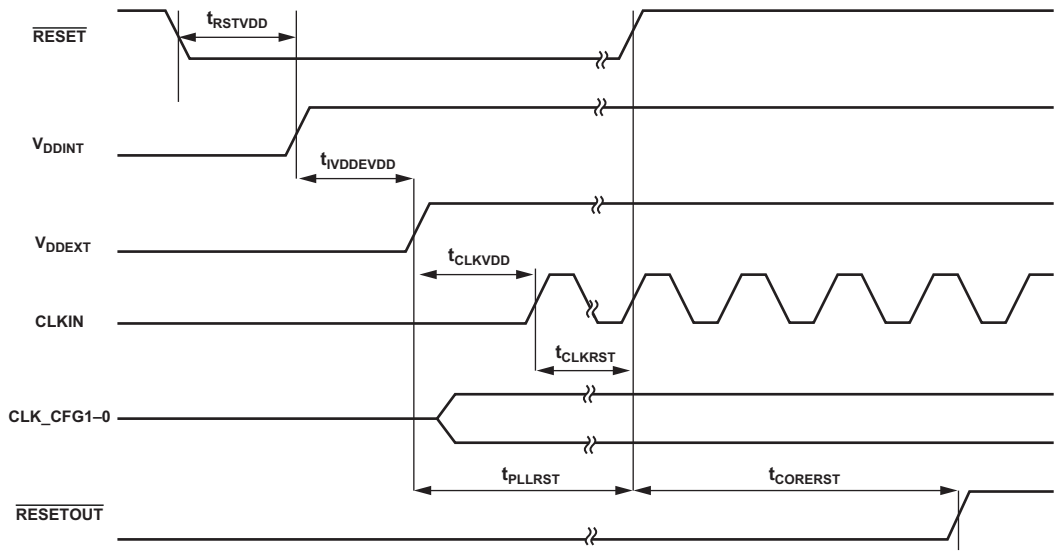


*Figure 5. Power-Up Sequencing*

### *Clock Input*

**Table 20. Clock Input**

| Parameter | | 300 MHz Min | 300 MHz Max | 350 MHz Min | 350 MHz Max | 400 MHz Min | 400 MHz Max | 450 MHz Min | 450 MHz Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | | | | | |
| $t_{CK}$ | CLKIN Period | 26.66[1] | 100[2] | 22.8[1] | 100[2] | 20[1] | 100[2] | 17.75[1] | 100[2] | ns |
| $t_{CKL}$ | CLKIN Width Low | 13 | 45 | 11 | 45 | 10 | 45 | 8.875 | 45 | ns |
| $t_{CKH}$ | CLKIN Width High | 13 | 45 | 11 | 45 | 10 | 45 | 8.875 | 45 | ns |
| $t_{CKRF}$[3] | CLKIN Rise/Fall (0.4 V to 2.0 V) | | 3 | | 3 | | 3 | | 3 | ns |
| $t_{CCLK}$[4] | CCLK Period | 3.33 | 10 | 2.85 | 10 | 2.5 | 10 | 2.22 | 10 | ns |
| $f_{VCO}$[5] | VCO Frequency | 200 | 800 | 200 | 800 | 200 | 800 | 200 | 900 | MHz |
| $t_{CKJ}$[6, 7] | CLKIN Jitter Tolerance | –250 | +250 | –250 | +250 | –250 | +250 | –250 | +250 | ps |

[1] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLK_CFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Guaranteed by simulation but not tested on silicon.
[4] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification $t_{CCLK}$.
[5] See Figure 4 on Page 22 for VCO diagram.
[6] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[7] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

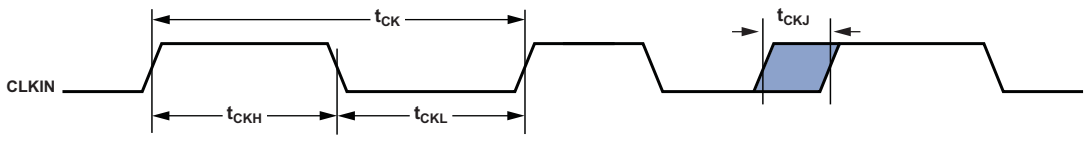


*Figure 6. Clock Input*

### *Precision Clock Generator (Direct Pin Routing)*

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

**Table 29. Precision Clock Generator (Direct Pin Routing)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{PCGIW}$ | Input Clock Period | $t_{PCLK} \times 4$ | | ns |
| $t_{STRIG}$ | PCG Trigger Setup Before Falling Edge of PCG Input Clock | 4.5 | | ns |
| $t_{HTRIG}$ | PCG Trigger Hold After Falling Edge of PCG Input Clock | 3 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DPCGIO}$ | PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock | 2.5 | 10 | ns |
| $t_{DTRIGCLK}$ | PCG Output Clock Delay After PCG Trigger | $2.5 + (2.5 \times t_{PCGIP})$ | $10 + (2.5 \times t_{PCGIP})$ | ns |
| $t_{DTRIGFS}$ | PCG Frame Sync Delay After PCG Trigger | $2.5 + ((2.5 + D - PH) \times t_{PCGIP})$ | $10 + ((2.5 + D - PH) \times t_{PCGIP})$ | ns |
| $t_{PCGOW}$[1] | Output Clock Period | $2 \times t_{PCGIP} - 1$ | | ns |

D = FSxDIV, PH = FSxPHASE. For more information, see the "Precision Clock Generators" chapter in the hardware reference.

[1] Normal mode of operation.

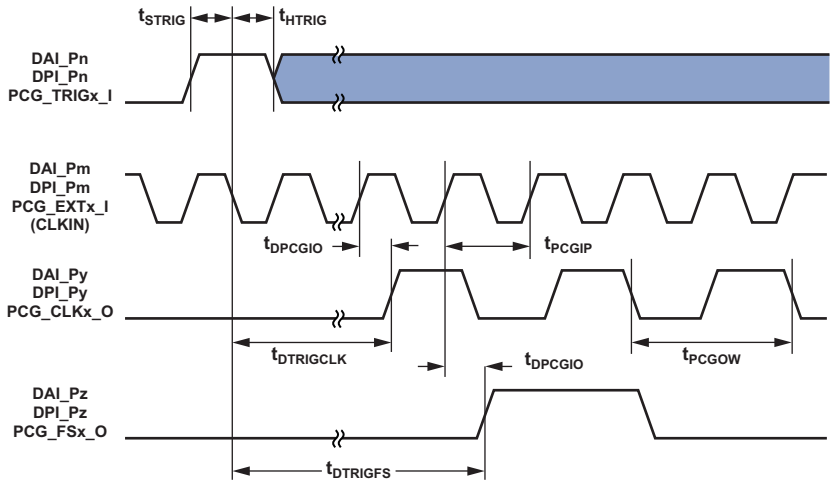


*Figure 16. Precision Clock Generator (Direct Pin Routing)*

### *Flags*

The timing specifications provided below apply to the DPI_P14–1, ADDR7–0, ADDR23–8, DATA7–0, and FLAG3–0 pins when configured as FLAGS. See Table 11 on Page 14 for more information on flag use.

**Table 30. Flags**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{FIPW}$[1] | FLAGs IN Pulse Width | $2 \times t_{PCLK} + 3$ | | ns |
| *Switching Characteristic* | | | | |
| $t_{FOPW}$[1] | FLAGs OUT Pulse Width | $2 \times t_{PCLK} - 3$ | | ns |

[1] This is applicable when the Flags are connected to DPI_P14–1, ADDR7–0, ADDR23–8, DATA7–0 and FLAG3–0 pins.

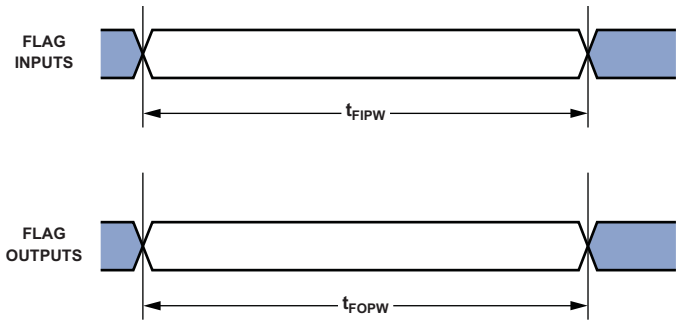


*Figure 17. Flags*

### *SDRAM Interface Timing (166 MHz SDCLK)*

The maximum frequency for SDRAM is 166 MHz. For information on SDRAM frequency and programming, see the hardware reference, Engineer-to-Engineer Note Interfacing SDRAM Memories to SHARC Processors (EE-286), and the SDRAM vendor data sheet.

**Table 31. SDRAM Interface Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SSDAT}$ | DATA Setup Before SDCLK | 0.7 | | ns |
| $t_{HSDAT}$ | DATA Hold After SDCLK | 1.23 | | ns |
| *Switching Characteristics* | | | | |
| $t_{SDCLK}$[1] | SDCLK Period | 6 | | ns |
| $t_{SDCLKH}$ | SDCLK Width High | 2.2 | | ns |
| $t_{SDCLKL}$ | SDCLK Width Low | 2.2 | | ns |
| $t_{DCAD}$[2] | Command, ADDR, Data Delay After SDCLK | | 4 | ns |
| $t_{HCAD}$[2] | Command, ADDR, Data Hold After SDCLK | 1 | | ns |
| $t_{DSDAT}$ | Data Disable After SDCLK | | 5.3 | ns |
| $t_{ENSDAT}$ | Data Enable After SDCLK | 0.3 | | ns |

[1] Systems should use the SDRAM model with a speed grade higher than the desired SDRAM controller speed. For example, to run the SDRAM controller at 166 MHz the SDRAM model with a speed grade of 183 MHz or above should be used. See Engineer-to-Engineer Note Interfacing SDRAM Memories to SHARC Processors (EE-286) for more information on hardware design guidelines for the SDRAM interface.
[2] Command pins include: $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{MSx}}$, SDA10, SDCKE.

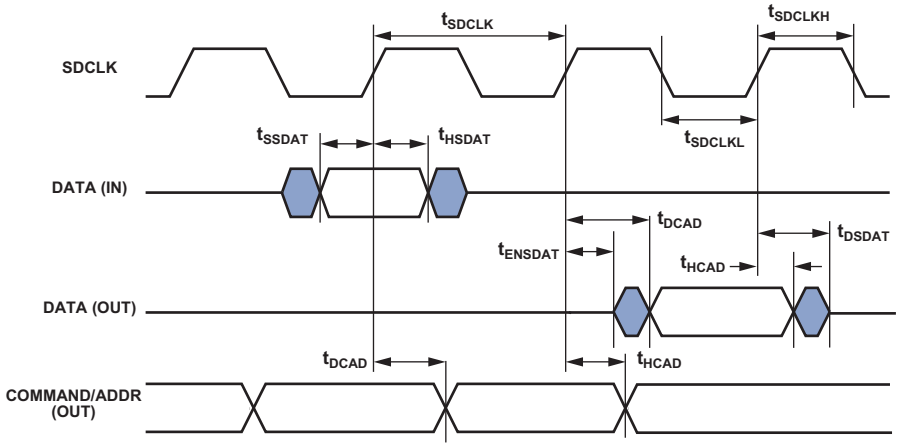


*Figure 18. SDRAM Interface Timing*

### *AMI Read*

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

**Table 32. AMI Read**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{DAD}$[1, 2, 3] | Address Selects Delay to Data Valid | | W + $t_{SDCLK}$ –5.4 | ns |
| $t_{DRLD}$[1, 3] | $\overline{\text{AMI\_RD}}$ Low to Data Valid | | W – 3.2 | ns |
| $t_{SDS}$ | Data Setup to $\overline{\text{AMI\_RD}}$ High | 2.5 | | ns |
| $t_{HDRH}$[4, 5] | Data Hold from $\overline{\text{AMI\_RD}}$ High | 0 | | ns |
| $t_{DAAK}$[2, 6] | AMI_ACK Delay from Address, Selects | | $t_{SDCLK}$ –9.5 + W | ns |
| $t_{DSAK}$[4] | AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low | | W – 7 | ns |
| *Switching Characteristics* | | | | |
| $t_{DRHA}$ | Address Selects Hold After $\overline{\text{AMI\_RD}}$ High | RHC + 0.20 | | ns |
| $t_{DARL}$[2] | Address Selects to $\overline{\text{AMI\_RD}}$ Low | $t_{SDCLK}$ – 3.8 | | ns |
| $t_{RW}$ | $\overline{\text{AMI\_RD}}$ Pulse Width | W – 1.4 | | ns |
| $t_{RWR}$ | $\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low | HI + $t_{SDCLK}$ – 1 | | ns |

W = (number of wait states specified in AMICTLx register) × $t_{SDCLK}$.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × $t_{SDCLK}$
Where PREDIS = 0
HI = RHC (if IC=0): Read to Read from same bank
HI = RHC + $t_{SDCLK}$ (if IC>0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × $t_{SDCLK}$)): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × $t_{SDCLK}$)): Read to Write from same or different bank
HI = RHC + (3 × $t_{SDCLK}$): Read to Read from same bank
HI = RHC + Max (IC, (3 × $t_{SDCLK}$): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × $t_{SDCLK}$
H = (number of hold cycles specified in AMICTLx register) × tSDCLK

[1] Data delay/setup: System must meet $t_{DAD}$, $t_{DRLD}$, or $t_{SDS}$.
[2] The falling edge of $\overline{\text{MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for $t_{DAD}$ and $t_{DRLD}$ parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet $t_{HDRH}$ in asynchronous access mode. See Test Conditions on Page 55 for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet $t_{DAAK}$, or $t_{DSAK}$, for deassertion of AMI_ACK (low).

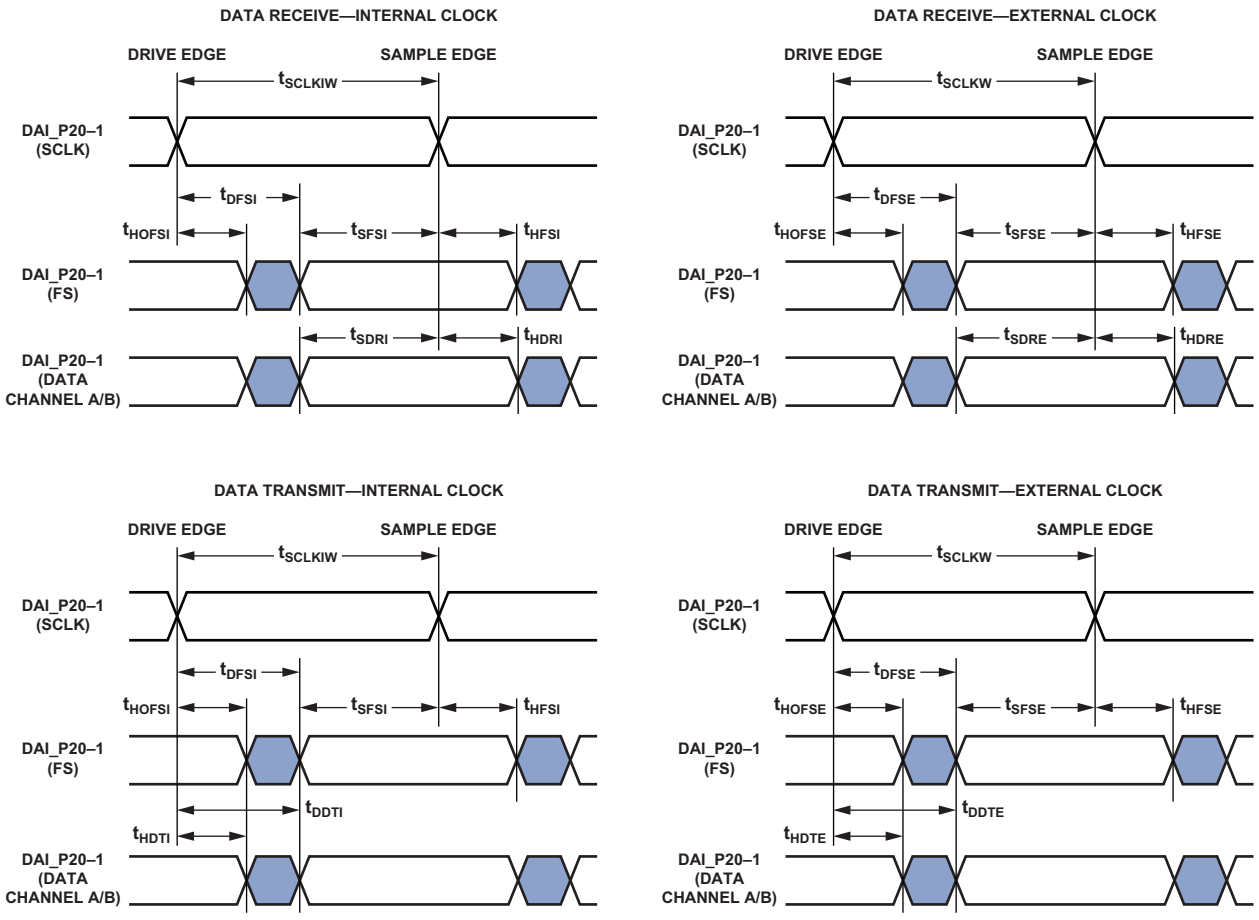


*Figure 21. Serial Ports*

### *Input Data Port (IDP)*

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 39. Input Data Port (IDP)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SISFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 3.8 | | ns |
| $t_{SIHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 2.5 | | ns |
| $t_{SISD}$[1] | Data Setup Before Serial Clock Rising Edge | 2.5 | | ns |
| $t_{SIHD}$[1] | Data Hold After Serial Clock Rising Edge | 2.5 | | ns |
| $t_{IDPCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{IDPCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

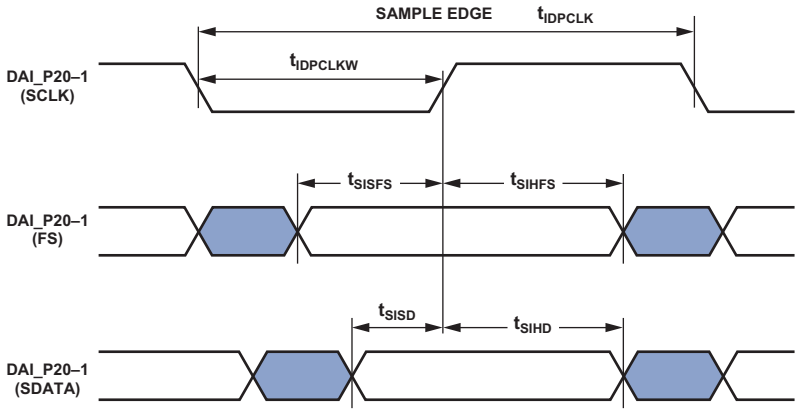


*Figure 25. IDP Master Timing*

### *Sample Rate Converter—Serial Input Port*

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 41 are valid at the DAI_P20–1 pins.

**Table 41. ASRC, Serial Input Port**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SRCSFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCSD}$[1] | Data Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHD}$[1] | Data Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{SRCCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

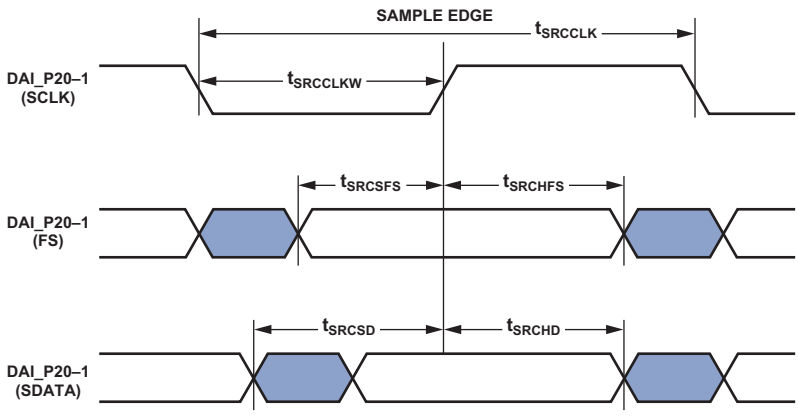


*Figure 27. ASRC Serial Input Port Timing*

### *Sample Rate Converter—Serial Output Port*

For the serial output port, the frame sync is an input, and it should meet setup and hold times with regard to SCLK on the output port. The serial data output has a hold time and delay specification with regard to serial clock. Note that serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

**Table 42. ASRC, Serial Output Port**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SRCSFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{SRCCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{SRCTDD}$[1] | Transmit Data Delay After Serial Clock Falling Edge | | 9.9 | ns |
| $t_{SRCTDH}$[1] | Transmit Data Hold After Serial Clock Falling Edge | 1 | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

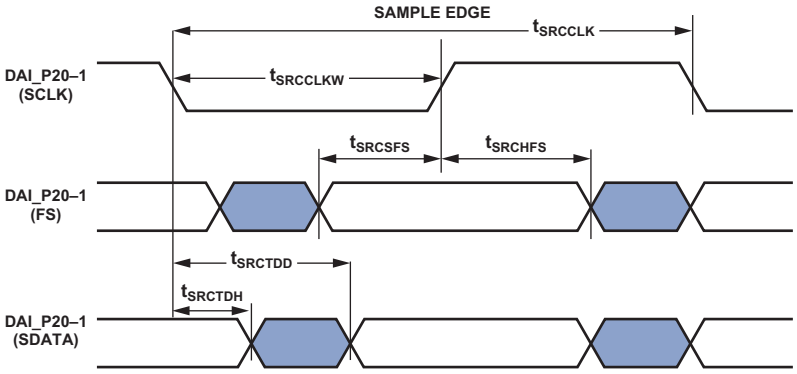


*Figure 28. ASRC Serial Output Port Timing*

Figure 31 shows the default I²S-justified mode. The frame sync is low for the left channel and HI for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

**Table 45. S/PDIF Transmitter I²S Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{I2SD}$ | Frame Sync to MSB Delay in I²S Mode | 1 | SCLK |

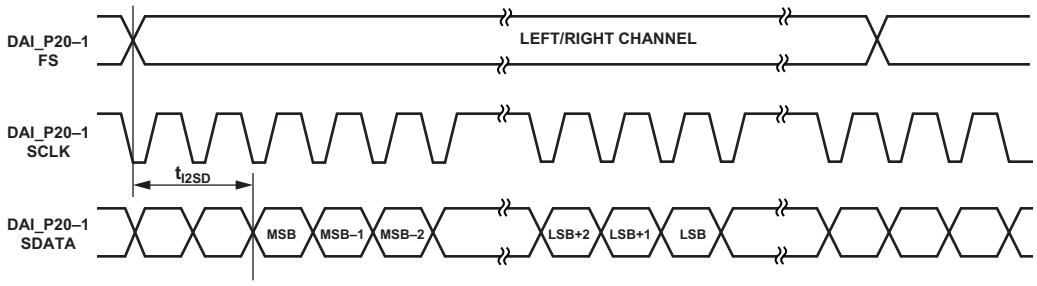


*Figure 31. I²S-Justified Mode*

Figure 32 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

**Table 46. S/PDIF Transmitter Left-Justified Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{LJD}$ | Frame Sync to MSB Delay in Left-Justified Mode | 0 | SCLK |

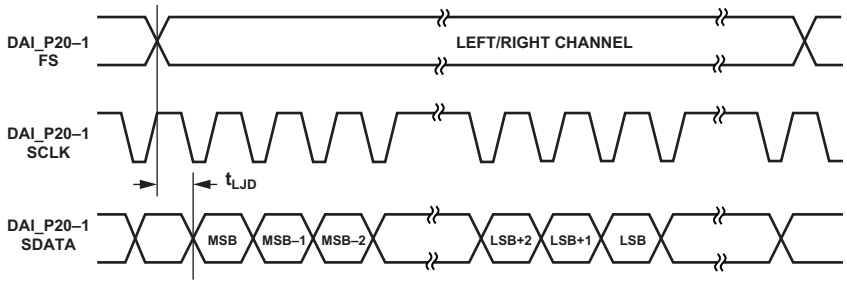


*Figure 32. Left-Justified Mode*

### S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 47. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 47. S/PDIF Transmitter Input Data Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SISFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 3 | | ns |
| $t_{SIHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 3 | | ns |
| $t_{SISD}$[1] | Data Setup Before Serial Clock Rising Edge | 3 | | ns |
| $t_{SIHD}$[1] | Data Hold After Serial Clock Rising Edge | 3 | | ns |
| $t_{SITXCLKW}$ | Transmit Clock Width | 9 | | ns |
| $t_{SITXCLK}$ | Transmit Clock Period | 20 | | ns |
| $t_{SISCLKW}$ | Clock Width | 36 | | ns |
| $t_{SISCLK}$ | Clock Period | 80 | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

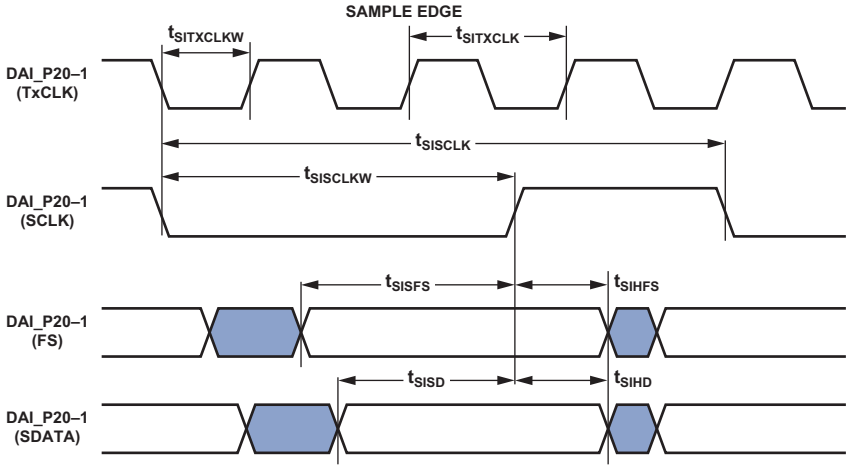


*Figure 33. S/PDIF Transmitter Input Timing*

### Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

**Table 48. Oversampling Clock (TxCLK) Switching Characteristics**

| Parameter | Max | Unit |
|---|---|---|
| Frequency for TxCLK = 384 × Frame Sync | Oversampling Ratio × Frame Sync <= $1/t_{SITXCLK}$ | MHz |
| Frequency for TxCLK = 256 × Frame Sync | 49.2 | MHz |
| Frame Rate (FS) | 192.0 | kHz |

### *S/PDIF Receiver*

The following section describes timing as it relates to the S/PDIF receiver.

#### Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

**Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DFSI}$ | Frame Sync Delay After Serial Clock | | 5 | ns |
| $t_{HOFSI}$ | Frame Sync Hold After Serial Clock | –2 | | ns |
| $t_{DDTI}$ | Transmit Data Delay After Serial Clock | | 5 | ns |
| $t_{HDTI}$ | Transmit Data Hold After Serial Clock | –2 | | ns |
| $t_{SCLKIW}$[1] | Transmit Serial Clock Width | $8 \times t_{PCLK} - 2$ | | ns |

[1] SCLK frequency is 64 × FS where FS = the frequency of frame sync.

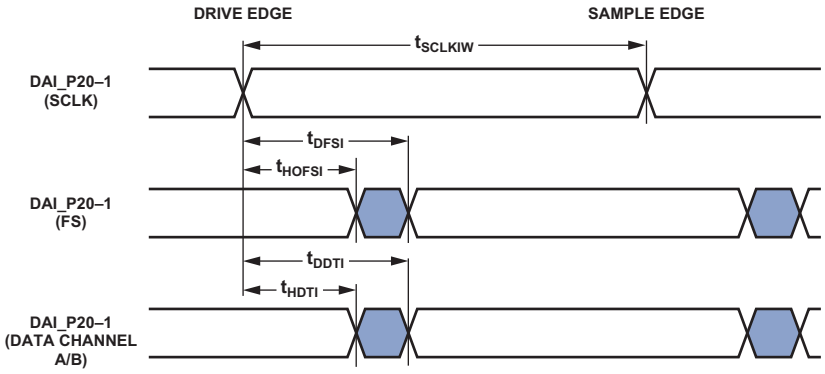


*Figure 34. S/PDIF Receiver Internal Digital PLL Mode Timing*

### *SPI Interface—Slave*

**Table 51. SPI Interface Protocol—Slave Switching and Timing Specifications**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SPICLKS}$ | Serial Clock Cycle | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICHS}$ | Serial Clock High Period | $2 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICLS}$ | Serial Clock Low Period | $2 \times t_{PCLK} - 2$ | | ns |
| $t_{SDSCO}$ | $\overline{SPIDS}$ Assertion to First SPICLK Edge<br>CPHASE = 0<br>CPHASE = 1 | $2 \times t_{PCLK}$ | | ns |
| $t_{HDS}$ | Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0 | $2 \times t_{PCLK}$ | | ns |
| $t_{SSPIDS}$ | Data Input Valid to SPICLK edge (Data Input Set-up Time) | 2 | | ns |
| $t_{HSPIDS}$ | SPICLK Last Sampling Edge to Data Input Not Valid | 2 | | ns |
| $t_{SDPPW}$ | $\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0) | $2 \times t_{PCLK}$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{DSOE}$ | $\overline{SPIDS}$ Assertion to Data Out Active | 0 | 7.5 | ns |
| $t_{DSOE}$[1] | $\overline{SPIDS}$ Assertion to Data Out Active (SPI2) | 0 | 7.5 | ns |
| $t_{DSDHI}$ | $\overline{SPIDS}$ Deassertion to Data High Impedance | 0 | 10.5 | ns |
| $t_{DSDHI}$[1] | $\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2) | 0 | 10.5 | ns |
| $t_{DDSPIDS}$ | SPICLK Edge to Data Out Valid (Data Out Delay Time) | | 9.5 | ns |
| $t_{HDSPIDS}$ | SPICLK Edge to Data Out Not Valid (Data Out Hold Time) | $2 \times t_{PCLK}$ | | ns |
| $t_{DSOV}$ | $\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0) | | $5 \times t_{PCLK}$ | ns |

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the "Serial Peripheral Interface Port" chapter of the hardware reference.

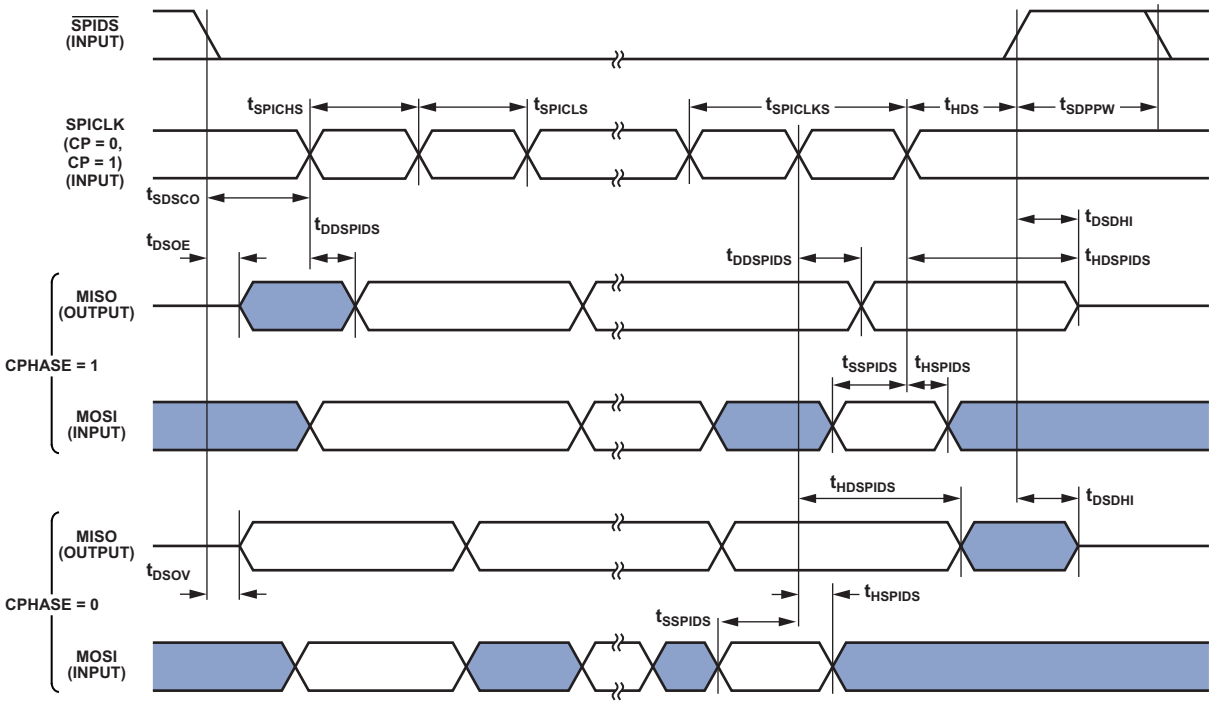


*Figure 36. SPI Slave Timing*

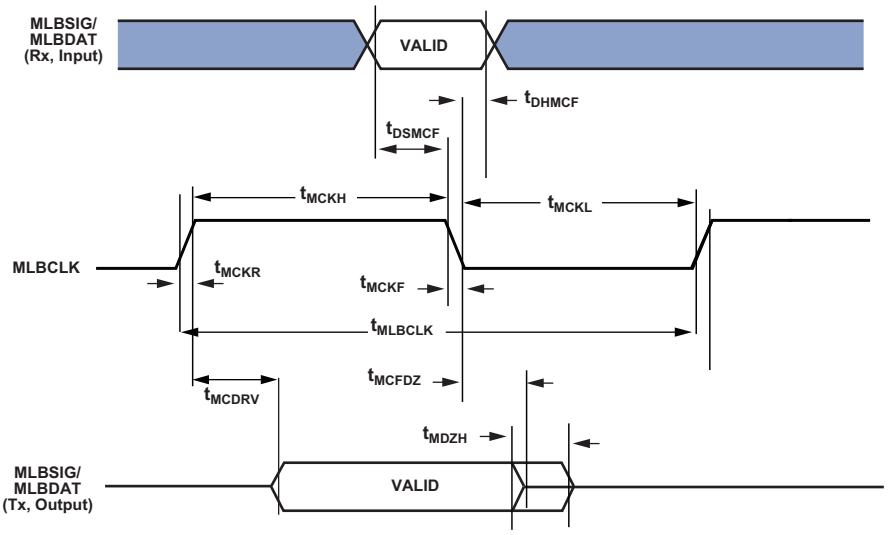


*Figure 37. MLB Timing (3-Pin Interface)*

**Table 53. MLB Interface, 5-Pin Specifications**

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| *5-Pin Characteristics* | | | | | |
| $t_{MLBCLK}$ | MLB Clock Period | | | | |
| | 512 FS | | 40 | | ns |
| | 256 FS | | 81 | | ns |
| $t_{MCKL}$ | MLBCLK Low Time | | | | |
| | 512 FS | 15 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKH}$ | MLBCLK High Time | | | | |
| | 512 FS | 15 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKR}$ | MLBCLK Rise Time ($V_{IL}$ to $V_{IH}$) | | | 6 | ns |
| $t_{MCKF}$ | MLBCLK Fall Time ($V_{IH}$ to $V_{IL}$) | | | 6 | ns |
| $t_{MPWV}$[1] | MLBCLK Pulse Width Variation | | | 2 | nspp |
| $t_{DSMCF}$[2] | DAT/SIG Input Setup Time | 3 | | | ns |
| $t_{DHMCF}$ | DAT/SIG Input Hold Time | 5 | | | ns |
| $t_{MCDRV}$ | DS/DO Output Data Delay From MLBCLK Rising Edge | | | 8 | ns |
| $t_{MCRDL}$[3] | DO/SO Low From MLBCLK High | | | | |
| | 512 FS | | | 10 | ns |
| | 256 FS | | | 20 | ns |
| $C_{MLB}$ | DS/DO Pin Load | | | 40 | pf |

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] Gate Delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

Note that the thermal characteristics values provided in Table 56 and Table 57 are modeled values.

**Table 56. Thermal Characteristics for 100-Lead LQFP_EP**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Airflow = 0 m/s | 17.8 | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 15.4 | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 14.6 | °C/W |
| $\theta_{JC}$ | | 2.4 | °C/W |
| $\Psi_{JT}$ | Airflow = 0 m/s | 0.24 | °C/W |
| $\Psi_{JMT}$ | Airflow = 1 m/s | 0.37 | °C/W |
| $\Psi_{JMT}$ | Airflow = 2 m/s | 0.51 | °C/W |

**Table 57. Thermal Characteristics for 176-Lead LQFP_EP**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Airflow = 0 m/s | 16.9 | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 14.6 | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 13.8 | °C/W |
| $\theta_{JC}$ | | 2.3 | °C/W |
| $\Psi_{JT}$ | Airflow = 0 m/s | 0.21 | °C/W |
| $\Psi_{JMT}$ | Airflow = 1 m/s | 0.32 | °C/W |
| $\Psi_{JMT}$ | Airflow = 2 m/s | 0.41 | °C/W |

### *Thermal Diode*

The ADSP-2148x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

$n$ = multiplication factor close to 1, depending on process variations

$k$ = Boltzmann's constant

$T$ = temperature (°C)

$q$ = charge of the electron

$N$ = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

Table 58 contains the thermal diode specifications using the transistor model.

**Table 58. Thermal Diode Parameters – Transistor Model[1]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{FW}$[2] | Forward Bias Current | 10 | | 300 | µA |
| $I_E$ | Emitter Current | 10 | | 300 | µA |
| $n_Q$[3, 4] | Transistor Ideality | 1.012 | 1.015 | 1.017 | |
| $R_T$[3, 5] | Series Resistance | 0.12 | 0.2 | 0.28 | Ω |

[1] See Engineer-to-Engineer Note Using the On-Chip Thermal Diode on Analog Devices Processors (EE-346).
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where $I_S$ = saturation current, q = electronic charge, $V_{BE}$ = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
[5] The series resistance ($R_T$) can be used for more accurate readings as needed.

Figure 50 shows the top view of the 176-lead LQFP_EP lead configuration. Figure 51 shows the bottom view of the 176-lead LQFP_EP lead configuration.

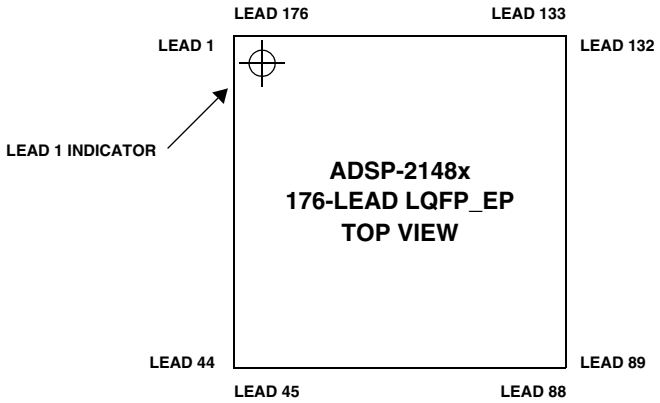


*Figure 50. 176-Lead LQFP_EP Lead Configuration (Top View)*

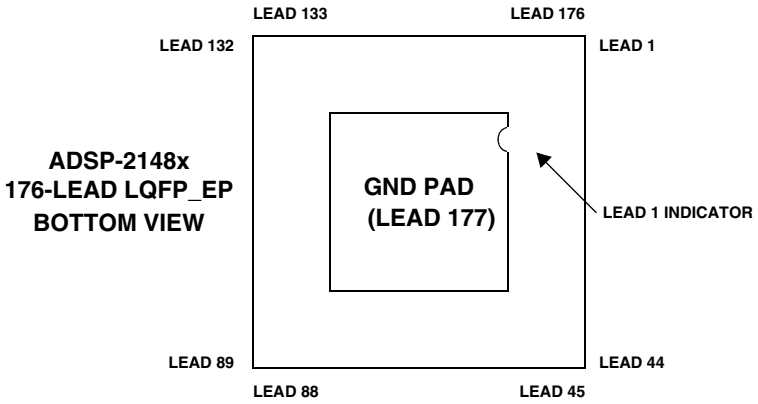


*Figure 51. 176-Lead LQFP_EP Lead Configuration (Bottom View)*

| Model[1] | Notes | Temperature Range[2] | RAM | Processor Instruction Rate (Max) | Package Description | Package Option |
|---|---|---|---|---|---|---|
| ADSP-21487KSWZ-2B | 3 | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-2BB | 3 | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-3B | 3 | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-3BB | 3 | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-4B | 3 | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-4BB | 3 | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-5B | 3, 4 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-5BB | 3, 4 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP21487KSWZ5BBRL | 5 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-3A | | –40°C to +85°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3A | | 0°C to +70°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3A1 | 6 | 0°C to +70°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3B | | 0°C to +70°C | 3 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-3B | | –40°C to +85°C | 3 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488KSWZ-4A | | 0°C to +70°C | 3 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488BSWZ-4A | | –40°C to +85°C | 3 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-4B | | 0°C to +70°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-4B | | –40°C to +85°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488KSWZ-4B1 | 6 | 0°C to +70°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-3A | | 0°C to +70°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489BSWZ-3A | | –40°C to +85°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489KSWZ-3B | | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489BSWZ-3B | | –40°C to +85°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-4A | | 0°C to +70°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489BSWZ-4A | | –40°C to +85°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489KSWZ-4B | | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489BSWZ-4B | | –40°C to +85°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-5B | 4 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature ($T_J$) specification, which is the only temperature specification.

[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

[4] See Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for operating ADSP-2148x processors at 450 MHz.

[5] RL = Tape and Reel.

[6] This product contains a –140 dB sample rate converter.