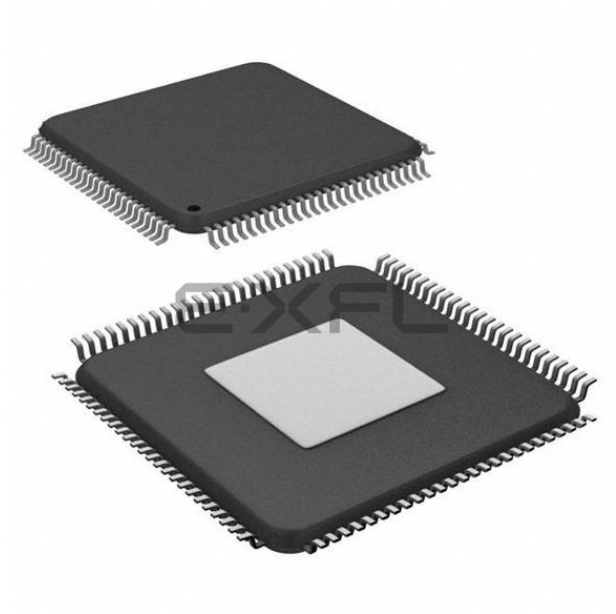

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	EBI/EMI, DAI, I²C, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21488kswz-4a

Table 4. Internal Memory Space (5 MBits—ADSP-21486/ADSP-21487/ADSP-21489)[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 EFFF	Block 0 SRAM 0x0008 C000–0x0009 3FFF	Block 0 SRAM 0x0009 2000–0x0009 DFFF	Block 0 SRAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 EFFF	Block 1 SRAM 0x000A C000–0x000B 3FFF	Block 1 SRAM 0x000B 2000–0x000B DFFF	Block 1 SRAM 0x0016 4000–0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 3FFF	Block 2 SRAM 0x000C 0000–0x000C 5554	Block 2 SRAM 0x000C 0000–0x000C 7FFF	Block 2 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000– 0x0006 FFFF	Reserved 0x000C 5555–0x000D FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 3FFF	Block 3 SRAM 0x000E 0000–0x000E 5554	Block 3 SRAM 0x000E 0000–0x000E 7FFF	Block 3 SRAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x0000F FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

[1] Some ADSP-2148x processors include a customer-definable ROM block and are not reserved as shown on this table. Please contact your Analog Devices sales representative for additional details.

instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

ROM Based Security

The ADSP-2148x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features are available after the correct key is scanned.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2 × 64-bits, CCLK speed) and the IOD0/1 buses (2 × 32-bit, PCLK speed).

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2148x family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Memory

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 6M words of external memory in bank 0 and 8M words of external memory in bank 1, bank 2, and bank 3.
- A SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in bank 0, and 64M words of external memory in bank 1, bank 2, and bank 3. NOTE: This feature is not available on the ADSP-21486 product.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single-update mode or double-update mode. In single-update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double-update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

MediaLB

The automotive models of the ADSP-2148x processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive models, see Automotive Products on Page 66.

Digital Applications Interface (DAI)

The digital applications interface (DAI) allows the connection of various peripherals to any of the DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes eight serial ports, four precision clock generators (PCG), a S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports (SPORTs)

The ADSP-2148x features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^2S or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, or the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter (SRC)

The asynchronous sample rate converter contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode.

The IDP also provides a parallel data acquisition port (PDAP), which can be used for receiving parallel data. The PDAP port has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

The outputs of PCG A and B can be routed through the DAI pins and the outputs of PCG C and D can be driven on to the DAI as well as the DPI pins.

Digital Peripheral Interface (DPI)

The ADSP-2148x SHARC processors have a digital peripheral interface that provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), three PWM modules (PWM3–1), and two general-purpose timers.

Serial Peripheral (Compatible) Interface (SPI)

The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O)—The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access)—The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Timers

The ADSP-2148x has a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

I/O PROCESSOR FEATURES

The I/O processors provide up to 65 channels of DMA, as well as an extensive set of peripherals.

DMA Controller

The processor's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-2148x's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the PDAP, or the UART. The DMA channel summary is shown in Table 8.

Programs can be downloaded to the ADSP-2148x using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Table 8. DMA Channels

Peripheral	DMA Channels
SPORTs	16
IDP/PDAP	8
SPI	2
UART	2
External Port	2
Accelerators	2
Memory-to-Memory	2
MLB[1]	31

[1] Automotive models only.

Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from non contiguous memory blocks.

FFT Accelerator

The FFT accelerator implements a radix-2 complex/real input, complex output FFT with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watchdog Timer

The watchdog timer is used to supervise the stability of the system software. When used in this way, software reloads the watchdog timer in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset, if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer. The watchdog timer resets both the core and the internal peripherals. Note that this feature is available on the 176-lead package only.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2148x boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2–0) pins in Table 9 for the 176-lead package and Table 10 for the 100-lead package.

Table 9. Boot Mode Selection, 176-Lead Package

BOOT_CFG2–0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI User Boot (for 8-bit Flash Boot)
011	No boot (processor executes from internal ROM after reset)
1xx	Reserved

Table 10. Boot Mode Selection, 100-Lead Package

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Reserved
11	No boot (processor executes from internal ROM after reset)

The "Running Reset" feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the RESETOUT/RUNRSTIN pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the hardware reference.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal supply must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Static Voltage Scaling (SVS)

Some models of the ADSP-2148x feature Static Voltage Scaling (SVS) on the V_{DD_INT} power supply. (See the Ordering Guide on Page 66 for model details.) This voltage specification technique can provide significant performance benefits including 450 MHz core frequency operation without a significant increase in power.

SVS optimizes the required V_{DD_INT} voltage for each individual device to enable enhanced operating frequency up to 450 MHz. The optimized SVS voltage results in a reduction of maximum I_{DD_INT} which enables 450 MHz operation at the same or lower maximum power than 400 MHz operation at a fixed voltage supply. Implementation of SVS requires a specific voltage regulator circuit design and initialization code.

Refer to the Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for further information. The EE-Note details the requirements and process to implement a SVS power supply system to enable operation up to 450 MHz. This applies only to specific products within the ADSP-2148x family which are capable of supporting 450 MHz operation.

Details on power consumption and Static and Dynamic current consumption can be found at Total Power Dissipation on Page 20. Also see Operating Conditions on Page 18 for more information.

The following are SVS features.

- SVS is applicable only to 450 MHz models (not applicable to 400 MHz or lower frequency models).
- Each individual SVS device includes a register (SVS_DAT) containing the unique SVS voltage set at the factory, known as SVS_{NOM}.
- The SVS_{NOM} value is the intended set voltage for the V_{DD_INT} voltage regulator.
- No dedicated pins are required for SVS. The TWI serial bus is used to communicate SVS_{NOM} to the voltage regulator.
- Analog Devices recommends a specific voltage regulator design and initialization code sequence that optimizes the power-up sequence.

  The Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) contains the details of the regulator design and the initialization requirements.
- Any differences from the Analog Devices recommended programmable regulator design must be reviewed by Analog Devices to ensure that it meets the voltage accuracy and range requirements.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2148x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

CrossCore Embedded Studio is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the Product Download area of the product web page.

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23–0}$	I/O/T (ipu)	High-Z/ driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, and FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in external memory interface mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23–4}$ pins for parallel input data.
$DATA_{15–0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), and $FLAGS_{7–0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0–1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information, see the hardware reference.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.**
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.**

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	300 MHz / 350 MHz / 400 MHz			450 MHz			Unit
		Min	Nominal	Max	Min	Nominal	Max	
V_{DD_INT}[2]	Internal (Core) Supply Voltage	1.05	1.1	1.15	SVS_{NOM} – 25 mV	1.0 – 1.15	SVS_{NOM} + 25 mV	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13		3.47	3.13		3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13		3.47	3.13		3.47	V
V_{IH}[3]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0		3.6	2.0		3.6	V
V_{IL}[3]	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		0.8	–0.3		0.8	V
V_{IH_CLKIN}[4]	High Level Input Voltage @ V_{DD_EXT} = Max	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		+0.8	–0.3		+0.8	V
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C

[1] Specifications subject to change without notice.

[2] SVS_{NOM} refers to the nominal SVS voltage which is set between 1.0 V and 1.15 V at the factory for each individual device. Only the unique SVS_{NOM} value in each chip may be used for 401 MHz to 450 MHz operation of that chip. This spec lists the possible range of the SVS_{NOM} values for all devices. The initial VDD_INT voltage at power on is 1.1 V nominal and it transitions to SVS programmed voltage as outlined in Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357).

[3] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[4] Applies to input pins CLKIN, WDT_CLKIN.

Total Power Dissipation

The information in this section should be augmented with the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348).

Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature (T_J) and core voltage (V_{DD_INT}).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13).

     Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

Table 13. Activity Scaling Factors (ASF)[1]

Activity	Scaling Factor (ASF)
Idle	0.29
Low	0.53
Medium Low	0.61
Medium High	0.77
Peak Typical (50:50)[2]	0.85
Peak Typical (60:40)[2]	0.93
Peak Typical (70:30)[2]	1.00
High Typical	1.16
High	1.25
Peak	1.31

[1] See the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for more information on the explanation of the power vectors specific to the ASF table.

[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]

	V_{DD_INT} (V)								
T_J (°C)	0.975 V	1.0 V	1.025 V	1.05 V	1.075 V	1.10 V	1.125 V	1.15 V	1.175 V
–45	68	77	86	96	107	118	131	144	159
–35	74	83	92	103	114	126	140	154	170
–25	82	92	101	113	125	138	153	168	185
–15	94	104	115	127	140	155	171	187	205
–5	109	121	133	147	161	177	194	212	233
+5	129	142	156	171	188	206	225	245	268
+15	152	168	183	201	219	240	261	285	309
+25	182	199	216	237	257	280	305	331	360
+35	217	237	256	279	303	329	358	388	420
+45	259	282	305	331	359	389	421	455	492
+55	309	334	361	391	423	458	495	533	576
+65	369	398	429	464	500	539	582	626	675
+75	437	471	506	547	588	633	682	731	789
+85	519	559	599	645	693	746	802	860	926
+95	615	662	707	761	816	877	942	1007	1083
+105	727	779	833	897	958	1026	1103	1179	1266
+115	853	914	975	1047	1119	1198	1285	1372	1473
+125	997	1067	1138	1219	1305	1397	1498	1601	1716

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

Table 15. Dynamic Current in CCLK Domain—$I_{DD\_INT\_DYNAMIC}$ (mA, with ASF = 1.0)[1, 2]

f_{CCLK} (MHz)	V_{DD_INT} (V)								
	0.975 V	1.0 V	1.025 V	1.05 V	1.075 V	1.10 V	1.125 V	1.15 V	1.175 V
100	76	77	81	84	87	88	90	92	95
150	117	119	123	126	130	133	136	139	144
200	153	156	161	165	170	174	179	183	188
250	190	195	201	207	212	217	223	229	235
300	227	233	240	246	253	260	266	273	280
350	263	272	278	286	294	302	309	318	325
400	300	309	317	326	335	344	352	361	370
450	339	349	356	365	374	385	394	405	415

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 19.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 18.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 16 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 16. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +3.6 V
Thermal Diode Supply Voltage (V_{DD_THD})	–0.3 V to +3.6 V
Input Voltage	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DD_EXT} +0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 56.

PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-2148x processors. For a complete listing of product availability, see Ordering Guide on Page 66.

Figure 3. Typical Package Brand

Table 17. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non automotive only. For branding information specific to automotive products, contact Analog Devices Inc.

Clock Signals

The ADSP-2148x can use an external clock or a crystal. See the CLKIN pin description in Table 11 on Page 14. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

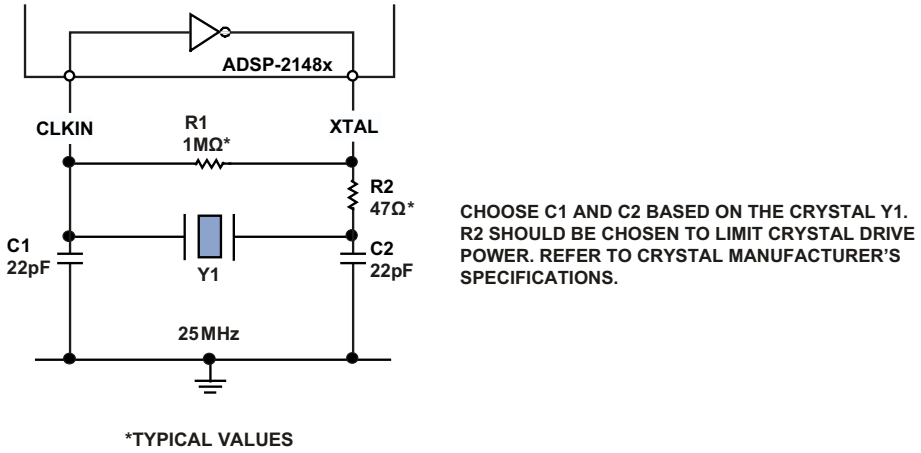

Figure 7. Recommended Circuit for Fundamental Mode Crystal Operation

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		W + t_{SDCLK} –5.4	ns
t_{DRLD}[1, 3]	$\overline{\text{AMI\_RD}}$ Low to Data Valid		W – 3.2	ns
t_{SDS}	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.5		ns
t_{HDRH}[4, 5]	Data Hold from $\overline{\text{AMI\_RD}}$ High	0		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address, Selects		t_{SDCLK} –9.5 + W	ns
t_{DSAK}[4]	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low		W – 7	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RHC + 0.20		ns
t_{DARL}[2]	Address Selects to $\overline{\text{AMI\_RD}}$ Low	t_{SDCLK} – 3.8		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	HI + t_{SDCLK} – 1		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
Where PREDIS = 0
HI = RHC (if IC=0): Read to Read from same bank
HI = RHC + t_{SDCLK} (if IC>0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{SDCLK}): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × tSDCLK

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 55 for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).

Serial Ports

In slave transmitter mode and master receiver mode, the maximum serial port frequency is $f_{PCLK}/8$. In master transmitter mode and slave receiver mode, the maximum serial port clock frequency is $f_{PCLK}/4$. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold; 2) data delay and data setup and hold; and 3) SCLK width.

Serial port signals (SCLK, frame sync, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		10.25	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 35. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–2		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

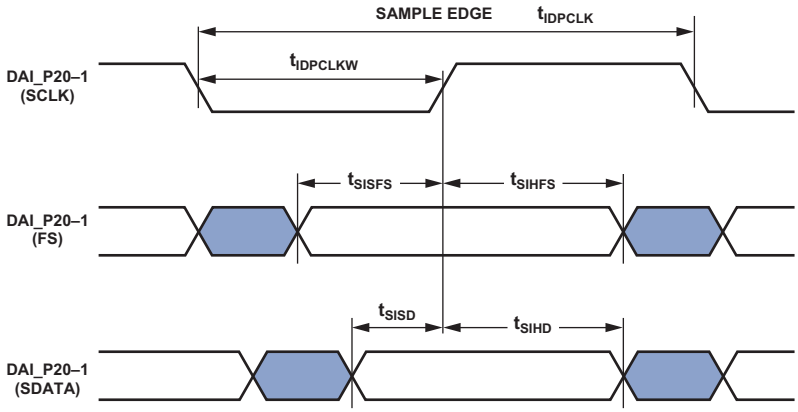

Figure 25. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 40. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the hardware reference. Note that the 20 bits of external PDAP data can be provided through the ADDR23–4 pins or over the DAI pins.

Table 40. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

[1] Source pins of PDAP_DATA are ADDR23–4 or DAI pins. Source pins for PDAP_CLK and PDAP_HOLD are 1) DAI pins; 2) CLKIN through PCG; 3) DAI pins through PCG; or 4) ADDR3–2 pins.

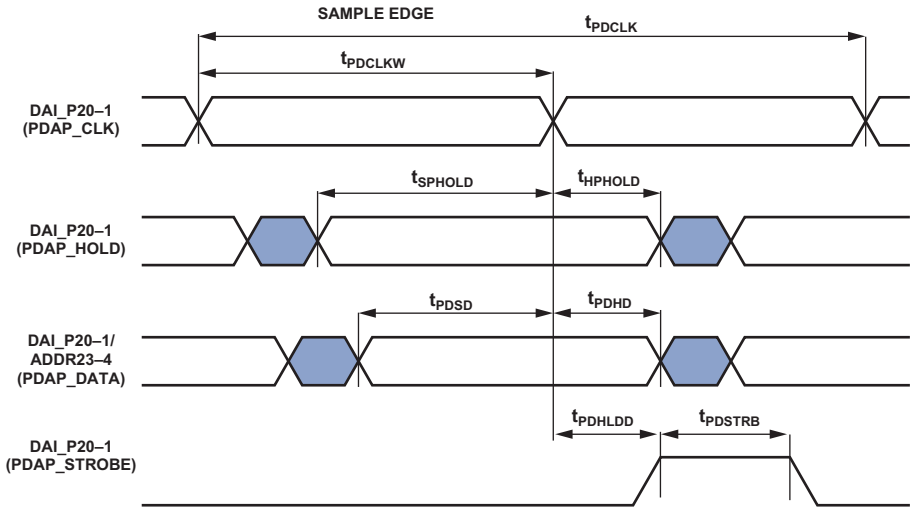

Figure 26. PDAP Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the ADDR23–8/DPI_14–1 pins are configured as PWM.

Table 43. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

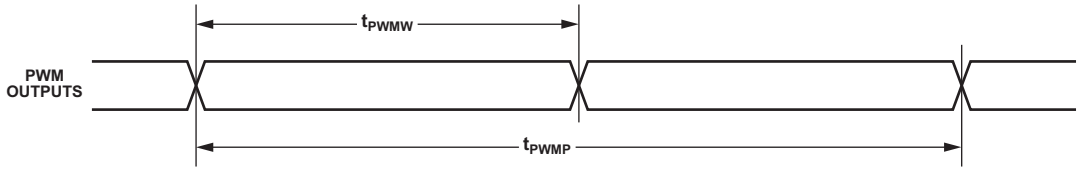

Figure 29. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 30 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Table 44. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	Frame Sync to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

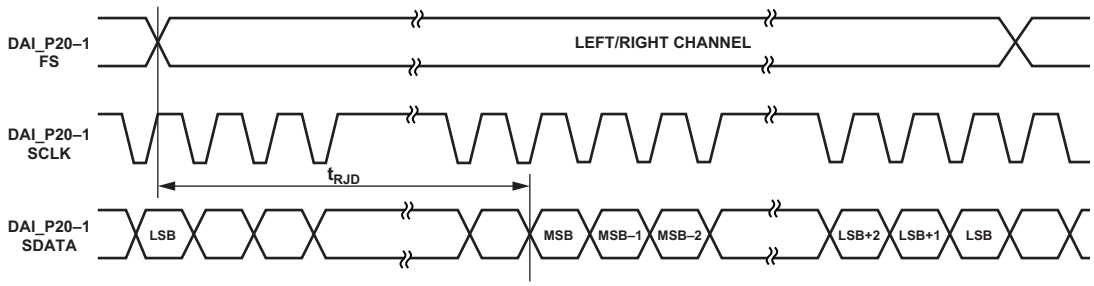

Figure 30. Right-Justified Mode

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After Serial Clock		5	ns
t_{HOFSI}	Frame Sync Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	$8 \times t_{PCLK} - 2$		ns

[1] SCLK frequency is 64 × FS where FS = the frequency of frame sync.

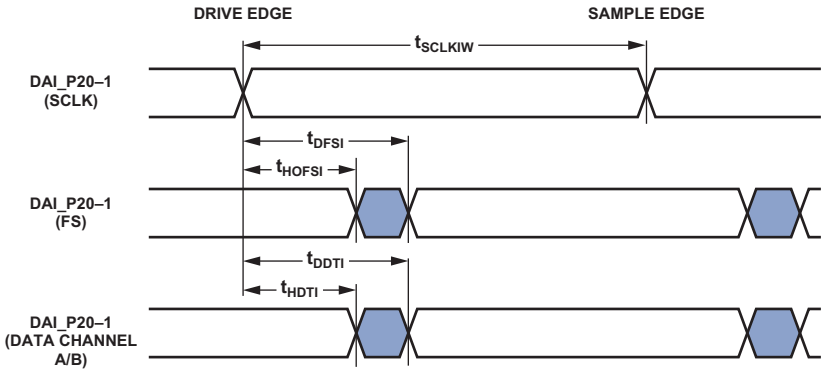

Figure 34. S/PDIF Receiver Internal Digital PLL Mode Timing

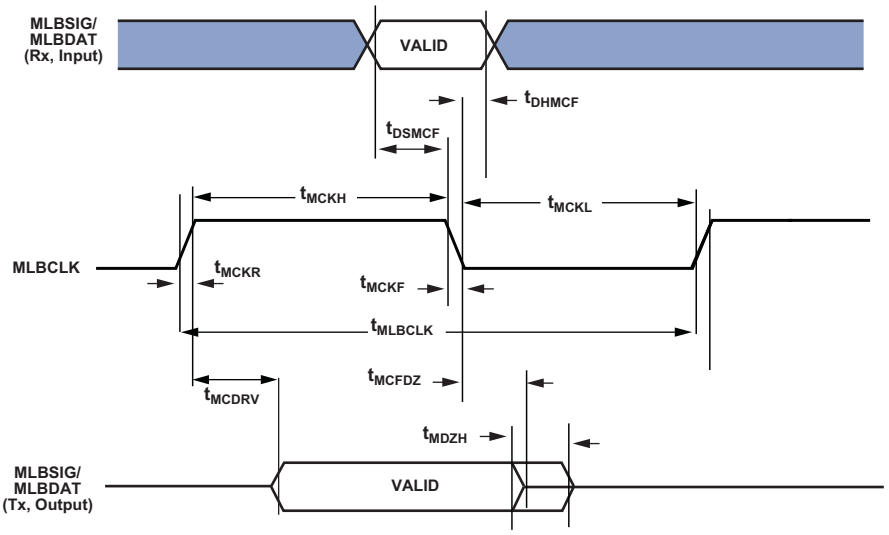

Figure 37. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	nspp
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{MLB}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] Gate Delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

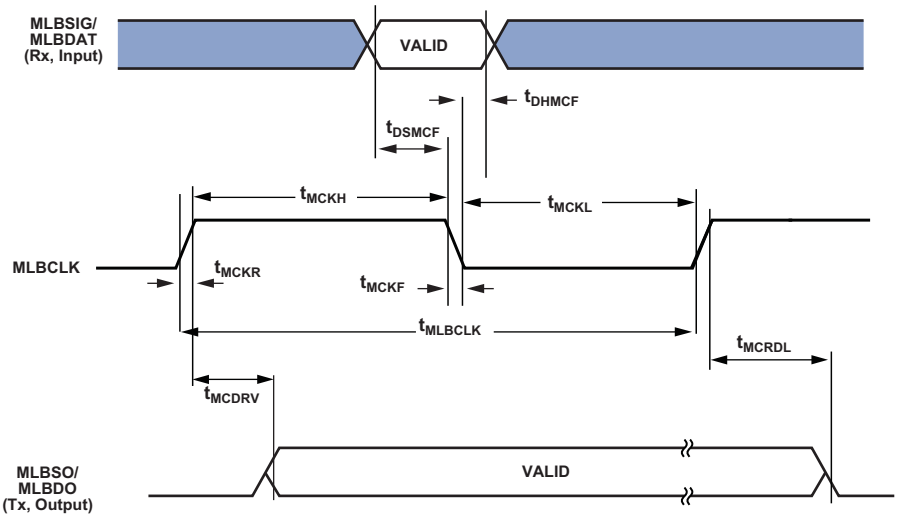

Figure 38. MLB Timing (5-Pin Interface)

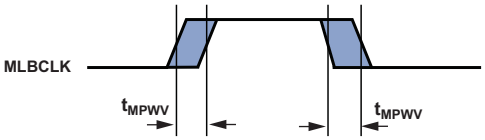

Figure 39. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the hardware reference.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the hardware reference.

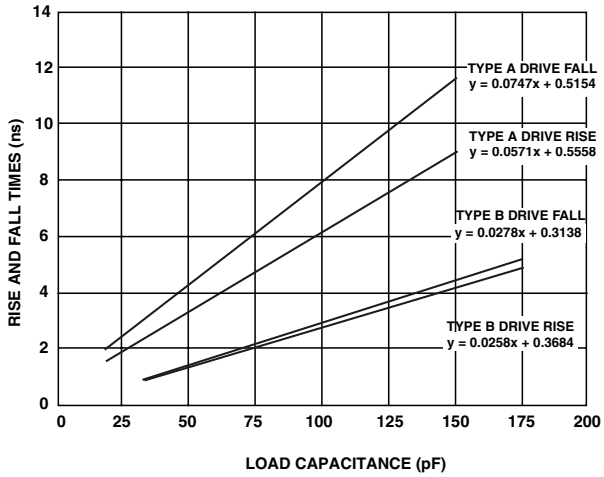

Figure 45. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

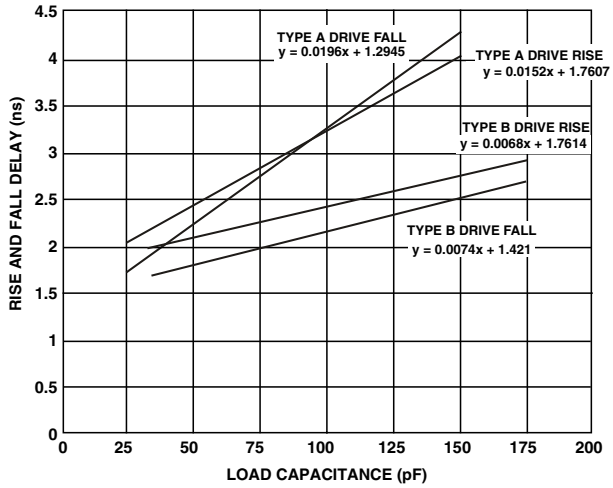

Figure 46. Typical Output Rise/Fall Delay (V_{DD_EXT} = Max)

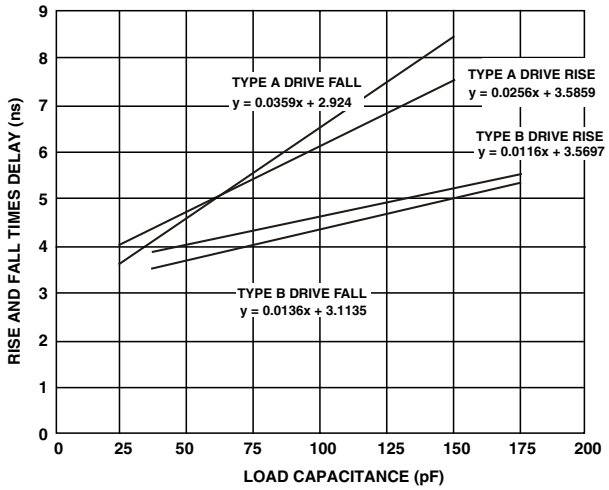

Figure 47. Typical Output Rise/Fall Delay (V_{DD_EXT} = Min)

THERMAL CHARACTERISTICS

The ADSP-2148x processor is rated for performance over the temperature range specified in Operating Conditions on Page 18.

Table 57 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (LQFP_EP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 57.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
NC	1	V_{DD_EXT}	45	DAI_P10	89	V_{DD_INT}	133
$\overline{MS0}$	2	DPI_P08	46	V_{DD_INT}	90	FLAG0	134
NC	3	DPI_P07	47	V_{DD_EXT}	91	FLAG1	135
V_{DD_INT}	4	V_{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V_{DD_INT}	93	GND	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	GND	139
V_{DD_EXT}	8	DPI_P12	52	DAI_P04	96	GND	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V_{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	GND	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V_{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	$\overline{TRST}$	144
ADDR5	13	V_{DD_EXT}	57	DAI_P15	101	GND	145
BOOT_CFG1	14	NC	58	V_{DD_INT}	102	$\overline{EMU}$	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V_{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V_{DD_INT}	105	DATA2	149
NC	18	V_{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V_{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V_{DD_INT}	65	GND	109	V_{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V_{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V_{DD_INT}	68	V_{DD_THD}	112	V_{DD_INT}	156
XTAL	25	NC	69	V_{DD_INT}	113	DATA7	157
ADDR10	26	$\overline{WDTRSTO}$	70	V_{DD_INT}	114	TDI	158
NC	27	NC	71	$\overline{MS1}$	115	NC	159*
V_{DD_EXT}	28	V_{DD_EXT}	72	V_{DD_INT}	116	V_{DD_EXT}	160
V_{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V_{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V_{DD_INT}	34	V_{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V_{DD_INT}	123	DATA14	167
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	36	NC	80	ADDR20	124	DATA13	168
V_{DD_INT}	37	NC	81	ADDR19	125	V_{DD_INT}	169
DPI_P01	38	NC	82	V_{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	NC	171
DPI_P03	40	V_{DD_EXT}	84	ADDR15	128	NC	172
V_{DD_INT}	41	V_{DD_INT}	85	V_{DD_INT}	129	$\overline{RESET}$	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	$\overline{AMI\_WR}$	131	NC	175
DPI_P06	44	DAI_P09	88	$\overline{AMI\_RD}$	132	V_{DD_INT}	176
						GND	177**

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.