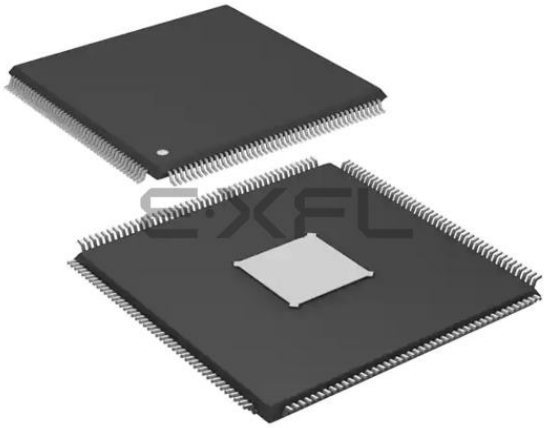

**Welcome to E-XFL.COM**

## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Floating Point |
| Interface | EBI/EMI, DAI, I²C, SPI, SPORT, UART/USART |
| Clock Rate | 400MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 3Mbit |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.10V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP Exposed Pad |
| Supplier Device Package | 176-LQFP-EP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-21488kswz-4b |

# GENERAL DESCRIPTION

The ADSP-2148x SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x, ADSP-2147x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2148x processors are 32-bit/40-bit floating point processors optimized for high performance audio applications with large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1 shows performance benchmarks for the ADSP-2148x processors. Table 2 shows the features of the individual product offerings.

**Table 1. Processor Benchmarks**

| Benchmark Algorithm | Speed (at 400 MHz) | Speed (at 450 MHz) |
|---|---|---|
| 1024 Point Complex FFT (Radix 4, with Reversal) | 23 µs | 20.44 µs |
| FIR Filter (per Tap)[1] | 1.25 ns | 1.1 ns |
| IIR Filter (per Biquad)[1] | 5 ns | 4.43 ns |
| Matrix Multiply (Pipelined) | | |
| [3 × 3] × [3 × 1] | 11.25 ns | 10.0 ns |
| [4 × 4] × [4 × 1] | 20 ns | 17.78 ns |
| Divide (y/×) | 7.5 ns | 6.67 ns |
| Inverse Square Root | 11.25 ns | 10.0 ns |

[1] Assumes two files in multichannel SIMD mode

**Table 2. ADSP-2148x Family Features**

| Feature | ADSP-21483 | ADSP-21486 | ADSP-21487 | ADSP-21488 | ADSP-21489 |
|---|---|---|---|---|---|
| Maximum Instruction Rate | 400 MHz | 400 MHz | 450 MHz | 400 MHz | 450 MHz |
| RAM | 3 Mbits | 5 Mbits | | 2/3 Mbits[1] | 5 Mbits |
| ROM | 4 Mbits | | | No | |
| Audio Decoders in ROM[2] | Yes | | | No | |
| Pulse-Width Modulation | 4 Units (3 Units on 100-Lead Packages) | | | | |
| DTCP Hardware Accelerator | Contact Analog Devices | | | | |
| External Port Interface (SDRAM, AMI)[3] | Yes (16-bit) | AMI Only | Yes (16-bit) | | |
| Serial Ports | 8 | | | | |
| Direct DMA from SPORTs to External Port (External Memory) | Yes | | | | |
| FIR, IIR, FFT Accelerator | Yes | | | | |
| Watchdog Timer | Yes (176-Lead Package Only) | | | | |
| MediaLB Interface | Automotive Models Only | | | | |
| IDP/PDAP | Yes | | | | |
| UART | 1 | | | | |
| DAI (SRU)/DPI (SRU2) | Yes | | | | |
| S/PDIF Transceiver | Yes | | | | |
| SPI | Yes | | | | |
| TWI | 1 | | | | |
| SRC Performance[4] | –128 dB | | | | |
| Thermal Diode | Yes | | | | |
| VISA Support | Yes | | | | |
| Package[3] | 176-Lead LQFP EPAD<br>100-Lead LQFP EPAD | | 176-Lead LQFP EPAD | 176-Lead LQFP EPAD<br>100-Lead LQFP EPAD[5] | |

[1] See Ordering Guide on Page 66.

[2] ROM is factory programmed with latest multichannel audio decoding and post-processing algorithms from Dolby® Labs and DTS®. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[3] The 100-lead packages do not contain an external port. The SDRAM controller pins must be disabled when using this package. For more information, see Pin Function Descriptions on Page 14. The ADSP-21486 processor in the 176-lead package also does not contain a SDRAM controller. For more information, see 176-Lead LQFP_EP Lead Assignment on page 60.

[4] Some models have –140 dB performance. For more information, see Ordering Guide on page 66.

[5] Only available up to 400 MHz. See Ordering Guide on Page 66 for details.

- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

Non-SDRAM external memory address space is shown in Table 5.

**Table 5. External Memory for Non-SDRAM Addresses**

| Bank | Size in Words | Address Range |
|---|---|---|
| Bank 0 | 6M | 0x0020 0000–0x007F FFFF |
| Bank 1 | 8M | 0x0400 0000–0x047F FFFF |
| Bank 2 | 8M | 0x0800 0000–0x087F FFFF |
| Bank 3 | 8M | 0x0C00 0000–0x0C7F FFFF |

### *External Port*

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 176-lead LQFP, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

#### Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and banks 1, 2, and 3 occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

#### SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices at speeds up to $f_{SDCLK}$. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 4M bytes and 256M bytes of memory. SDRAM external memory address space is shown in Table 6. NOTE: this feature is not available on the ADSP-21486 model.

**Table 6. External Memory for SDRAM Addresses**

| Bank | Size in Words | Address Range |
|---|---|---|
| Bank 0 | 62M | 0x0020 0000–0x03FF FFFF |
| Bank 1 | 64M | 0x0400 0000–0x07FF FFFF |
| Bank 2 | 64M | 0x0800 0000–0x0BFF FFFF |
| Bank 3 | 64M | 0x0C00 0000–0x0FFF FFFF |

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on the SDRAM and AMI interfaces.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

#### SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This removes the need to explicitly access the complimentary registers when the data is in external SDRAM memory.

#### VISA and ISA Access to External Memory

The SDRAM controller on the ADSP-2148x processors supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. Table 7 shows the address ranges for instruction fetch in each mode.

**Table 7. External Bank 0 Instruction Fetch**

| Access Type | Size in Words | Address Range |
|---|---|---|
| ISA (NW) | 4M | 0x0020 0000–0x005F FFFF |
| VISA (SW) | 10M | 0x0060 0000–0x00FF FFFF |

### *Pulse-Width Modulation*

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

Details on power consumption and Static and Dynamic current consumption can be found at Total Power Dissipation on Page 20. Also see Operating Conditions on Page 18 for more information.

The following are SVS features.

- SVS is applicable only to 450 MHz models (not applicable to 400 MHz or lower frequency models).
- Each individual SVS device includes a register (SVS_DAT) containing the unique SVS voltage set at the factory, known as $SVS_{NOM}$.
- The $SVS_{NOM}$ value is the intended set voltage for the $V_{DD\_INT}$ voltage regulator.
- No dedicated pins are required for SVS. The TWI serial bus is used to communicate $SVS_{NOM}$ to the voltage regulator.
- Analog Devices recommends a specific voltage regulator design and initialization code sequence that optimizes the power-up sequence.

  The Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) contains the details of the regulator design and the initialization requirements.
- Any differences from the Analog Devices recommended programmable regulator design must be reviewed by Analog Devices to ensure that it meets the voltage accuracy and range requirements.

### *Target Board JTAG Emulator Connector*

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2148x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

## DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

### *Integrated Development Environments (IDEs)*

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

CrossCore Embedded Studio is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

### *EZ-KIT Lite Evaluation Board*

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

### *EZ-KIT Lite Evaluation Kits*

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

### *Software Add-Ins for CrossCore Embedded Studio*

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

### *Board Support Packages for Evaluation Hardware*

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the Product Download area of the product web page.

**Table 11. Pin Descriptions (Continued)**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| MLBCLK[1] | I | | **Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS=48 kHz. When the MLB controller is not used, this pin should be grounded. |
| MLBDAT[1] | I/O/T in 3 pin mode. I in 5 pin mode. | High-Z | **Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded. |
| MLBSIG[1] | I/O/T in 3 pin mode. I in 5 pin mode | High-Z | **Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded. |
| MLBDO[1] | O/T | High-Z | **Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground. |
| MLBSO[1] | O/T | High-Z | **Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground. |
| TDI | I (ipu) | | **Test Data Input (JTAG).** Provides serial data for the boundary scan logic. |
| TDO | O/T | High-Z | **Test Data Output (JTAG).** Serial scan output of the boundary scan path. |
| TMS | I (ipu) | | **Test Mode Select (JTAG).** Used to control the test state machine. |
| TCK | I | | **Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device. |
| $\overline{\text{TRST}}$ | I (ipu) | | **Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. |
| $\overline{\text{EMU}}$ | O (O/D, ipu) | High-Z | **Emulation Status.** Must be connected to the ADSP-2148x Analog Devices DSP Tools product line of JTAG emulators target board connector only. |

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full $V_{DD\_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

**Table 11. Pin Descriptions (Continued)**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| $CLK\_CFG_{1-0}$ | I | | **Core to CLKIN Ratio Control.** These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are:<br>00 = 8:1<br>01 = 32:1<br>10 = 16:1<br>11 = reserved |
| CLKIN | I | | **Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency. |
| XTAL | O | | **Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal. |
| $\overline{\text{RESET}}$ | I | | **Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up. |
| $\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$ | I/O (ipu) | | **Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the hardware reference. |
| $BOOT\_CFG_{2-0}$ | I | | **Boot Configuration Select.** These pins select the boot mode for the processor (see Table 9). The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is asserted. |

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full $V_{DD\_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

[1] The MLB pins are only available on the automotive models.

**Table 12. Pin List, Power and Ground**

| Name | Type | Description |
|---|---|---|
| $V_{DD\_INT}$ | P | **Internal Power Supply** |
| $V_{DD\_EXT}$ | P | **I/O Power Supply** |
| GND[1] | G | **Ground** |
| $V_{DD\_THD}$ | P | **Thermal Diode Power Supply**. When not used, this pin can be left floating. |

[1] The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be robustly connected to the GND plane in the PCB for best electrical and thermal performance. No separate GND pins are provided in the package.

# SPECIFICATIONS

## OPERATING CONDITIONS

| Parameter[1] | Description | 300 MHz / 350 MHz / 400 MHz | | | 450 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nominal | Max | Min | Nominal | Max | |
| $V_{DD\_INT}$[2] | Internal (Core) Supply Voltage | 1.05 | 1.1 | 1.15 | $SVS_{NOM}$ – 25 mV | 1.0 – 1.15 | $SVS_{NOM}$ + 25 mV | V |
| $V_{DD\_EXT}$ | External (I/O) Supply Voltage | 3.13 | | 3.47 | 3.13 | | 3.47 | V |
| $V_{DD\_THD}$ | Thermal Diode Supply Voltage | 3.13 | | 3.47 | 3.13 | | 3.47 | V |
| $V_{IH}$[3] | High Level Input Voltage @ $V_{DD\_EXT}$ = Max | 2.0 | | 3.6 | 2.0 | | 3.6 | V |
| $V_{IL}$[3] | Low Level Input Voltage @ $V_{DD\_EXT}$ = Min | –0.3 | | 0.8 | –0.3 | | 0.8 | V |
| $V_{IH\_CLKIN}$[4] | High Level Input Voltage @ $V_{DD\_EXT}$ = Max | 2.2 | | $V_{DD\_EXT}$ | 2.2 | | $V_{DD\_EXT}$ | V |
| $V_{IL\_CLKIN}$ | Low Level Input Voltage @ $V_{DD\_EXT}$ = Min | –0.3 | | +0.8 | –0.3 | | +0.8 | V |
| $T_J$ | Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C | 0 | | 110 | 0 | | 115 | °C |
| $T_J$ | Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C | –40 | | 125 | NA | | NA | °C |
| $T_J$ | Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C | 0 | | 110 | 0 | | 115 | °C |
| $T_J$ | Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C | –40 | | 125 | NA | | NA | °C |

[1] Specifications subject to change without notice.

[2] $SVS_{NOM}$ refers to the nominal SVS voltage which is set between 1.0 V and 1.15 V at the factory for each individual device. Only the unique $SVS_{NOM}$ value in each chip may be used for 401 MHz to 450 MHz operation of that chip. This spec lists the possible range of the $SVS_{NOM}$ values for all devices. The initial VDD_INT voltage at power on is 1.1 V nominal and it transitions to SVS programmed voltage as outlined in Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357).

[3] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[4] Applies to input pins CLKIN, WDT_CLKIN.

### *Total Power Dissipation*

The information in this section should be augmented with the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348).

Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature ($T_J$) and core voltage ($V_{DD\_INT}$).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13).

     Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

**Table 13. Activity Scaling Factors (ASF)[1]**

| Activity | Scaling Factor (ASF) |
|---|---|
| Idle | 0.29 |
| Low | 0.53 |
| Medium Low | 0.61 |
| Medium High | 0.77 |
| Peak Typical (50:50)[2] | 0.85 |
| Peak Typical (60:40)[2] | 0.93 |
| Peak Typical (70:30)[2] | 1.00 |
| High Typical | 1.16 |
| High | 1.25 |
| Peak | 1.31 |

[1] See the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for more information on the explanation of the power vectors specific to the ASF table.

[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

**Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]**

| | $V_{DD\_INT}$ (V) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $T_J$ (°C) | 0.975 V | 1.0 V | 1.025 V | 1.05 V | 1.075 V | 1.10 V | 1.125 V | 1.15 V | 1.175 V |
| –45 | 68 | 77 | 86 | 96 | 107 | 118 | 131 | 144 | 159 |
| –35 | 74 | 83 | 92 | 103 | 114 | 126 | 140 | 154 | 170 |
| –25 | 82 | 92 | 101 | 113 | 125 | 138 | 153 | 168 | 185 |
| –15 | 94 | 104 | 115 | 127 | 140 | 155 | 171 | 187 | 205 |
| –5 | 109 | 121 | 133 | 147 | 161 | 177 | 194 | 212 | 233 |
| +5 | 129 | 142 | 156 | 171 | 188 | 206 | 225 | 245 | 268 |
| +15 | 152 | 168 | 183 | 201 | 219 | 240 | 261 | 285 | 309 |
| +25 | 182 | 199 | 216 | 237 | 257 | 280 | 305 | 331 | 360 |
| +35 | 217 | 237 | 256 | 279 | 303 | 329 | 358 | 388 | 420 |
| +45 | 259 | 282 | 305 | 331 | 359 | 389 | 421 | 455 | 492 |
| +55 | 309 | 334 | 361 | 391 | 423 | 458 | 495 | 533 | 576 |
| +65 | 369 | 398 | 429 | 464 | 500 | 539 | 582 | 626 | 675 |
| +75 | 437 | 471 | 506 | 547 | 588 | 633 | 682 | 731 | 789 |
| +85 | 519 | 559 | 599 | 645 | 693 | 746 | 802 | 860 | 926 |
| +95 | 615 | 662 | 707 | 761 | 816 | 877 | 942 | 1007 | 1083 |
| +105 | 727 | 779 | 833 | 897 | 958 | 1026 | 1103 | 1179 | 1266 |
| +115 | 853 | 914 | 975 | 1047 | 1119 | 1198 | 1285 | 1372 | 1473 |
| +125 | 997 | 1067 | 1138 | 1219 | 1305 | 1397 | 1498 | 1601 | 1716 |

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

### *Reset*

**Table 21. Reset**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{WRST}$[1] | $\overline{\text{RESET}}$ Pulse Width Low | $4 \times t_{CK}$ | | ns |
| $t_{SRST}$ | $\overline{\text{RESET}}$ Setup Before CLKIN Low | 8 | | ns |

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 μσ while $\overline{\text{RESET}}$ is low, assuming stable $V_{DD}$ and CLKIN (not including start-up time of external clock oscillator).

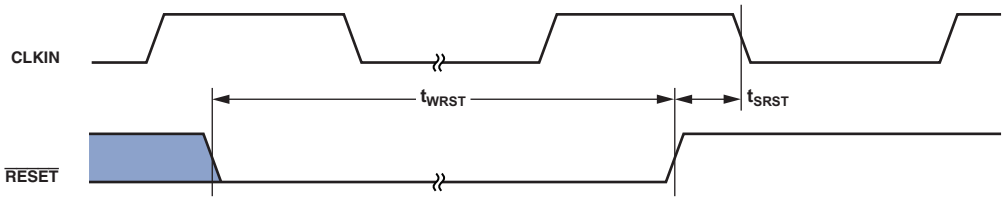


*Figure 8. Reset*

### *Running Reset*

The following timing specification applies to $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

**Table 22. Running Reset**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{WRUNRST}$ | Running $\overline{\text{RESET}}$ Pulse Width Low | $4 \times t_{CK}$ | | ns |
| $t_{SRUNRST}$ | Running $\overline{\text{RESET}}$ Setup Before CLKIN High | 8 | | ns |

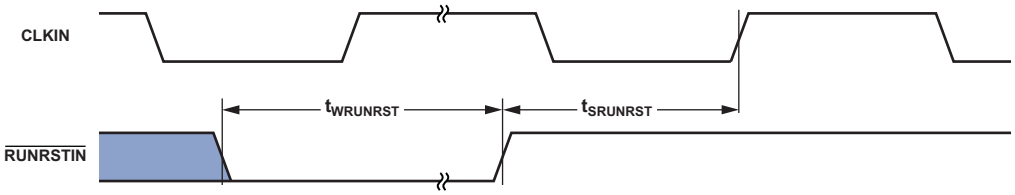


*Figure 9. Running Reset*

### *Timer PWM_OUT Cycle Timing*

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

**Table 25. Timer PWM_OUT Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristic* | | | | |
| $t_{PWMO}$ | Timer Pulse Width Output | $2 \times t_{PCLK} - 1.2$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns |

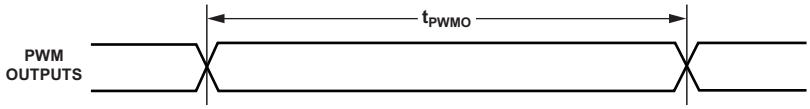


*Figure 12. Timer PWM_OUT Timing*

### *Timer WDTH_CAP Timing*

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse-width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

**Table 26. Timer Width Capture Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{PWI}$ | Timer Pulse Width | $2 \times t_{PCLK}$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns |

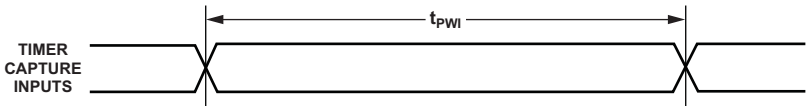


*Figure 13. Timer Width Capture Timing*

### *Watchdog Timer Timing*

**Table 27. Watchdog Timer Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{WDTCLKPER}$ | | 100 | 1000 | ns |
| Switching Characteristics | | | | |
| $t_{RST}$ | WDT Clock Rising Edge to Watchdog Timer $\overline{\text{RESET}}$ Falling Edge | 3 | 6.4 | ns |
| $t_{RSTPW}$ | Reset Pulse Width | $64 \times t_{WDTCLKPER}$ | | ns |

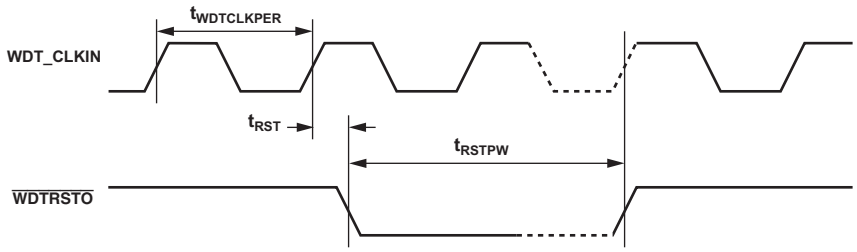


*Figure 14. Watchdog Timer Timing*

### *Pin to Pin Direct Routing (DAI and DPI)*

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

**Table 28. DAI/DPI Pin to Pin Routing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{DPIO}$ | Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid | 1.5 | 12 | ns |

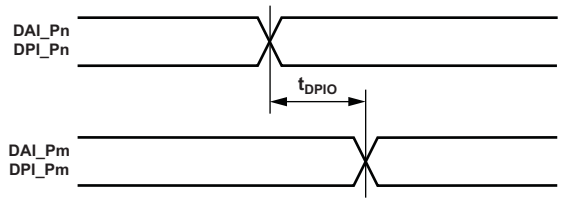


*Figure 15. DAI Pin to Pin Direct Routing*

### *Precision Clock Generator (Direct Pin Routing)*

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

**Table 29. Precision Clock Generator (Direct Pin Routing)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{PCGIW}$ | Input Clock Period | $t_{PCLK} \times 4$ | | ns |
| $t_{STRIG}$ | PCG Trigger Setup Before Falling Edge of PCG Input Clock | 4.5 | | ns |
| $t_{HTRIG}$ | PCG Trigger Hold After Falling Edge of PCG Input Clock | 3 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DPCGIO}$ | PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock | 2.5 | 10 | ns |
| $t_{DTRIGCLK}$ | PCG Output Clock Delay After PCG Trigger | $2.5 + (2.5 \times t_{PCGIP})$ | $10 + (2.5 \times t_{PCGIP})$ | ns |
| $t_{DTRIGFS}$ | PCG Frame Sync Delay After PCG Trigger | $2.5 + ((2.5 + D - PH) \times t_{PCGIP})$ | $10 + ((2.5 + D - PH) \times t_{PCGIP})$ | ns |
| $t_{PCGOW}$[1] | Output Clock Period | $2 \times t_{PCGIP} - 1$ | | ns |

D = FSxDIV, PH = FSxPHASE. For more information, see the "Precision Clock Generators" chapter in the hardware reference.

[1] Normal mode of operation.

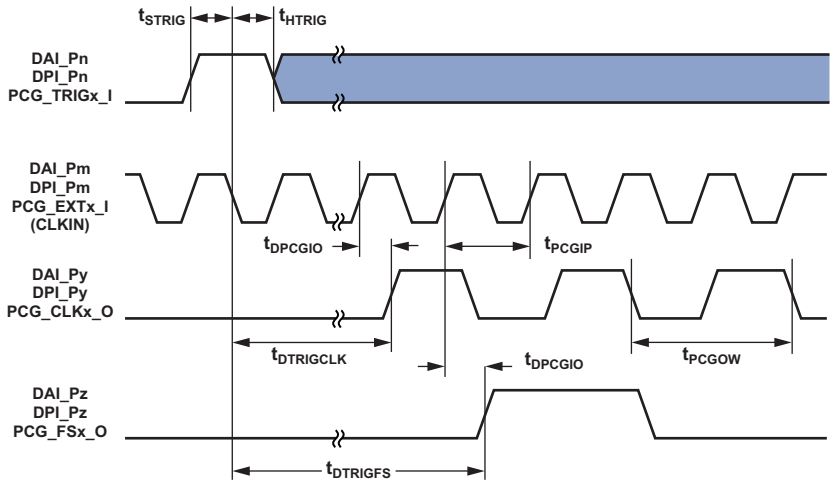


*Figure 16. Precision Clock Generator (Direct Pin Routing)*

### *Sample Rate Converter—Serial Output Port*

For the serial output port, the frame sync is an input, and it should meet setup and hold times with regard to SCLK on the output port. The serial data output has a hold time and delay specification with regard to serial clock. Note that serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

**Table 42. ASRC, Serial Output Port**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SRCSFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{SRCCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{SRCTDD}$[1] | Transmit Data Delay After Serial Clock Falling Edge | | 9.9 | ns |
| $t_{SRCTDH}$[1] | Transmit Data Hold After Serial Clock Falling Edge | 1 | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

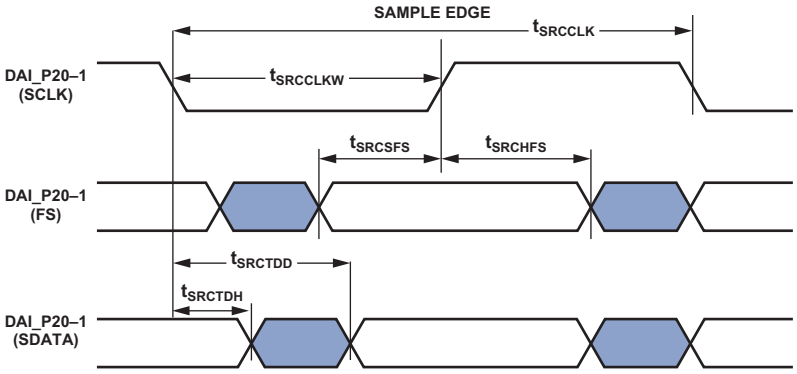


*Figure 28. ASRC Serial Output Port Timing*

### *Pulse-Width Modulation Generators (PWM)*

The following timing specifications apply when the ADDR23–8/DPI_14–1 pins are configured as PWM.

**Table 43. Pulse-Width Modulation (PWM) Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{PWMW}$ | PWM Output Pulse Width | $t_{PCLK} - 2$ | $(2^{16} - 2) \times t_{PCLK}$ | ns |
| $t_{PWMP}$ | PWM Output Period | $2 \times t_{PCLK} - 1.5$ | $(2^{16} - 1) \times t_{PCLK}$ | ns |

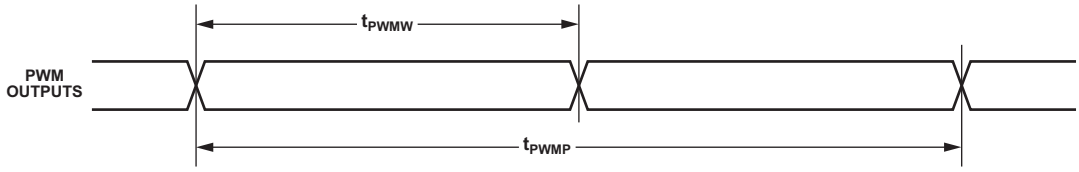


*Figure 29. PWM Timing*

### *S/PDIF Transmitter*

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

#### S/PDIF Transmitter-Serial Input Waveforms

Figure 30 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

**Table 44. S/PDIF Transmitter Right-Justified Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{RJD}$ | Frame Sync to MSB Delay in Right-Justified Mode | | |
| | 16-Bit Word Mode | 16 | SCLK |
| | 18-Bit Word Mode | 14 | SCLK |
| | 20-Bit Word Mode | 12 | SCLK |
| | 24-Bit Word Mode | 8 | SCLK |

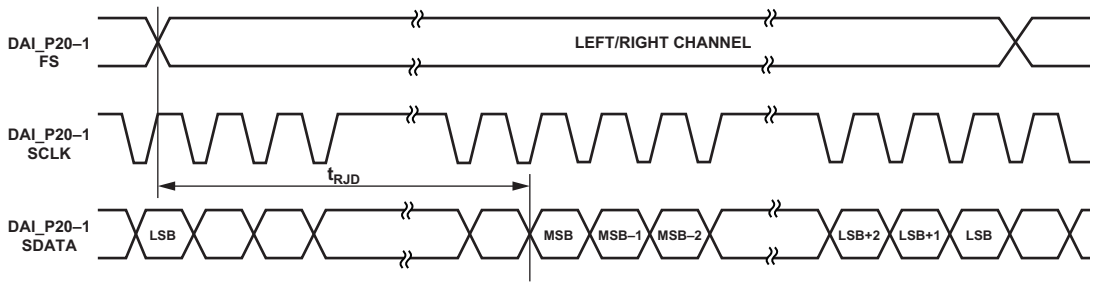


*Figure 30. Right-Justified Mode*

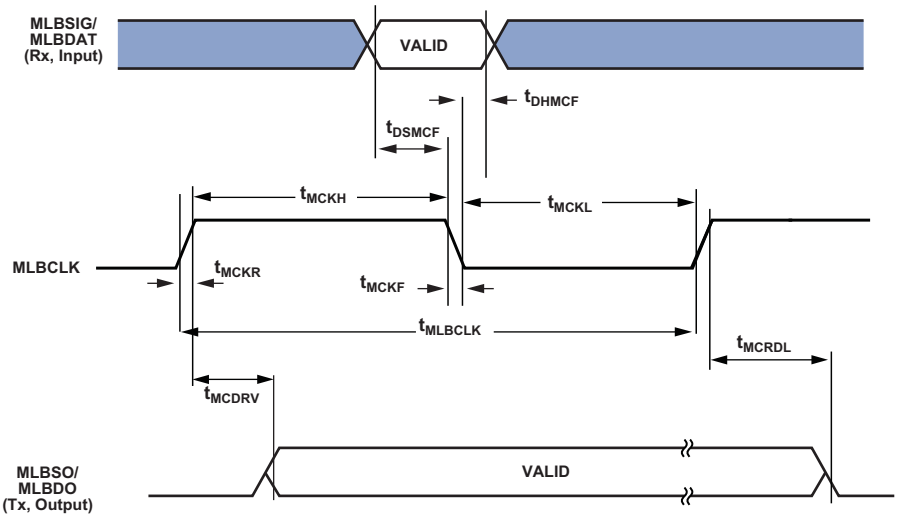


*Figure 38. MLB Timing (5-Pin Interface)*

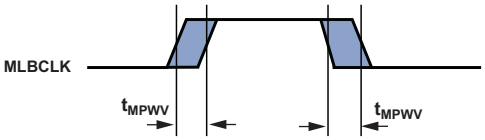


*Figure 39. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing*

### *Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing*

For information on the UART port receive and transmit operations, see the hardware reference.

### *2-Wire Interface (TWI)—Receive and Transmit Timing*

For information on the TWI receive and transmit operations, see the hardware reference.

Note that the thermal characteristics values provided in Table 56 and Table 57 are modeled values.

**Table 56. Thermal Characteristics for 100-Lead LQFP_EP**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Airflow = 0 m/s | 17.8 | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 15.4 | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 14.6 | °C/W |
| $\theta_{JC}$ | | 2.4 | °C/W |
| $\Psi_{JT}$ | Airflow = 0 m/s | 0.24 | °C/W |
| $\Psi_{JMT}$ | Airflow = 1 m/s | 0.37 | °C/W |
| $\Psi_{JMT}$ | Airflow = 2 m/s | 0.51 | °C/W |

**Table 57. Thermal Characteristics for 176-Lead LQFP_EP**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Airflow = 0 m/s | 16.9 | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 14.6 | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 13.8 | °C/W |
| $\theta_{JC}$ | | 2.3 | °C/W |
| $\Psi_{JT}$ | Airflow = 0 m/s | 0.21 | °C/W |
| $\Psi_{JMT}$ | Airflow = 1 m/s | 0.32 | °C/W |
| $\Psi_{JMT}$ | Airflow = 2 m/s | 0.41 | °C/W |

### *Thermal Diode*

The ADSP-2148x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

$n$ = multiplication factor close to 1, depending on process variations

$k$ = Boltzmann's constant

$T$ = temperature (°C)

$q$ = charge of the electron

$N$ = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

Table 58 contains the thermal diode specifications using the transistor model.

**Table 58. Thermal Diode Parameters – Transistor Model[1]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{FW}$[2] | Forward Bias Current | 10 | | 300 | µA |
| $I_E$ | Emitter Current | 10 | | 300 | µA |
| $n_Q$[3, 4] | Transistor Ideality | 1.012 | 1.015 | 1.017 | |
| $R_T$[3, 5] | Series Resistance | 0.12 | 0.2 | 0.28 | Ω |

[1] See Engineer-to-Engineer Note Using the On-Chip Thermal Diode on Analog Devices Processors (EE-346).
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where $I_S$ = saturation current, q = electronic charge, $V_{BE}$ = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
[5] The series resistance ($R_T$) can be used for more accurate readings as needed.

Figure 48 shows the top view of the 100-lead LQFP_EP lead configuration. Figure 49 shows the bottom view of the 100-lead LQFP_EP lead configuration.

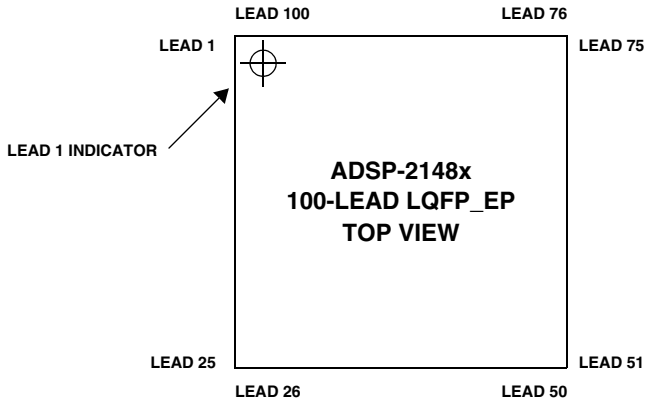


*Figure 48. 100-Lead LQFP_EP Lead Configuration (Top View)*

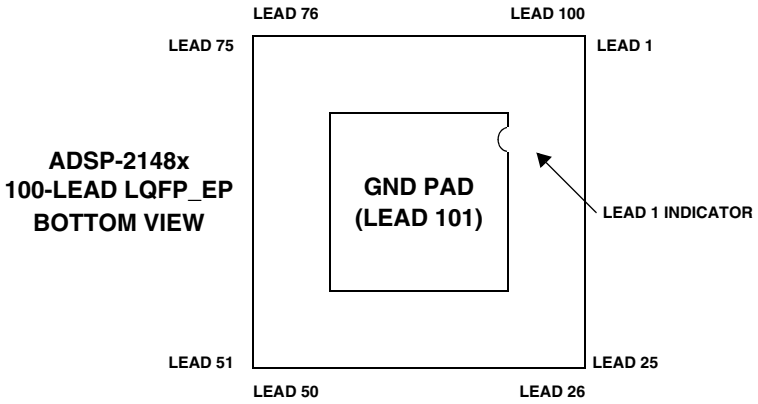


*Figure 49. 100-Lead LQFP_EP Lead Configuration (Bottom View)*

## 176-LEAD LQFP_EP LEAD ASSIGNMENT

**Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)**

| Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. |
|---|---|---|---|---|---|---|---|
| NC | 1 | $V_{DD\_EXT}$ | 45 | DAI_P10 | 89 | $V_{DD\_INT}$ | 133 |
| $\overline{MS0}$ | 2 | DPI_P08 | 46 | $V_{DD\_INT}$ | 90 | FLAG0 | 134 |
| NC | 3 | DPI_P07 | 47 | $V_{DD\_EXT}$ | 91 | FLAG1 | 135 |
| $V_{DD\_INT}$ | 4 | $V_{DD\_INT}$ | 48 | DAI_P20 | 92 | FLAG2 | 136 |
| CLK_CFG1 | 5 | DPI_P09 | 49 | $V_{DD\_INT}$ | 93 | GND | 137 |
| ADDR0 | 6 | DPI_P10 | 50 | DAI_P08 | 94 | FLAG3 | 138 |
| BOOT_CFG0 | 7 | DPI_P11 | 51 | DAI_P14 | 95 | GND | 139 |
| $V_{DD\_EXT}$ | 8 | DPI_P12 | 52 | DAI_P04 | 96 | GND | 140 |
| ADDR1 | 9 | DPI_P13 | 53 | DAI_P18 | 97 | $V_{DD\_EXT}$ | 141 |
| ADDR2 | 10 | DPI_P14 | 54 | DAI_P17 | 98 | GND | 142 |
| ADDR3 | 11 | DAI_P03 | 55 | DAI_P16 | 99 | $V_{DD\_INT}$ | 143 |
| ADDR4 | 12 | NC | 56 | DAI_P12 | 100 | $\overline{TRST}$ | 144 |
| ADDR5 | 13 | $V_{DD\_EXT}$ | 57 | DAI_P15 | 101 | GND | 145 |
| BOOT_CFG1 | 14 | NC | 58 | $V_{DD\_INT}$ | 102 | $\overline{EMU}$ | 146 |
| GND | 15 | NC | 59 | DAI_P11 | 103 | DATA0 | 147 |
| ADDR6 | 16 | NC | 60 | $V_{DD\_EXT}$ | 104 | DATA1 | 148 |
| ADDR7 | 17 | NC | 61 | $V_{DD\_INT}$ | 105 | DATA2 | 149 |
| NC | 18 | $V_{DD\_INT}$ | 62 | BOOT_CFG2 | 106 | DATA3 | 150 |
| NC | 19 | NC | 63 | $V_{DD\_INT}$ | 107 | TDO | 151 |
| ADDR8 | 20 | NC | 64 | AMI_ACK | 108 | DATA4 | 152 |
| ADDR9 | 21 | $V_{DD\_INT}$ | 65 | GND | 109 | $V_{DD\_EXT}$ | 153 |
| CLK_CFG0 | 22 | NC | 66 | THD_M | 110 | DATA5 | 154 |
| $V_{DD\_INT}$ | 23 | NC | 67 | THD_P | 111 | DATA6 | 155 |
| CLKIN | 24 | $V_{DD\_INT}$ | 68 | $V_{DD\_THD}$ | 112 | $V_{DD\_INT}$ | 156 |
| XTAL | 25 | NC | 69 | $V_{DD\_INT}$ | 113 | DATA7 | 157 |
| ADDR10 | 26 | $\overline{WDTRSTO}$ | 70 | $V_{DD\_INT}$ | 114 | TDI | 158 |
| NC | 27 | NC | 71 | $\overline{MS1}$ | 115 | NC | 159* |
| $V_{DD\_EXT}$ | 28 | $V_{DD\_EXT}$ | 72 | $V_{DD\_INT}$ | 116 | $V_{DD\_EXT}$ | 160 |
| $V_{DD\_INT}$ | 29 | DAI_P07 | 73 | WDT_CLKO | 117 | DATA8 | 161 |
| ADDR11 | 30 | DAI_P13 | 74 | WDT_CLKIN | 118 | DATA9 | 162 |
| ADDR12 | 31 | DAI_P19 | 75 | $V_{DD\_EXT}$ | 119 | DATA10 | 163 |
| ADDR17 | 32 | DAI_P01 | 76 | ADDR23 | 120 | TCK | 164 |
| ADDR13 | 33 | DAI_P02 | 77 | ADDR22 | 121 | DATA11 | 165 |
| $V_{DD\_INT}$ | 34 | $V_{DD\_INT}$ | 78 | ADDR21 | 122 | DATA12 | 166 |
| ADDR18 | 35 | NC | 79 | $V_{DD\_INT}$ | 123 | DATA14 | 167 |
| $\overline{RESETOUT}$/$\overline{RUNRSTIN}$ | 36 | NC | 80 | ADDR20 | 124 | DATA13 | 168 |
| $V_{DD\_INT}$ | 37 | NC | 81 | ADDR19 | 125 | $V_{DD\_INT}$ | 169 |
| DPI_P01 | 38 | NC | 82 | $V_{DD\_EXT}$ | 126 | DATA15 | 170 |
| DPI_P02 | 39 | NC | 83 | ADDR16 | 127 | NC | 171 |
| DPI_P03 | 40 | $V_{DD\_EXT}$ | 84 | ADDR15 | 128 | NC | 172 |
| $V_{DD\_INT}$ | 41 | $V_{DD\_INT}$ | 85 | $V_{DD\_INT}$ | 129 | $\overline{RESET}$ | 173 |
| DPI_P05 | 42 | DAI_P06 | 86 | ADDR14 | 130 | TMS | 174 |
| DPI_P04 | 43 | DAI_P05 | 87 | $\overline{AMI\_WR}$ | 131 | NC | 175 |
| DPI_P06 | 44 | DAI_P09 | 88 | $\overline{AMI\_RD}$ | 132 | $V_{DD\_INT}$ | 176 |
| | | | | | | GND | 177** |

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

Figure 50 shows the top view of the 176-lead LQFP_EP lead configuration. Figure 51 shows the bottom view of the 176-lead LQFP_EP lead configuration.

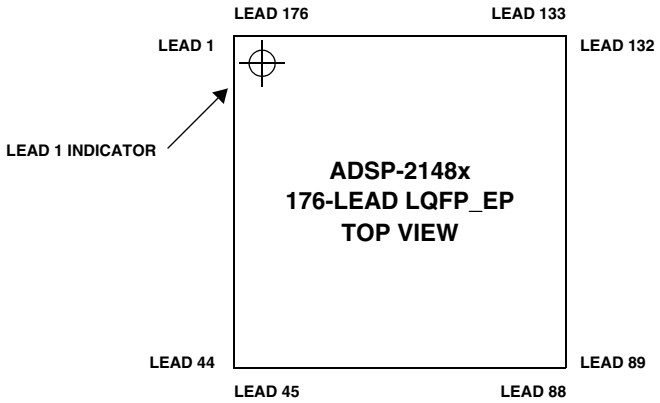


*Figure 50. 176-Lead LQFP_EP Lead Configuration (Top View)*

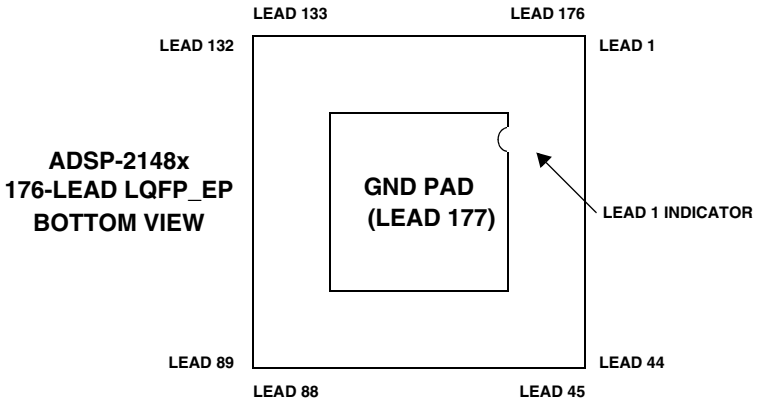


*Figure 51. 176-Lead LQFP_EP Lead Configuration (Bottom View)*

# OUTLINE DIMENSIONS

The ADSP-2148x processors are available in 100-lead and 176-lead LQFP_EP RoHS compliant packages.

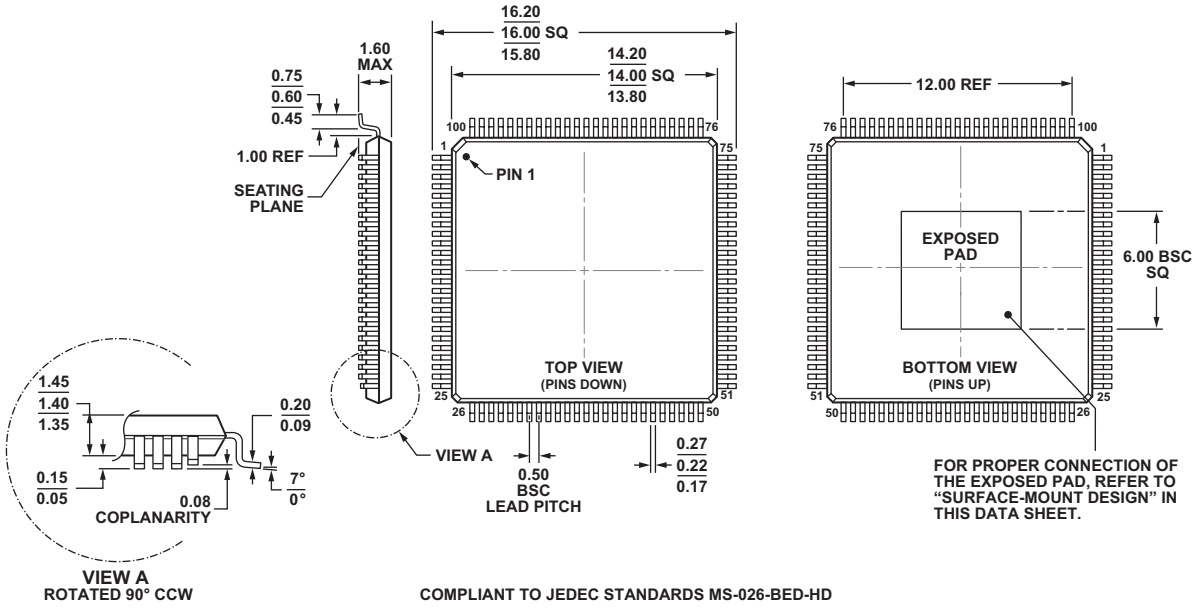


*Figure 52. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]*
*(SW-100-2)*
*Dimensions shown in millimeters*

[1] For information relating to the exposed pad on the SW-100-2 package, see the table endnote on Page 58.

| Model[1] | Notes | Temperature Range[2] | RAM | Processor Instruction Rate (Max) | Package Description | Package Option |
|---|---|---|---|---|---|---|
| ADSP-21487KSWZ-2B | 3 | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-2BB | 3 | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-3B | 3 | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-3BB | 3 | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-4B | 3 | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-4BB | 3 | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-5B | 3, 4 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-5BB | 3, 4 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP21487KSWZ5BBRL | 5 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-3A | | –40°C to +85°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3A | | 0°C to +70°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3A1 | 6 | 0°C to +70°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3B | | 0°C to +70°C | 3 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-3B | | –40°C to +85°C | 3 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488KSWZ-4A | | 0°C to +70°C | 3 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488BSWZ-4A | | –40°C to +85°C | 3 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-4B | | 0°C to +70°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-4B | | –40°C to +85°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488KSWZ-4B1 | 6 | 0°C to +70°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-3A | | 0°C to +70°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489BSWZ-3A | | –40°C to +85°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489KSWZ-3B | | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489BSWZ-3B | | –40°C to +85°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-4A | | 0°C to +70°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489BSWZ-4A | | –40°C to +85°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489KSWZ-4B | | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489BSWZ-4B | | –40°C to +85°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-5B | 4 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature ($T_J$) specification, which is the only temperature specification.

[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

[4] See Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for operating ADSP-2148x processors at 450 MHz.

[5] RL = Tape and Reel.

[6] This product contains a –140 dB sample rate converter.