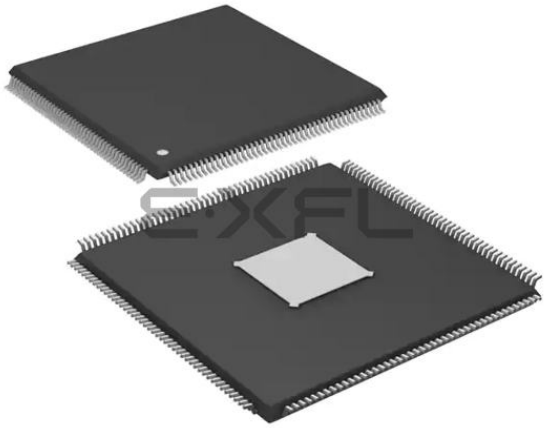

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	EBI/EMI, DAI, I²C, SPI, SPORT, UART/USART
Clock Rate	350MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21489bswz-3b

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REVISION HISTORY

5/2016—Rev. C to Rev. D

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The diagram on Page 1 shows the two clock domains that make up the ADSP-2148x processors. The core clock domain contains the following features:

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (5 Mbit) and mask-programmable ROM (4 Mbit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-2148x on Page 1 also shows the peripheral clock domain (also known as the I/O processor) which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 memory-to-memory (MTM) unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP/PDAP) for serial and parallel interconnects, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface (TWI), one UART, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG), pulse width modulation (PWM), and a flexible signal routing unit (DPI SRU2).

As shown in the SHARC core block diagram on Page 5, the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz.

FAMILY CORE ARCHITECTURE

The ADSP-2148x is code compatible at the assembly level with the ADSP-2147x, ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2148x shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The ADSP-2148x contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEx is always active, and PEy may be enabled by setting the PEYEN mode bit in the MODE1 register. SIMD mode allows the processor to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

SIMD mode also affects the way data is transferred between memory and the processing elements because twice the data bandwidth is required to sustain computational operation in the processing elements. Therefore, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each memory or register file access.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle and are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Timer

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

Non-SDRAM external memory address space is shown in Table 5.

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	6M	0x0020 0000–0x007F FFFF
Bank 1	8M	0x0400 0000–0x047F FFFF
Bank 2	8M	0x0800 0000–0x087F FFFF
Bank 3	8M	0x0C00 0000–0x0C7F FFFF

External Port

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 176-lead LQFP, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and banks 1, 2, and 3 occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices at speeds up to f_{SDCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 4M bytes and 256M bytes of memory. SDRAM external memory address space is shown in Table 6. NOTE: this feature is not available on the ADSP-21486 model.

Table 6. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on the SDRAM and AMI interfaces.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This removes the need to explicitly access the complimentary registers when the data is in external SDRAM memory.

VISA and ISA Access to External Memory

The SDRAM controller on the ADSP-2148x processors supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. Table 7 shows the address ranges for instruction fetch in each mode.

Table 7. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000–0x005F FFFF
VISA (SW)	10M	0x0060 0000–0x00FF FFFF

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see Analog Devices JTAG Emulation Technical Reference (EE-68). This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2148x architecture and functionality. For detailed information on the ADSP-2148x family core architecture and instruction set, refer to the programming reference manual.

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http:\\www.analog.com\circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23–0}$	I/O/T (ipu)	High-Z/ driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, and FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in external memory interface mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23–4}$ pins for parallel input data.
$DATA_{15–0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), and $FLAGS_{7–0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0–1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information, see the hardware reference.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.**
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.**

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{SDRAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
SDCKE	O/T (ipu)	High-Z/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (ipu)	High-Z/ driven high	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's ADDR10 pin only during SDRAM accesses.
SDDQM	O/T (ipu)	High-Z/ driven high	**DQM Data Mask.** SDRAM Input mask signal for write accesses and output mask signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The SDRAM output buffers are placed in a High-Z state when DQM is sampled high during a read cycle. SDDQM is driven high from reset de-assertion until SDRAM initialization completes. Afterwards it is driven low irrespective of whether any SDRAM accesses occur or not.
SDCLK	O/T (ipd)	High-Z/ driving	**SDRAM Clock Output.** Clock driver for this pin differs from all other clock drivers. See Figure 41 on Page 55. For models in the 100-lead package, the SDRAM interface should be disabled to avoid unnecessary power switching by setting the DSDCTL bit in SDCTL register. For more information, see the hardware reference.
DAI _P_{20-1}	I/O/T (ipu)	High-Z	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins.
DPI _P_{14-1}	I/O/T (ipu)	High-Z	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins.
WDT_CLKIN	I		**Watchdog Timer Clock Input.** This pin should be pulled low when not used.
WDT_CLKO	O		**Watchdog Resonator Pad Output.**
$\overline{\text{WDTRSTO}}$	O (ipu)		**Watchdog Timer Reset Out.**
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
MLBCLK[1]	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS=48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT[1]	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG[1]	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO[1]	O/T	High-Z	**Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
MLBSO[1]	O/T	High-Z	**Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{\text{EMU}}$	O (O/D, ipu)	High-Z	**Emulation Status.** Must be connected to the ADSP-2148x Analog Devices DSP Tools product line of JTAG emulators target board connector only.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	300 MHz / 350 MHz / 400 MHz			450 MHz			Unit
		Min	Nominal	Max	Min	Nominal	Max	
V_{DD_INT}[2]	Internal (Core) Supply Voltage	1.05	1.1	1.15	SVS_{NOM} – 25 mV	1.0 – 1.15	SVS_{NOM} + 25 mV	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13		3.47	3.13		3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13		3.47	3.13		3.47	V
V_{IH}[3]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0		3.6	2.0		3.6	V
V_{IL}[3]	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		0.8	–0.3		0.8	V
V_{IH_CLKIN}[4]	High Level Input Voltage @ V_{DD_EXT} = Max	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		+0.8	–0.3		+0.8	V
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C

[1] Specifications subject to change without notice.

[2] SVS_{NOM} refers to the nominal SVS voltage which is set between 1.0 V and 1.15 V at the factory for each individual device. Only the unique SVS_{NOM} value in each chip may be used for 401 MHz to 450 MHz operation of that chip. This spec lists the possible range of the SVS_{NOM} values for all devices. The initial VDD_INT voltage at power on is 1.1 V nominal and it transitions to SVS programmed voltage as outlined in Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357).

[3] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[4] Applies to input pins CLKIN, WDT_CLKIN.

Table 15. Dynamic Current in CCLK Domain—$I_{DD\_INT\_DYNAMIC}$ (mA, with ASF = 1.0)[1, 2]

f_{CCLK} (MHz)	V_{DD_INT} (V)								
	0.975 V	1.0 V	1.025 V	1.05 V	1.075 V	1.10 V	1.125 V	1.15 V	1.175 V
100	76	77	81	84	87	88	90	92	95
150	117	119	123	126	130	133	136	139	144
200	153	156	161	165	170	174	179	183	188
250	190	195	201	207	212	217	223	229	235
300	227	233	240	246	253	260	266	273	280
350	263	272	278	286	294	302	309	318	325
400	300	309	317	326	335	344	352	361	370
450	339	349	356	365	374	385	394	405	415

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 19.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 18.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 16 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 16. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +3.6 V
Thermal Diode Supply Voltage (V_{DD_THD})	–0.3 V to +3.6 V
Input Voltage	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DD_EXT} +0.5 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 56.

PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-2148x processors. For a complete listing of product availability, see Ordering Guide on Page 66.

Figure 3. Typical Package Brand

Table 17. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Option
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Non automotive only. For branding information specific to automotive products, contact Analog Devices Inc.

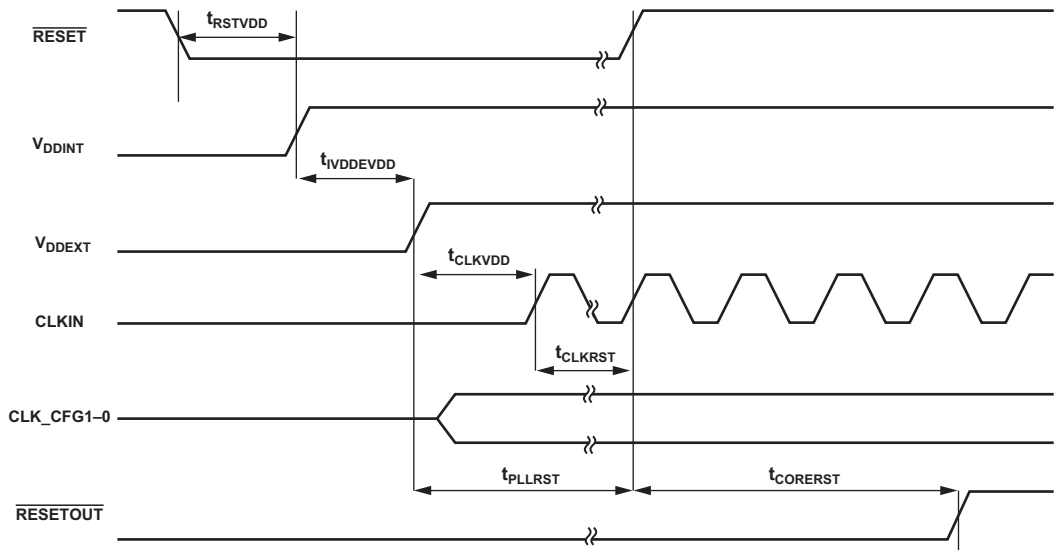

Figure 5. Power-Up Sequencing

Clock Input

Table 20. Clock Input

Parameter		300 MHz Min	300 MHz Max	350 MHz Min	350 MHz Max	400 MHz Min	400 MHz Max	450 MHz Min	450 MHz Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	26.66[1]	100[2]	22.8[1]	100[2]	20[1]	100[2]	17.75[1]	100[2]	ns
t_{CKL}	CLKIN Width Low	13	45	11	45	10	45	8.875	45	ns
t_{CKH}	CLKIN Width High	13	45	11	45	10	45	8.875	45	ns
t_{CKRF}[3]	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns
t_{CCLK}[4]	CCLK Period	3.33	10	2.85	10	2.5	10	2.22	10	ns
f_{VCO}[5]	VCO Frequency	200	800	200	800	200	800	200	900	MHz
t_{CKJ}[6, 7]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	–250	+250	ps

[1] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLK_CFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Guaranteed by simulation but not tested on silicon.
[4] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.
[5] See Figure 4 on Page 22 for VCO diagram.
[6] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[7] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

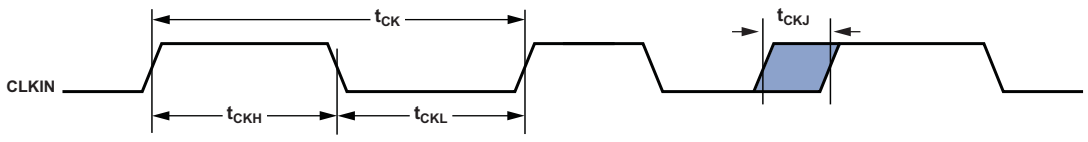

Figure 6. Clock Input

SDRAM Interface Timing (166 MHz SDCLK)

The maximum frequency for SDRAM is 166 MHz. For information on SDRAM frequency and programming, see the hardware reference, Engineer-to-Engineer Note Interfacing SDRAM Memories to SHARC Processors (EE-286), and the SDRAM vendor data sheet.

Table 31. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA Setup Before SDCLK	0.7		ns
t_{HSDAT}	DATA Hold After SDCLK	1.23		ns
Switching Characteristics				
t_{SDCLK}[1]	SDCLK Period	6		ns
t_{SDCLKH}	SDCLK Width High	2.2		ns
t_{SDCLKL}	SDCLK Width Low	2.2		ns
t_{DCAD}[2]	Command, ADDR, Data Delay After SDCLK		4	ns
t_{HCAD}[2]	Command, ADDR, Data Hold After SDCLK	1		ns
t_{DSDAT}	Data Disable After SDCLK		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	0.3		ns

[1] Systems should use the SDRAM model with a speed grade higher than the desired SDRAM controller speed. For example, to run the SDRAM controller at 166 MHz the SDRAM model with a speed grade of 183 MHz or above should be used. See Engineer-to-Engineer Note Interfacing SDRAM Memories to SHARC Processors (EE-286) for more information on hardware design guidelines for the SDRAM interface.
[2] Command pins include: $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{MSx}}$, SDA10, SDCKE.

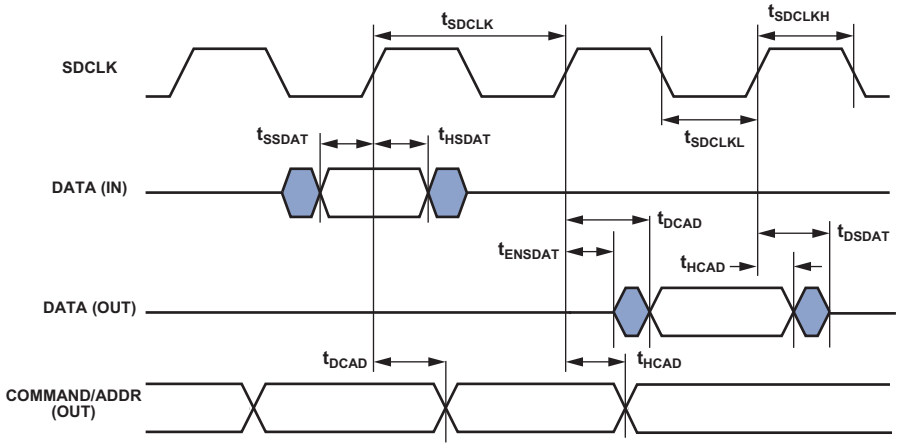

Figure 18. SDRAM Interface Timing

Table 37. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		11.5	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1.5		ns

[1] Referenced to drive edge.

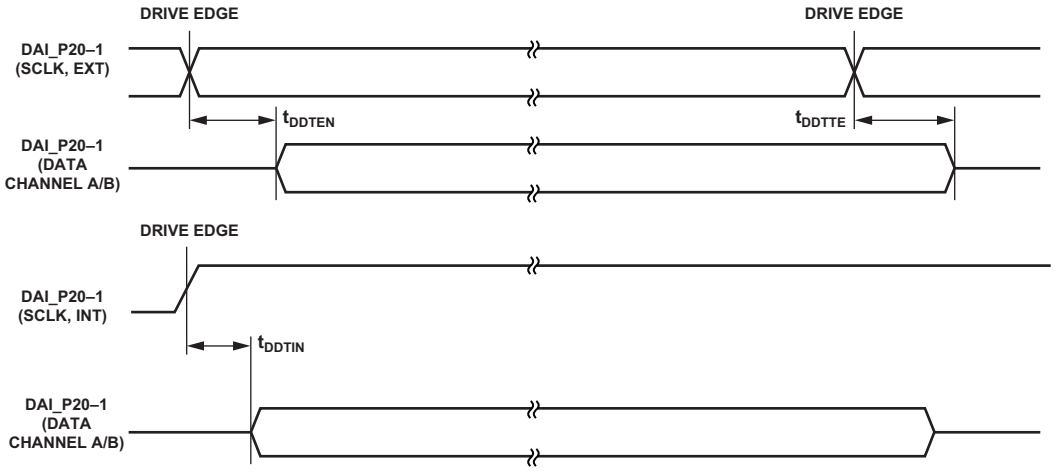

Figure 23. Serial Ports—Enable and Three-State

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

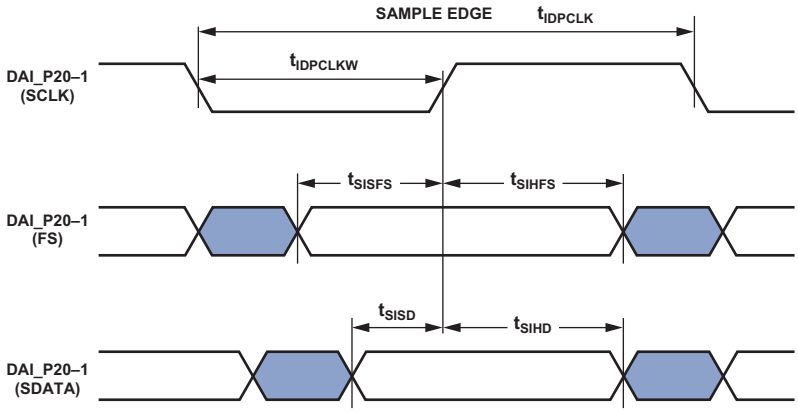

Figure 25. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 40. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the hardware reference. Note that the 20 bits of external PDAP data can be provided through the ADDR23–4 pins or over the DAI pins.

Table 40. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

[1] Source pins of PDAP_DATA are ADDR23–4 or DAI pins. Source pins for PDAP_CLK and PDAP_HOLD are 1) DAI pins; 2) CLKIN through PCG; 3) DAI pins through PCG; or 4) ADDR3–2 pins.

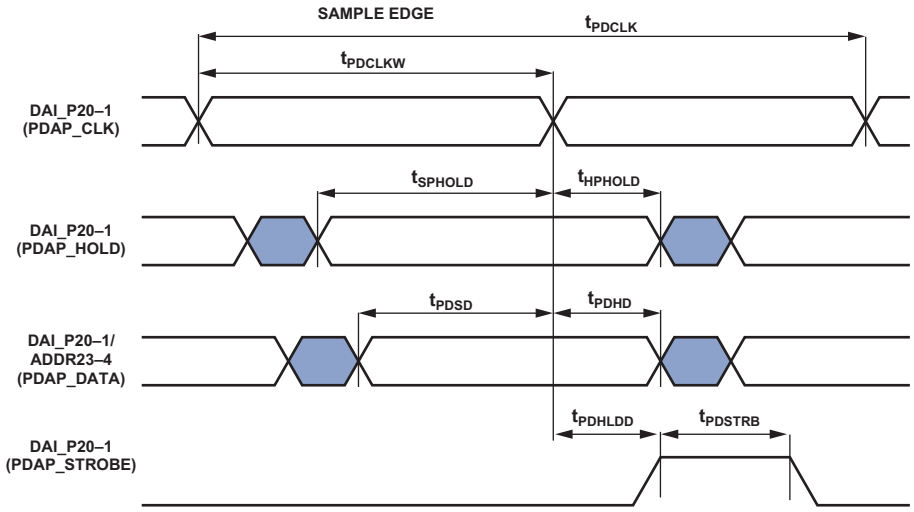

Figure 26. PDAP Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the ADDR23–8/DPI_14–1 pins are configured as PWM.

Table 43. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

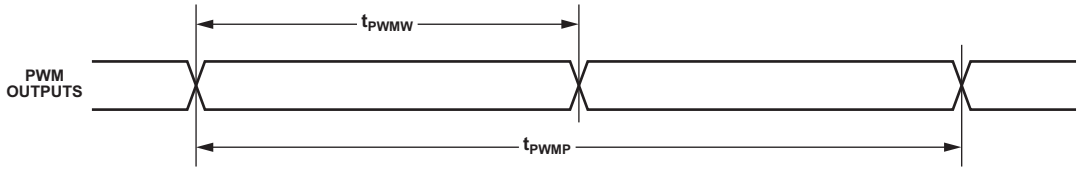

Figure 29. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 30 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Table 44. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	Frame Sync to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

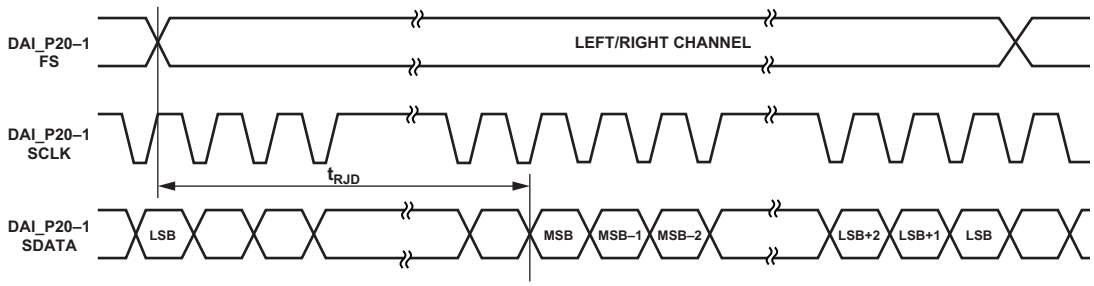

Figure 30. Right-Justified Mode

SPI Interface—Master

The ADSP-2148x contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 50 and Table 51 applies to both.

Table 50. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1.2$		ns

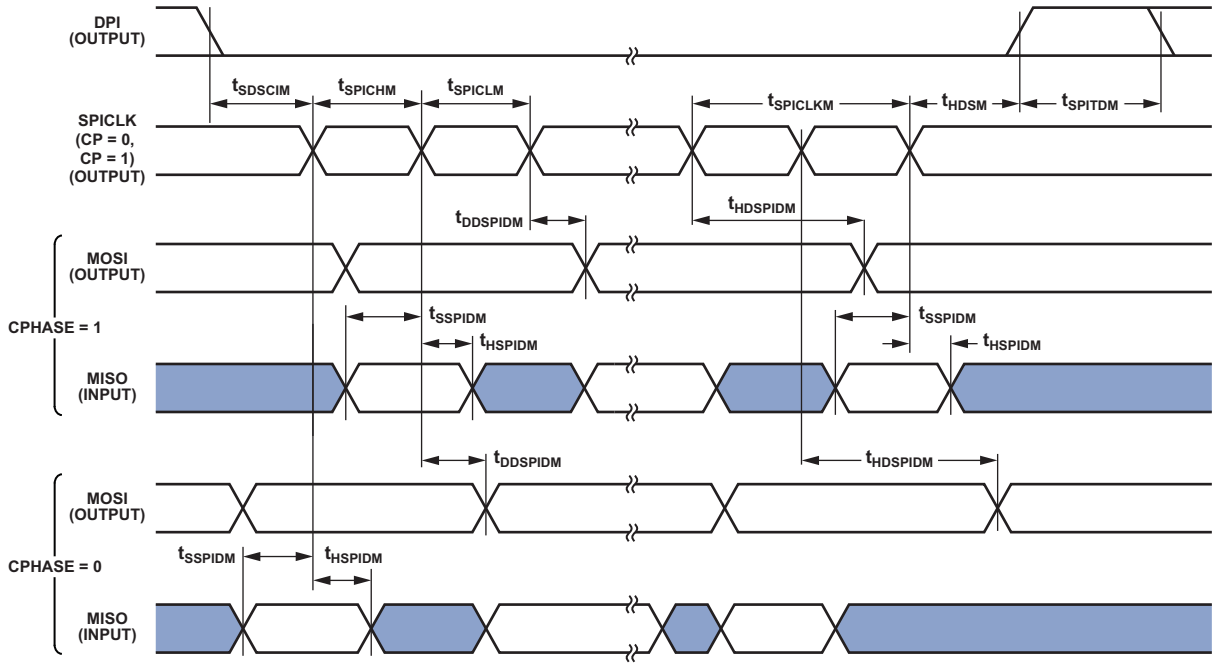

Figure 35. SPI Master Timing

SPI Interface—Slave

Table 51. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge CPHASE = 0 CPHASE = 1	$2 \times t_{PCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Set-up Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0)	$2 \times t_{PCLK}$		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	7.5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	7.5	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	10.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	10.5	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the "Serial Peripheral Interface Port" chapter of the hardware reference.

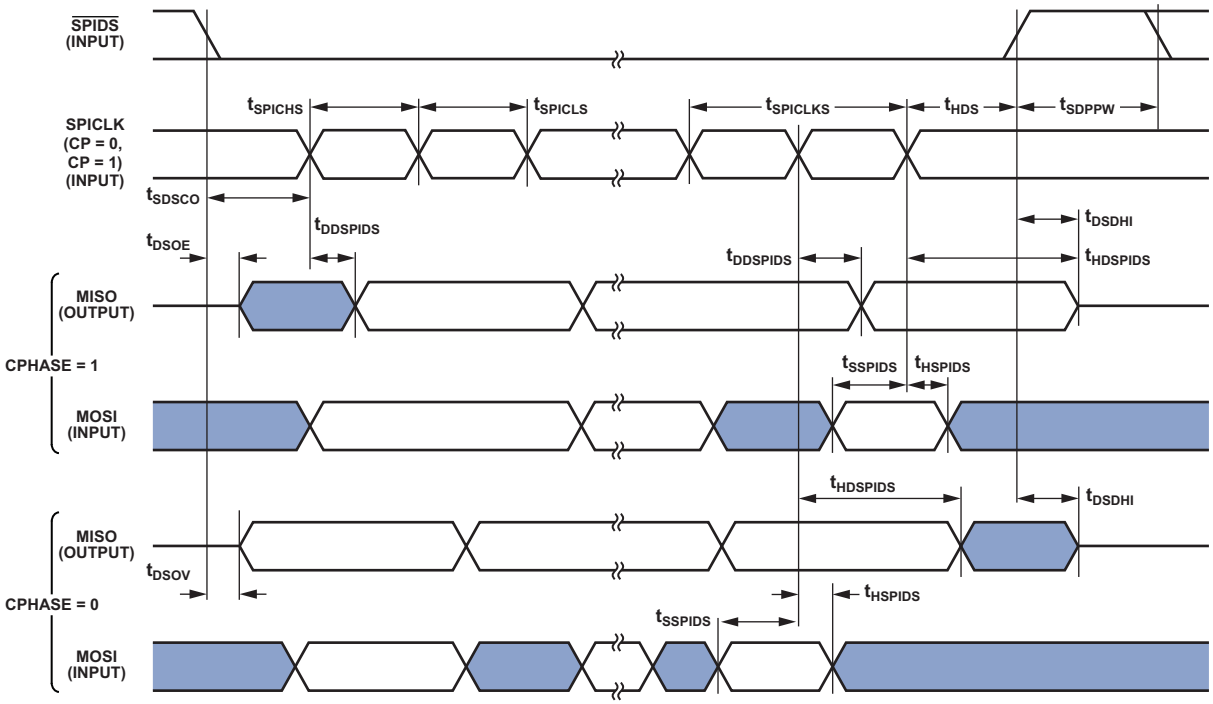

Figure 36. SPI Slave Timing

Note that the thermal characteristics values provided in Table 56 and Table 57 are modeled values.

Table 56. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.8	°C/W
θ_{JMA}	Airflow = 1 m/s	15.4	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.24	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.37	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.51	°C/W

Table 57. Thermal Characteristics for 176-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	16.9	°C/W
θ_{JMA}	Airflow = 1 m/s	14.6	°C/W
θ_{JMA}	Airflow = 2 m/s	13.8	°C/W
θ_{JC}		2.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.21	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.32	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.41	°C/W

Thermal Diode

The ADSP-2148x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann's constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

Table 58 contains the thermal diode specifications using the transistor model.

Table 58. Thermal Diode Parameters – Transistor Model[1]

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}[2]	Forward Bias Current	10		300	µA
I_E	Emitter Current	10		300	µA
n_Q[3, 4]	Transistor Ideality	1.012	1.015	1.017	
R_T[3, 5]	Series Resistance	0.12	0.2	0.28	Ω

[1] See Engineer-to-Engineer Note Using the On-Chip Thermal Diode on Analog Devices Processors (EE-346).
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
[5] The series resistance (R_T) can be used for more accurate readings as needed.

AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications on Page 18 section of this data sheet carefully. Only the automotive grade products shown in Table 63 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 63. Automotive Products

Model[1, 2, 3, 4]	Notes	Temperature Range[5]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
AD21486WBSWZ4Axx	[6]	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Axx	[6]	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Bxx	[6]	–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ1Axx		–40°C to +85°C	3 Mbit	266 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ2Axx		–40°C to +85°C	3 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ1Bxx		–40°C to +85°C	2 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ2Bxx		–40°C to +85°C	3 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ4Bxx		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21489WBSWZ4xx		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4xxRL		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4Bxx		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z =RoHS Compliant Part.
[2] W = automotive applications.
[3] xx denotes the current die revision.
[4] RL = Tape and Reel.
[5] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification which is the only temperature specification.
[6] This product contains IP from Dolby, DTS and DTLA. Proper software licenses required. Contact Analog Devices, Inc. for information.

ORDERING GUIDE

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21483KSWZ-2B	[3]	0°C to +70°C	3 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3B	[3]	0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3AB	[3]	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21483KSWZ-4B	[3]	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2A	[3]	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2B	[3]	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2AB	[3]	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2BB	[3]	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3A	[3]	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3B	[3]	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3AB	[3]	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3BB	[3]	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-4A	[3]	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-4AB	[3]	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21487KSWZ-2B	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-2BB	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3B	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3BB	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4B	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4BB	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5B	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5BB	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP21487KSWZ5BBRL	5	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3A		–40°C to +85°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A		0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A1	6	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3B		0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3B		–40°C to +85°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4A		0°C to +70°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488BSWZ-4A		–40°C to +85°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-4B		0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-4B		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4B1	6	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-3A		0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-3A		–40°C to +85°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-3B		0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-3B		–40°C to +85°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-4A		0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-4A		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-4B		0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-4B		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-5B	4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification, which is the only temperature specification.

[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

[4] See Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for operating ADSP-2148x processors at 450 MHz.

[5] RL = Tape and Reel.

[6] This product contains a –140 dB sample rate converter.