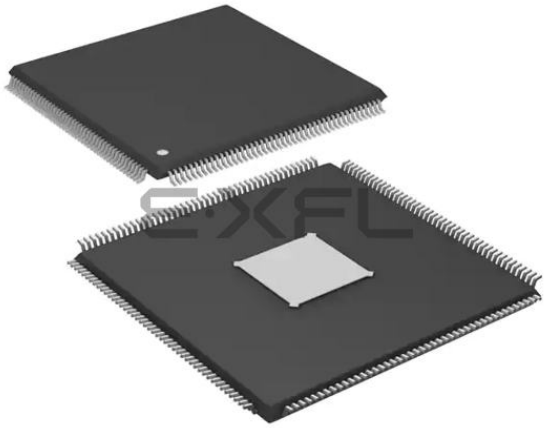

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	EBI/EMI, DAI, I²C, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21489bswz-4b

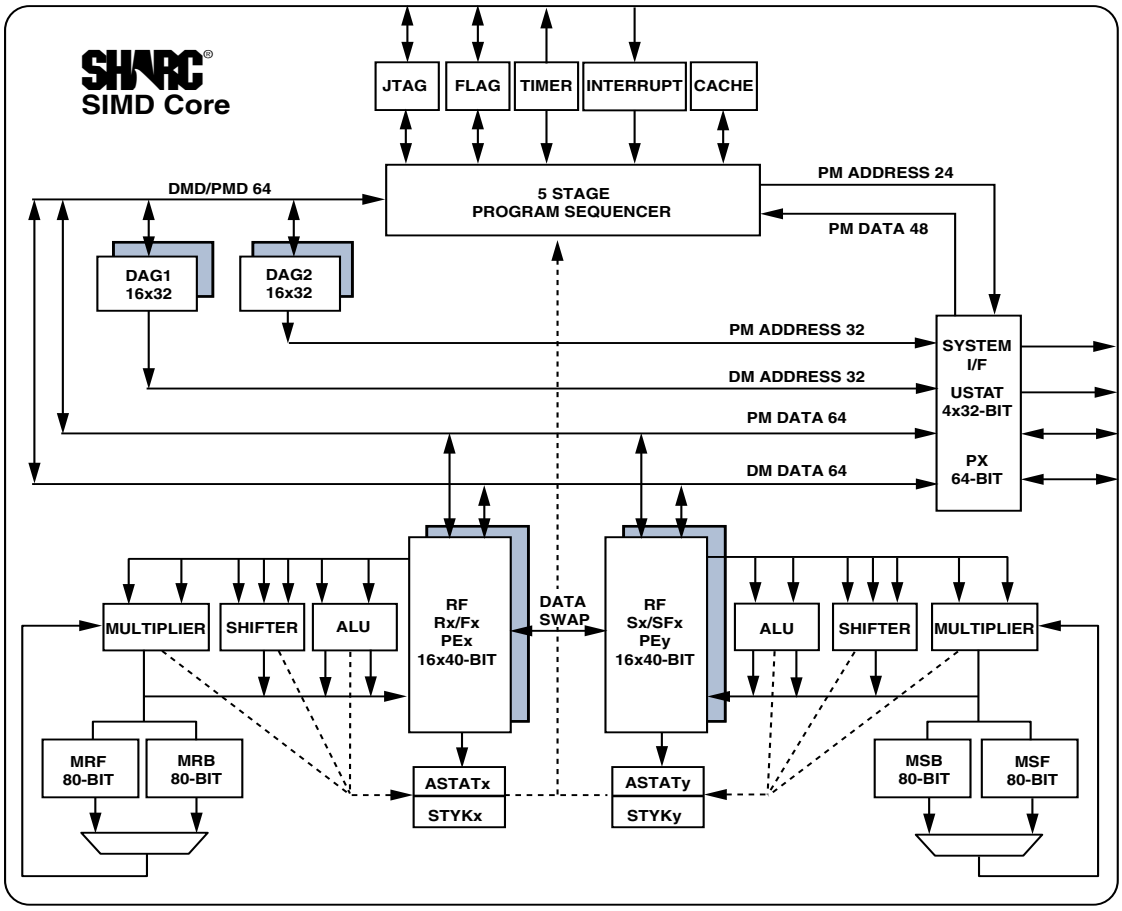

Figure 2. SHARC Core Block Diagram

Universal Registers

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all peripheral registers (control/status).

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2148x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data. With the its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processor can conditionally execute a multiply, an add, and a

- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

Non-SDRAM external memory address space is shown in Table 5.

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	6M	0x0020 0000–0x007F FFFF
Bank 1	8M	0x0400 0000–0x047F FFFF
Bank 2	8M	0x0800 0000–0x087F FFFF
Bank 3	8M	0x0C00 0000–0x0C7F FFFF

External Port

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 176-lead LQFP, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and banks 1, 2, and 3 occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices at speeds up to f_{SDCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 4M bytes and 256M bytes of memory. SDRAM external memory address space is shown in Table 6. NOTE: this feature is not available on the ADSP-21486 model.

Table 6. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on the SDRAM and AMI interfaces.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This removes the need to explicitly access the complimentary registers when the data is in external SDRAM memory.

VISA and ISA Access to External Memory

The SDRAM controller on the ADSP-2148x processors supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. Table 7 shows the address ranges for instruction fetch in each mode.

Table 7. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000–0x005F FFFF
VISA (SW)	10M	0x0060 0000–0x00FF FFFF

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single-update mode or double-update mode. In single-update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double-update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

MediaLB

The automotive models of the ADSP-2148x processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive models, see Automotive Products on Page 66.

Digital Applications Interface (DAI)

The digital applications interface (DAI) allows the connection of various peripherals to any of the DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes eight serial ports, four precision clock generators (PCG), a S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports (SPORTs)

The ADSP-2148x features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I^2S or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, or the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter (SRC)

The asynchronous sample rate converter contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode.

The IDP also provides a parallel data acquisition port (PDAP), which can be used for receiving parallel data. The PDAP port has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23–0}$	I/O/T (ipu)	High-Z/ driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, and FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in external memory interface mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23–4}$ pins for parallel input data.
$DATA_{15–0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), and $FLAGS_{7–0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0–1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information, see the hardware reference.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.**
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.**

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{SDRAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
SDCKE	O/T (ipu)	High-Z/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (ipu)	High-Z/ driven high	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's ADDR10 pin only during SDRAM accesses.
SDDQM	O/T (ipu)	High-Z/ driven high	**DQM Data Mask.** SDRAM Input mask signal for write accesses and output mask signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The SDRAM output buffers are placed in a High-Z state when DQM is sampled high during a read cycle. SDDQM is driven high from reset de-assertion until SDRAM initialization completes. Afterwards it is driven low irrespective of whether any SDRAM accesses occur or not.
SDCLK	O/T (ipd)	High-Z/ driving	**SDRAM Clock Output.** Clock driver for this pin differs from all other clock drivers. See Figure 41 on Page 55. For models in the 100-lead package, the SDRAM interface should be disabled to avoid unnecessary power switching by setting the DSDCTL bit in SDCTL register. For more information, see the hardware reference.
DAI _P_{20-1}	I/O/T (ipu)	High-Z	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins.
DPI _P_{14-1}	I/O/T (ipu)	High-Z	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins.
WDT_CLKIN	I		**Watchdog Timer Clock Input.** This pin should be pulled low when not used.
WDT_CLKO	O		**Watchdog Resonator Pad Output.**
$\overline{\text{WDTRSTO}}$	O (ipu)		**Watchdog Timer Reset Out.**
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	300 MHz / 350 MHz / 400 MHz			450 MHz			Unit
		Min	Nominal	Max	Min	Nominal	Max	
V_{DD_INT}[2]	Internal (Core) Supply Voltage	1.05	1.1	1.15	SVS_{NOM} – 25 mV	1.0 – 1.15	SVS_{NOM} + 25 mV	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13		3.47	3.13		3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13		3.47	3.13		3.47	V
V_{IH}[3]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0		3.6	2.0		3.6	V
V_{IL}[3]	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		0.8	–0.3		0.8	V
V_{IH_CLKIN}[4]	High Level Input Voltage @ V_{DD_EXT} = Max	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Min	–0.3		+0.8	–0.3		+0.8	V
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		110	0		115	°C
T_J	Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	–40		125	NA		NA	°C

[1] Specifications subject to change without notice.

[2] SVS_{NOM} refers to the nominal SVS voltage which is set between 1.0 V and 1.15 V at the factory for each individual device. Only the unique SVS_{NOM} value in each chip may be used for 401 MHz to 450 MHz operation of that chip. This spec lists the possible range of the SVS_{NOM} values for all devices. The initial VDD_INT voltage at power on is 1.1 V nominal and it transitions to SVS programmed voltage as outlined in Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357).

[3] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[4] Applies to input pins CLKIN, WDT_CLKIN.

Total Power Dissipation

The information in this section should be augmented with the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348).

Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature (T_J) and core voltage (V_{DD_INT}).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13).

     Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

Table 13. Activity Scaling Factors (ASF)[1]

Activity	Scaling Factor (ASF)
Idle	0.29
Low	0.53
Medium Low	0.61
Medium High	0.77
Peak Typical (50:50)[2]	0.85
Peak Typical (60:40)[2]	0.93
Peak Typical (70:30)[2]	1.00
High Typical	1.16
High	1.25
Peak	1.31

[1] See the Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for more information on the explanation of the power vectors specific to the ASF table.

[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]

	V_{DD_INT} (V)								
T_J (°C)	0.975 V	1.0 V	1.025 V	1.05 V	1.075 V	1.10 V	1.125 V	1.15 V	1.175 V
–45	68	77	86	96	107	118	131	144	159
–35	74	83	92	103	114	126	140	154	170
–25	82	92	101	113	125	138	153	168	185
–15	94	104	115	127	140	155	171	187	205
–5	109	121	133	147	161	177	194	212	233
+5	129	142	156	171	188	206	225	245	268
+15	152	168	183	201	219	240	261	285	309
+25	182	199	216	237	257	280	305	331	360
+35	217	237	256	279	303	329	358	388	420
+45	259	282	305	331	359	389	421	455	492
+55	309	334	361	391	423	458	495	533	576
+65	369	398	429	464	500	539	582	626	675
+75	437	471	506	547	588	633	682	731	789
+85	519	559	599	645	693	746	802	860	926
+95	615	662	707	761	816	877	942	1007	1083
+105	727	779	833	897	958	1026	1103	1179	1266
+115	853	914	975	1047	1119	1198	1285	1372	1473
+125	997	1067	1138	1219	1305	1397	1498	1601	1716

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 18. All of the timing specifications for the ADSP-2148x peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information.

Table 18. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}
t_{SDCLK}	SDRAM Clock Period = (t_{CCLK}) × SDCKR

Figure 4 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the hardware reference.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 19. While no specific power-up sequencing is required between V_{DD_EXT} and V_{DD_INT}, there are some considerations that system designs should take into account.

- No power supply should be powered up for an extended period of time (> 200 ms) before another supply starts to ramp up.
- If the V_{DD_INT} power supply comes up after V_{DD_EXT}, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the V_{DD_INT} rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the V_{DD_INT} power supply comes up after V_{DD_EXT}, a leakage current of the order of three-state leakage current pull-up, pull-down may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the V_{DD_INT} rail has powered up.

Table 19. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_EXT} or V_{DD_INT} On	0		ms
$t_{IVDDEVDD}$	V_{DD_INT} On Before V_{DD_EXT}	–200	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DD_INT} and V_{DD_EXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		µs
Switching Characteristic				
$t_{CORERST}$[4, 5]	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	4096 × t_{CK} + 2 × t_{CCLK}		

[1] Valid V_{DD_INT} and V_{DD_EXT} assumes that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 21. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 29. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the "Precision Clock Generators" chapter in the hardware reference.

[1] Normal mode of operation.

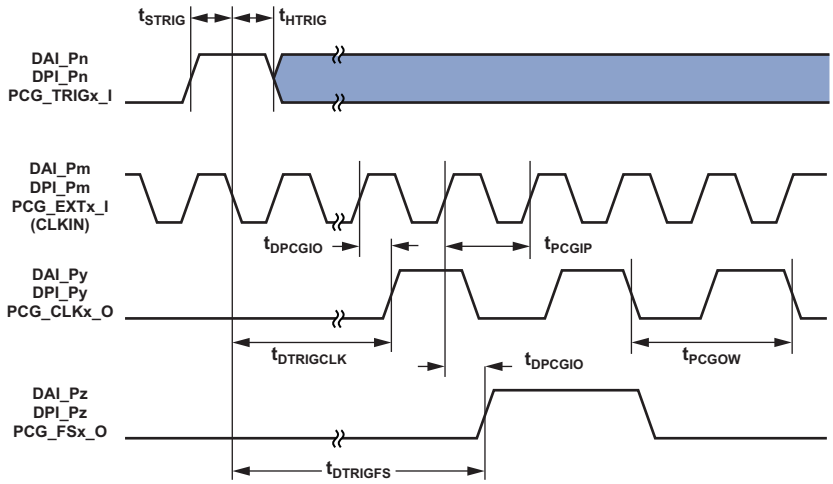

Figure 16. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to the DPI_P14–1, ADDR7–0, ADDR23–8, DATA7–0, and FLAG3–0 pins when configured as FLAGS. See Table 11 on Page 14 for more information on flag use.

Table 30. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}[1]	FLAGs IN Pulse Width	$2 \times t_{PCLK} + 3$		ns
Switching Characteristic				
t_{FOPW}[1]	FLAGs OUT Pulse Width	$2 \times t_{PCLK} - 3$		ns

[1] This is applicable when the Flags are connected to DPI_P14–1, ADDR7–0, ADDR23–8, DATA7–0 and FLAG3–0 pins.

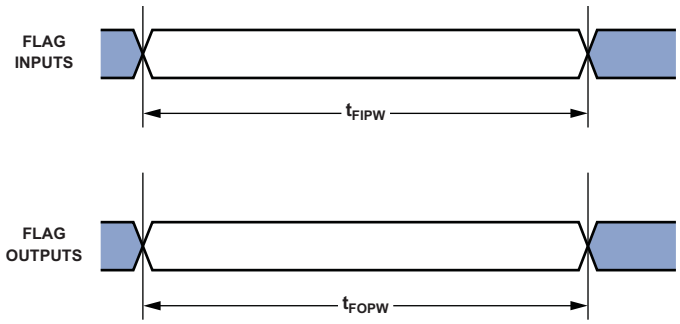

Figure 17. Flags

Serial Ports

In slave transmitter mode and master receiver mode, the maximum serial port frequency is $f_{PCLK}/8$. In master transmitter mode and slave receiver mode, the maximum serial port clock frequency is $f_{PCLK}/4$. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold; 2) data delay and data setup and hold; and 3) SCLK width.

Serial port signals (SCLK, frame sync, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	1.9		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		10.25	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		9	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 35. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	7		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	7		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		ns
Switching Characteristics				
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		4	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		9.75	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		3.25	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–2		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

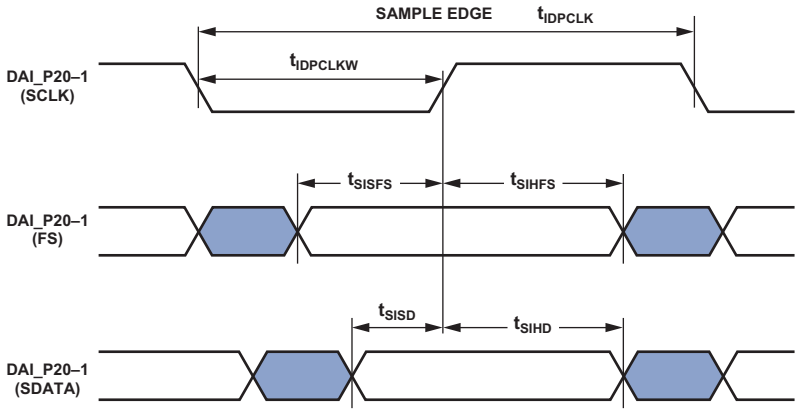

Figure 25. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 40. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the hardware reference. Note that the 20 bits of external PDAP data can be provided through the ADDR23–4 pins or over the DAI pins.

Table 40. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$		ns

[1] Source pins of PDAP_DATA are ADDR23–4 or DAI pins. Source pins for PDAP_CLK and PDAP_HOLD are 1) DAI pins; 2) CLKIN through PCG; 3) DAI pins through PCG; or 4) ADDR3–2 pins.

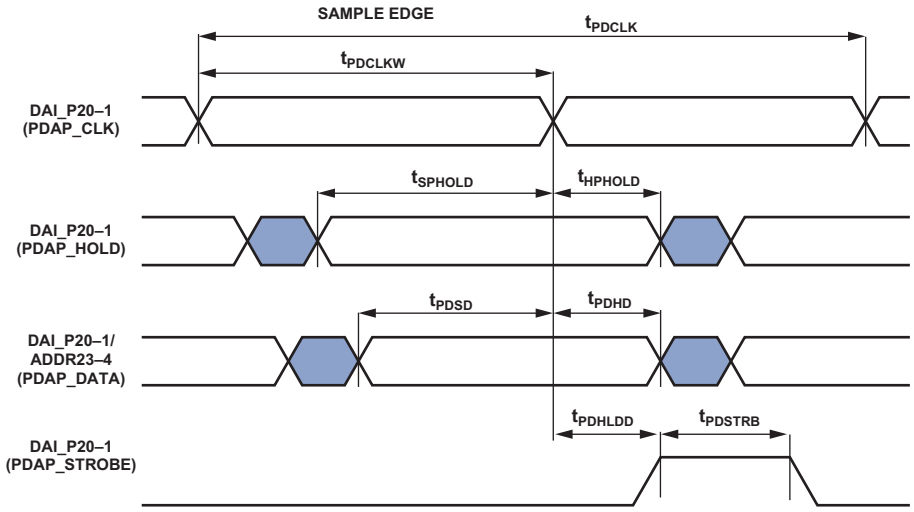

Figure 26. PDAP Timing

Sample Rate Converter—Serial Input Port

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 41 are valid at the DAI_P20–1 pins.

Table 41. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

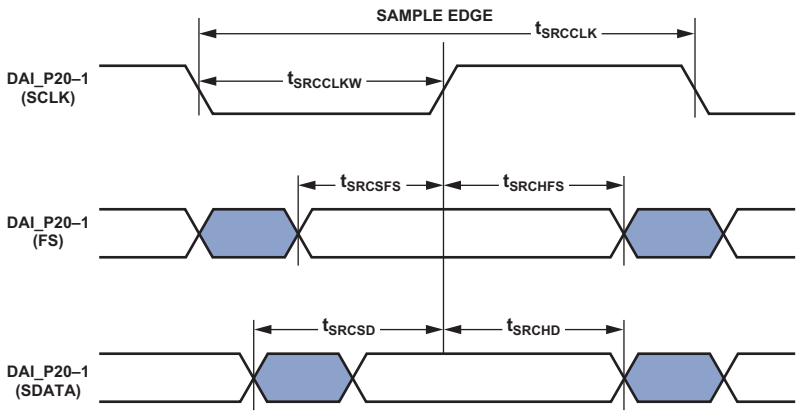

Figure 27. ASRC Serial Input Port Timing

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After Serial Clock		5	ns
t_{HOFSI}	Frame Sync Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	$8 \times t_{PCLK} - 2$		ns

[1] SCLK frequency is 64 × FS where FS = the frequency of frame sync.

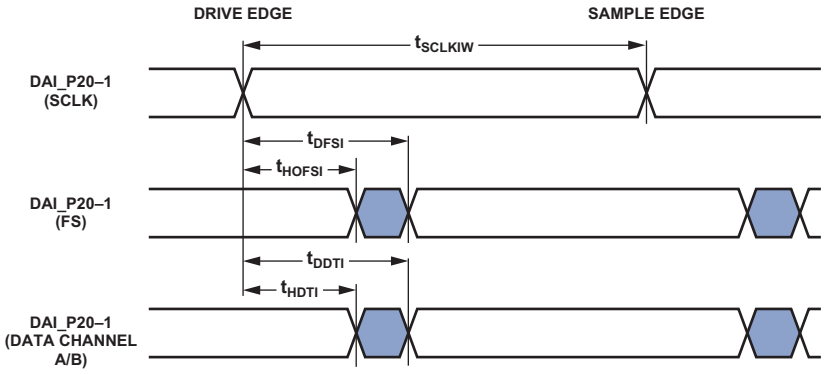

Figure 34. S/PDIF Receiver Internal Digital PLL Mode Timing

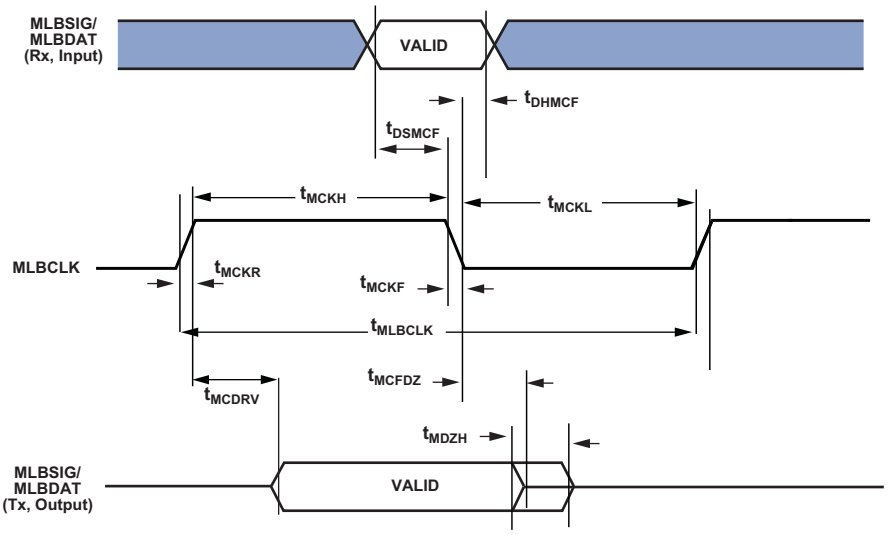

Figure 37. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	nspp
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{MLB}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] Gate Delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

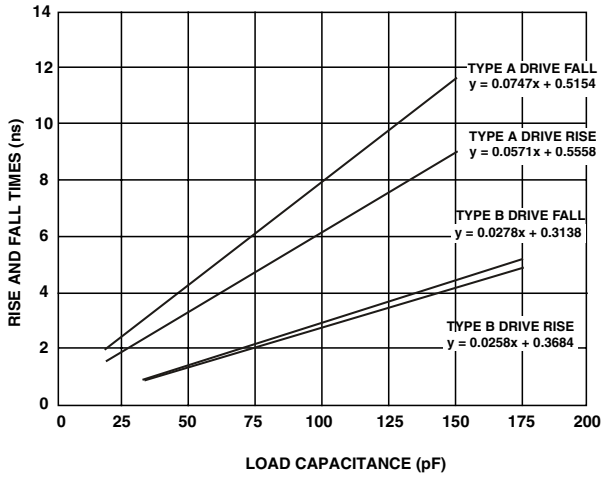

Figure 45. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

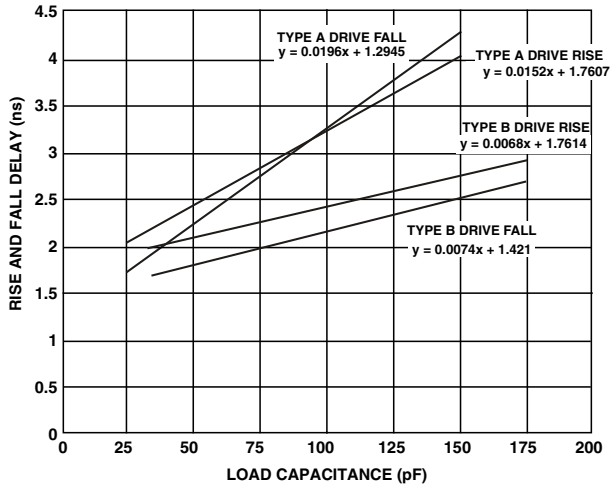

Figure 46. Typical Output Rise/Fall Delay (V_{DD_EXT} = Max)

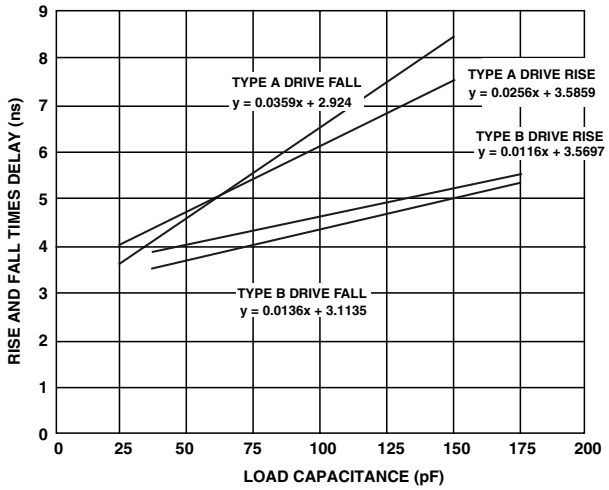

Figure 47. Typical Output Rise/Fall Delay (V_{DD_EXT} = Min)

THERMAL CHARACTERISTICS

The ADSP-2148x processor is rated for performance over the temperature range specified in Operating Conditions on Page 18.

Table 57 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (LQFP_EP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 57.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
NC	1	V_{DD_EXT}	45	DAI_P10	89	V_{DD_INT}	133
$\overline{MS0}$	2	DPI_P08	46	V_{DD_INT}	90	FLAG0	134
NC	3	DPI_P07	47	V_{DD_EXT}	91	FLAG1	135
V_{DD_INT}	4	V_{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V_{DD_INT}	93	GND	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	GND	139
V_{DD_EXT}	8	DPI_P12	52	DAI_P04	96	GND	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V_{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	GND	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V_{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	$\overline{TRST}$	144
ADDR5	13	V_{DD_EXT}	57	DAI_P15	101	GND	145
BOOT_CFG1	14	NC	58	V_{DD_INT}	102	$\overline{EMU}$	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V_{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V_{DD_INT}	105	DATA2	149
NC	18	V_{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V_{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V_{DD_INT}	65	GND	109	V_{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V_{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V_{DD_INT}	68	V_{DD_THD}	112	V_{DD_INT}	156
XTAL	25	NC	69	V_{DD_INT}	113	DATA7	157
ADDR10	26	$\overline{WDTRSTO}$	70	V_{DD_INT}	114	TDI	158
NC	27	NC	71	$\overline{MS1}$	115	NC	159*
V_{DD_EXT}	28	V_{DD_EXT}	72	V_{DD_INT}	116	V_{DD_EXT}	160
V_{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V_{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V_{DD_INT}	34	V_{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V_{DD_INT}	123	DATA14	167
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	36	NC	80	ADDR20	124	DATA13	168
V_{DD_INT}	37	NC	81	ADDR19	125	V_{DD_INT}	169
DPI_P01	38	NC	82	V_{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	NC	171
DPI_P03	40	V_{DD_EXT}	84	ADDR15	128	NC	172
V_{DD_INT}	41	V_{DD_INT}	85	V_{DD_INT}	129	$\overline{RESET}$	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	$\overline{AMI\_WR}$	131	NC	175
DPI_P06	44	DAI_P09	88	$\overline{AMI\_RD}$	132	V_{DD_INT}	176
						GND	177**

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications on Page 18 section of this data sheet carefully. Only the automotive grade products shown in Table 63 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 63. Automotive Products

Model[1, 2, 3, 4]	Notes	Temperature Range[5]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
AD21486WBSWZ4Axx	[6]	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Axx	[6]	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Bxx	[6]	–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ1Axx		–40°C to +85°C	3 Mbit	266 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ2Axx		–40°C to +85°C	3 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ1Bxx		–40°C to +85°C	2 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ2Bxx		–40°C to +85°C	3 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ4Bxx		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21489WBSWZ4xx		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4xxRL		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4Bxx		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z =RoHS Compliant Part.
[2] W = automotive applications.
[3] xx denotes the current die revision.
[4] RL = Tape and Reel.
[5] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification which is the only temperature specification.
[6] This product contains IP from Dolby, DTS and DTLA. Proper software licenses required. Contact Analog Devices, Inc. for information.

ORDERING GUIDE

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21483KSWZ-2B	[3]	0°C to +70°C	3 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3B	[3]	0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3AB	[3]	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21483KSWZ-4B	[3]	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2A	[3]	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2B	[3]	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2AB	[3]	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2BB	[3]	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3A	[3]	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3B	[3]	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3AB	[3]	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3BB	[3]	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-4A	[3]	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-4AB	[3]	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21487KSWZ-2B	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-2BB	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3B	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3BB	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4B	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4BB	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5B	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5BB	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP21487KSWZ5BBRL	5	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3A		–40°C to +85°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A		0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A1	6	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3B		0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3B		–40°C to +85°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4A		0°C to +70°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488BSWZ-4A		–40°C to +85°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-4B		0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-4B		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4B1	6	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-3A		0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-3A		–40°C to +85°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-3B		0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-3B		–40°C to +85°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-4A		0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-4A		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-4B		0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-4B		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-5B	4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification, which is the only temperature specification.

[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

[4] See Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for operating ADSP-2148x processors at 450 MHz.

[5] RL = Tape and Reel.

[6] This product contains a –140 dB sample rate converter.