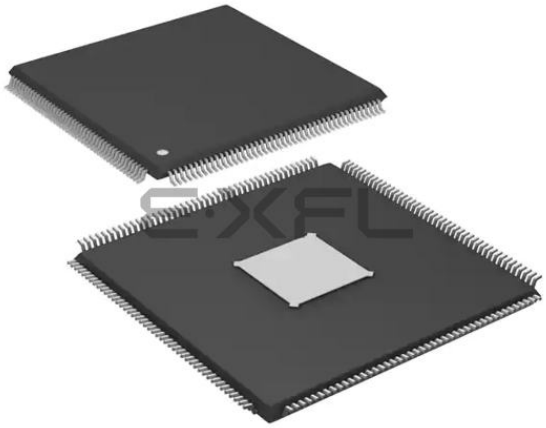

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	EBI/EMI, DAI, I²C, SPI, SPORT, UART/USART
Clock Rate	350MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP-EP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21489kswz-3b

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5/2016—Rev. C to Rev. D

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GENERAL DESCRIPTION

The ADSP-2148x SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x, ADSP-2147x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2148x processors are 32-bit/40-bit floating point processors optimized for high performance audio applications with large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1 shows performance benchmarks for the ADSP-2148x processors. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks

Benchmark Algorithm	Speed (at 400 MHz)	Speed (at 450 MHz)
1024 Point Complex FFT (Radix 4, with Reversal)	23 µs	20.44 µs
FIR Filter (per Tap)[1]	1.25 ns	1.1 ns
IIR Filter (per Biquad)[1]	5 ns	4.43 ns
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	11.25 ns	10.0 ns
[4 × 4] × [4 × 1]	20 ns	17.78 ns
Divide (y/×)	7.5 ns	6.67 ns
Inverse Square Root	11.25 ns	10.0 ns

[1] Assumes two files in multichannel SIMD mode

Table 2. ADSP-2148x Family Features

Feature	ADSP-21483	ADSP-21486	ADSP-21487	ADSP-21488	ADSP-21489
Maximum Instruction Rate	400 MHz	400 MHz	450 MHz	400 MHz	450 MHz
RAM	3 Mbits	5 Mbits		2/3 Mbits[1]	5 Mbits
ROM	4 Mbits			No	
Audio Decoders in ROM[2]	Yes			No	
Pulse-Width Modulation	4 Units (3 Units on 100-Lead Packages)				
DTCP Hardware Accelerator	Contact Analog Devices				
External Port Interface (SDRAM, AMI)[3]	Yes (16-bit)	AMI Only	Yes (16-bit)		
Serial Ports	8				
Direct DMA from SPORTs to External Port (External Memory)	Yes				
FIR, IIR, FFT Accelerator	Yes				
Watchdog Timer	Yes (176-Lead Package Only)				
MediaLB Interface	Automotive Models Only				
IDP/PDAP	Yes				
UART	1				
DAI (SRU)/DPI (SRU2)	Yes				
S/PDIF Transceiver	Yes				
SPI	Yes				
TWI	1				
SRC Performance[4]	–128 dB				
Thermal Diode	Yes				
VISA Support	Yes				
Package[3]	176-Lead LQFP EPAD 100-Lead LQFP EPAD		176-Lead LQFP EPAD	176-Lead LQFP EPAD 100-Lead LQFP EPAD[5]	

[1] See Ordering Guide on Page 66.

[2] ROM is factory programmed with latest multichannel audio decoding and post-processing algorithms from Dolby® Labs and DTS®. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[3] The 100-lead packages do not contain an external port. The SDRAM controller pins must be disabled when using this package. For more information, see Pin Function Descriptions on Page 14. The ADSP-21486 processor in the 176-lead package also does not contain a SDRAM controller. For more information, see 176-Lead LQFP_EP Lead Assignment on page 60.

[4] Some models have –140 dB performance. For more information, see Ordering Guide on page 66.

[5] Only available up to 400 MHz. See Ordering Guide on Page 66 for details.

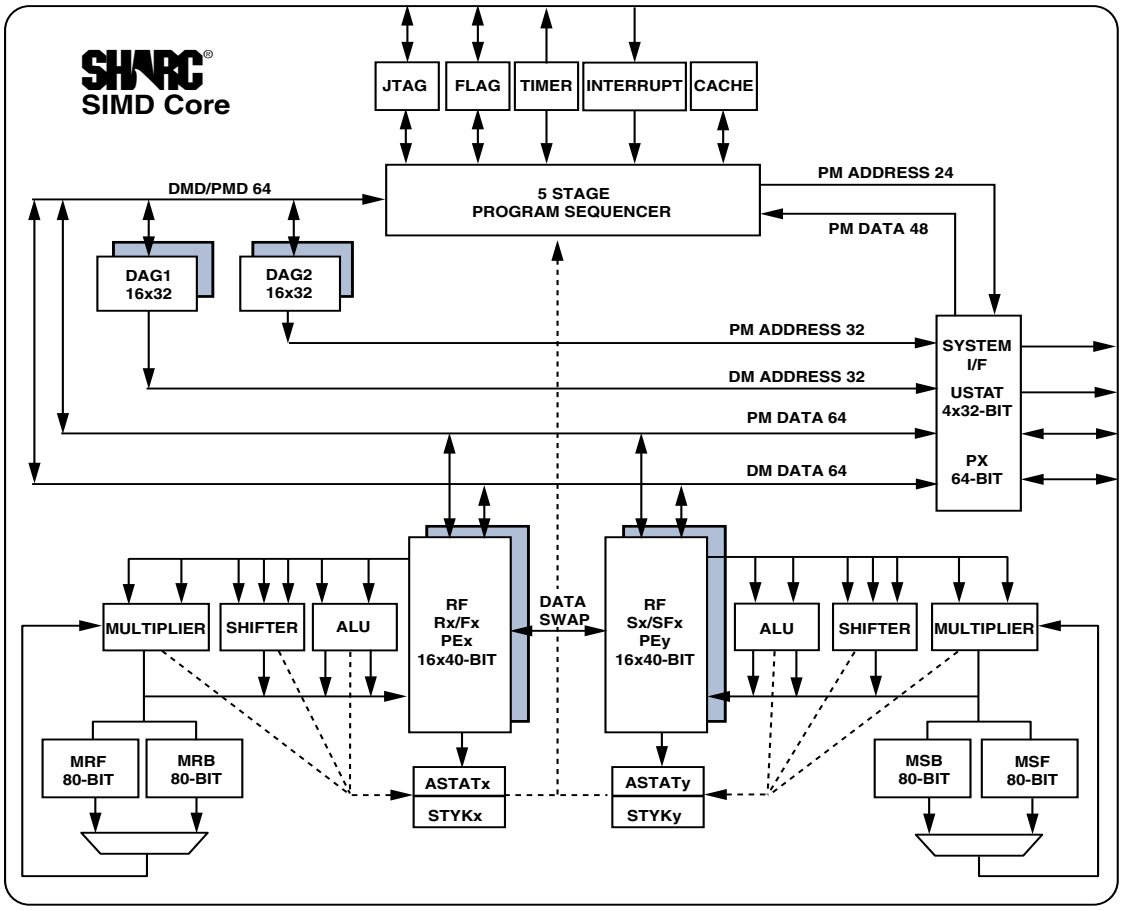

Figure 2. SHARC Core Block Diagram

Universal Registers

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all peripheral registers (control/status).

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2148x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data. With the its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processor can conditionally execute a multiply, an add, and a

Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from non contiguous memory blocks.

FFT Accelerator

The FFT accelerator implements a radix-2 complex/real input, complex output FFT with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watchdog Timer

The watchdog timer is used to supervise the stability of the system software. When used in this way, software reloads the watchdog timer in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset, if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer. The watchdog timer resets both the core and the internal peripherals. Note that this feature is available on the 176-lead package only.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2148x boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2–0) pins in Table 9 for the 176-lead package and Table 10 for the 100-lead package.

Table 9. Boot Mode Selection, 176-Lead Package

BOOT_CFG2–0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI User Boot (for 8-bit Flash Boot)
011	No boot (processor executes from internal ROM after reset)
1xx	Reserved

Table 10. Boot Mode Selection, 100-Lead Package

BOOT_CFG1–0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Reserved
11	No boot (processor executes from internal ROM after reset)

The "Running Reset" feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the RESETOUT/RUNRSTIN pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the hardware reference.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal supply must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Static Voltage Scaling (SVS)

Some models of the ADSP-2148x feature Static Voltage Scaling (SVS) on the V_{DD_INT} power supply. (See the Ordering Guide on Page 66 for model details.) This voltage specification technique can provide significant performance benefits including 450 MHz core frequency operation without a significant increase in power.

SVS optimizes the required V_{DD_INT} voltage for each individual device to enable enhanced operating frequency up to 450 MHz. The optimized SVS voltage results in a reduction of maximum I_{DD_INT} which enables 450 MHz operation at the same or lower maximum power than 400 MHz operation at a fixed voltage supply. Implementation of SVS requires a specific voltage regulator circuit design and initialization code.

Refer to the Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for further information. The EE-Note details the requirements and process to implement a SVS power supply system to enable operation up to 450 MHz. This applies only to specific products within the ADSP-2148x family which are capable of supporting 450 MHz operation.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
MLBCLK[1]	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS=48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT[1]	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG[1]	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO[1]	O/T	High-Z	**Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
MLBSO[1]	O/T	High-Z	**Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground.
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{\text{EMU}}$	O (O/D, ipu)	High-Z	**Emulation Status.** Must be connected to the ADSP-2148x Analog Devices DSP Tools product line of JTAG emulators target board connector only.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	300 MHz / 350 MHz / 400 MHz / 450 MHz Min	Typ	Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]			0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V			10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V			200	µA
I_{OZHPD}[8]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max			200	µA
I_{DD_INT}[9]	Supply Current (Internal)	f_{CCLK} > 0 MHz			Table 14 + Table 15 × ASF	mA
I_{DD_INT}	Supply Current (Internal)	V_{DDINT} = 1.1 V, ASF = 1, T_J = 25°C		410 / 450 / 500 / 550		mA
C_{IN}[10, 11]	Input Capacitance	T_{CASE} = 25°C			5	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23–0, DATA15–0, $\overline{AMI\_RD}$, $\overline{AMI\_WR}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{EMU}$, TDO, $\overline{RESETOUT}$ MLBSIG, MLBDAT, MLBDO, MLBSO, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDDQM, $\overline{MS0\text{-}1}$.
[3] See Output Drive Currents on Page 55 for typical drive current capabilities.
[4] Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pin: TDO.
[7] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{EMU}$.
[8] Applies to three-statable pin with pull-down: SDCLK.
[9] See Engineer-to-Engineer Note Estimating Power for ADSP-214xx SHARC Processors (EE-348) for further information.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 23. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{IRQx}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

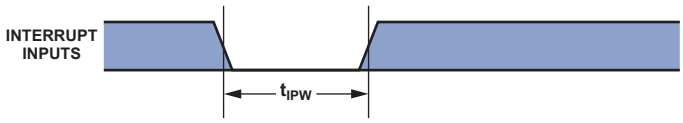

Figure 10. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1$		ns

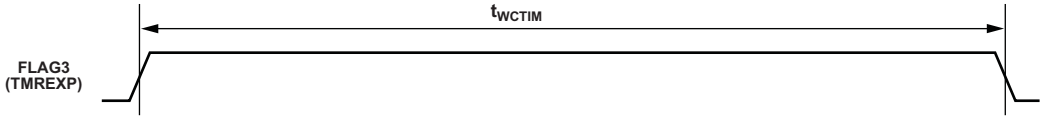

Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

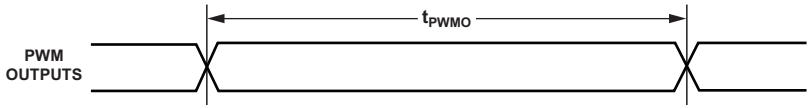

Figure 12. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse-width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 26. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

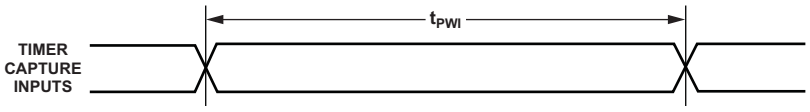

Figure 13. Timer Width Capture Timing

Watchdog Timer Timing

Table 27. Watchdog Timer Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{WDTCLKPER}$		100	1000	ns
Switching Characteristics				
t_{RST}	WDT Clock Rising Edge to Watchdog Timer $\overline{\text{RESET}}$ Falling Edge	3	6.4	ns
t_{RSTPW}	Reset Pulse Width	$64 \times t_{WDTCLKPER}$		ns

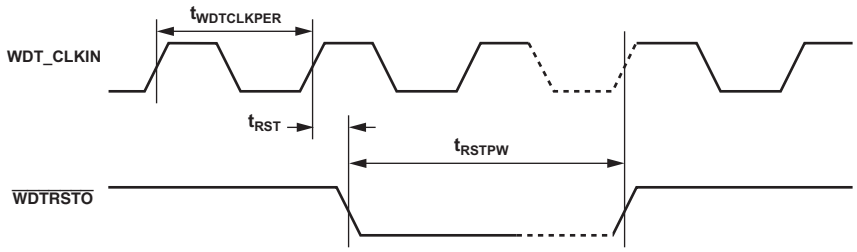

Figure 14. Watchdog Timer Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 28. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	12	ns

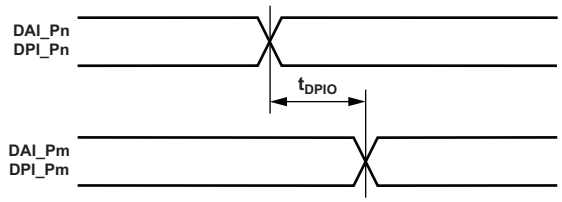

Figure 15. DAI Pin to Pin Direct Routing

AMI Write

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 33. AMI Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}[1, 2]	AMI_ACK Delay from Address, Selects		t_{SDCLK} – 9.7 + W	ns
t_{DSAK}[1, 3]	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low		W – 6	ns
Switching Characteristics				
t_{DAWH}[2]	Address Selects to $\overline{\text{AMI\_WR}}$ Deasserted	t_{SDCLK} – 3.1 + W		ns
t_{DAWL}[2]	Address Selects to $\overline{\text{AMI\_WR}}$ Low	t_{SDCLK} – 3		ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	t_{SDCLK} – 3.7 + W		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DATRWH}[4]	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted	t_{SDCLK} – 4.3 + H	t_{SDCLK} + 4.9 + H	ns
t_{WWR}[5]	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$ Low	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	2 × t_{SDCLK} – 6		ns
t_{WDE}	Data Enabled to $\overline{\text{AMI\_WR}}$ Low	t_{SDCLK} – 3.7		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).
[2] The falling edge of $\overline{\text{MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 55 for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: t_{SDCLK} + H, for both same bank and different bank. For Write to Read: 3 × t_{SDCLK} + H, for the same bank and different banks.

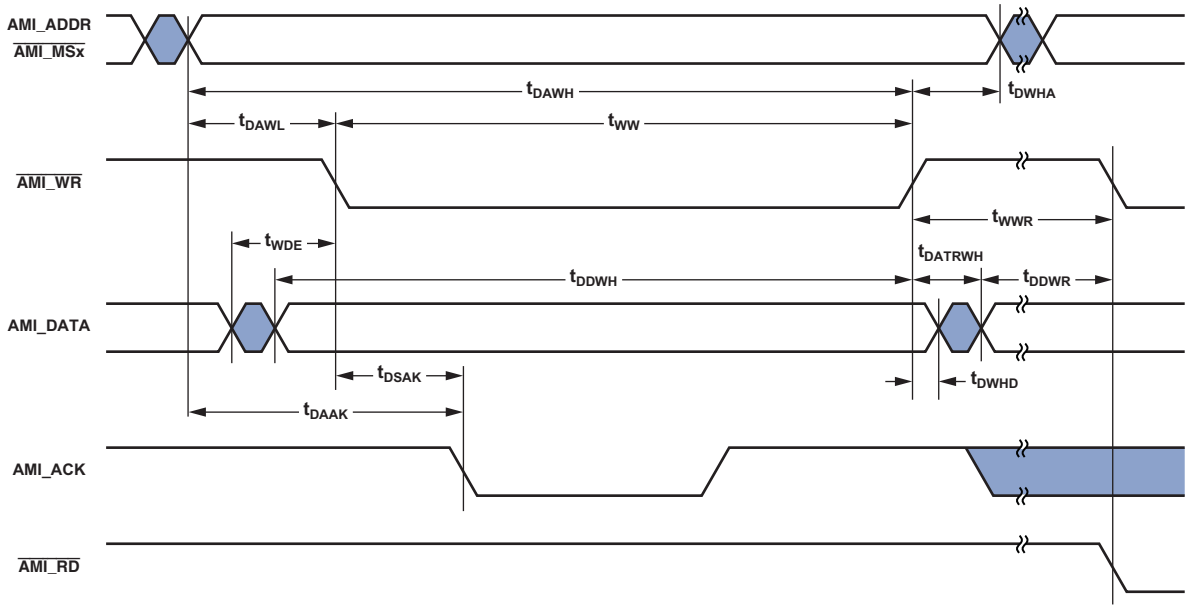

Figure 20. AMI Write

Table 36. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		8.5	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified, as well as DSP serial mode, and MCE = 1, MFD = 0.

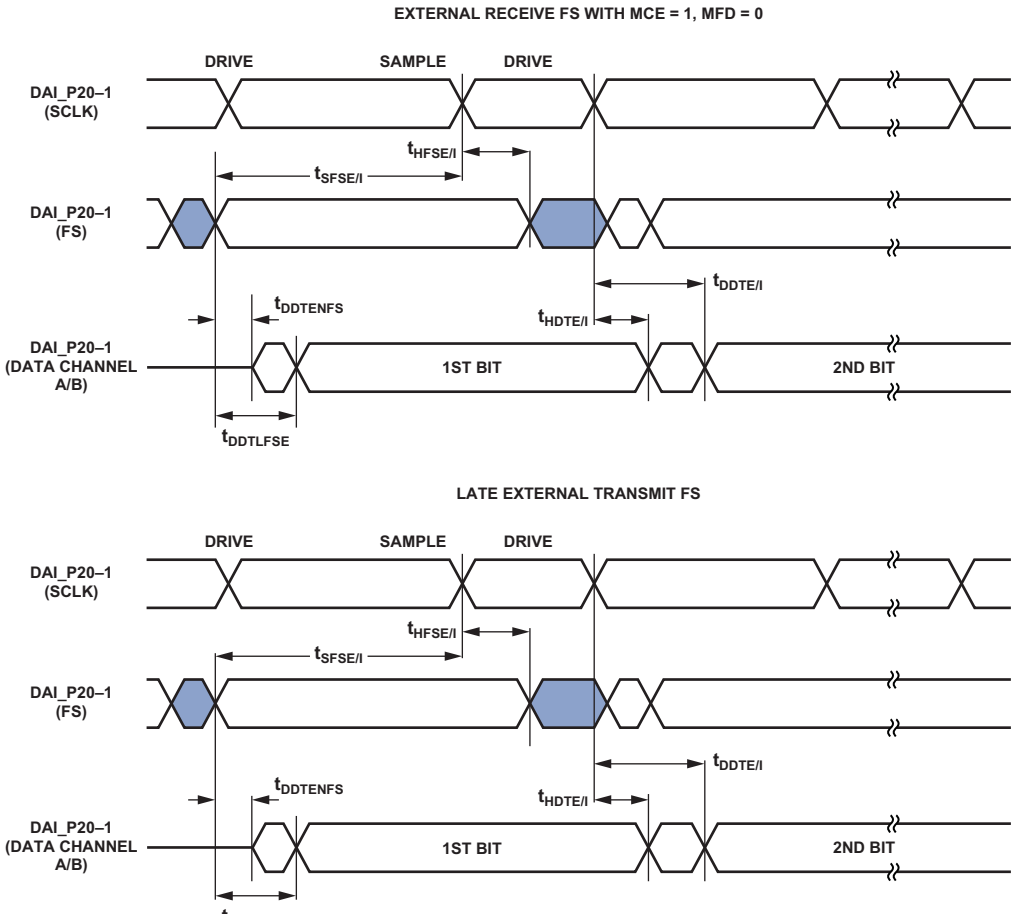

Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified mode.

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPORTx_TDV_O is asserted for communication with external devices.

Table 38. Serial Ports—TDV (Transmit Data Valid)

Parameter		Min	Max	Unit
Switching Characteristics[1]				
t_{DRDVEN}	TDV Assertion Delay from Drive Edge of External Clock	3		ns
t_{DFDVEN}	TDV Deassertion Delay from Drive Edge of External Clock		8	ns
t_{DRDVIN}	TDV Assertion Delay from Drive Edge of Internal Clock	–1		ns
t_{DFDVIN}	TDV Deassertion Delay from Drive Edge of Internal Clock		2	ns

[1] Referenced to drive edge.

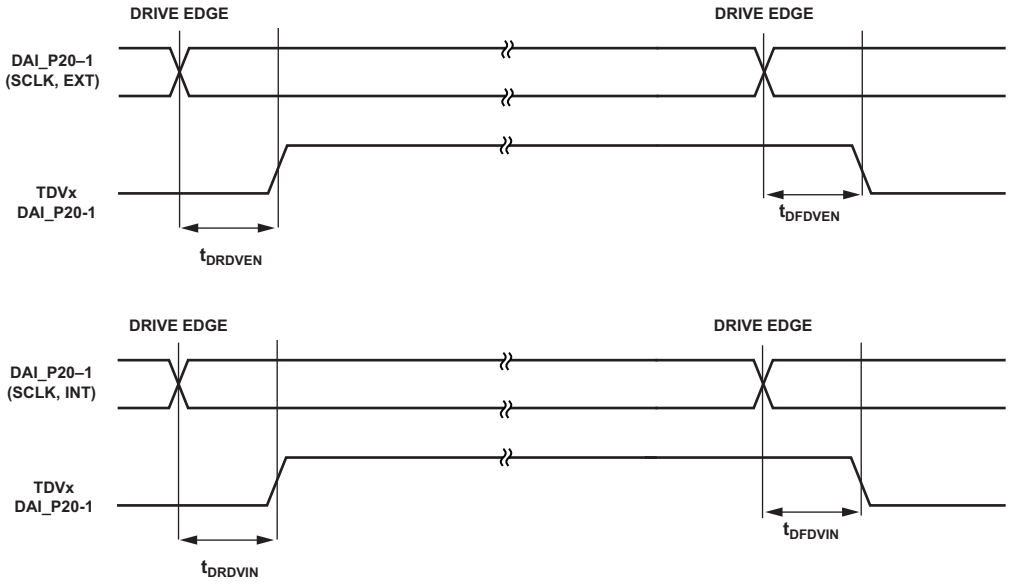

Figure 24. Serial Ports—TDM Internal and External Clock

SPI Interface—Slave

Table 51. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge CPHASE = 0 CPHASE = 1	$2 \times t_{PCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Set-up Time)	2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0)	$2 \times t_{PCLK}$		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	7.5	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	7.5	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	10.5	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	10.5	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		9.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the "Serial Peripheral Interface Port" chapter of the hardware reference.

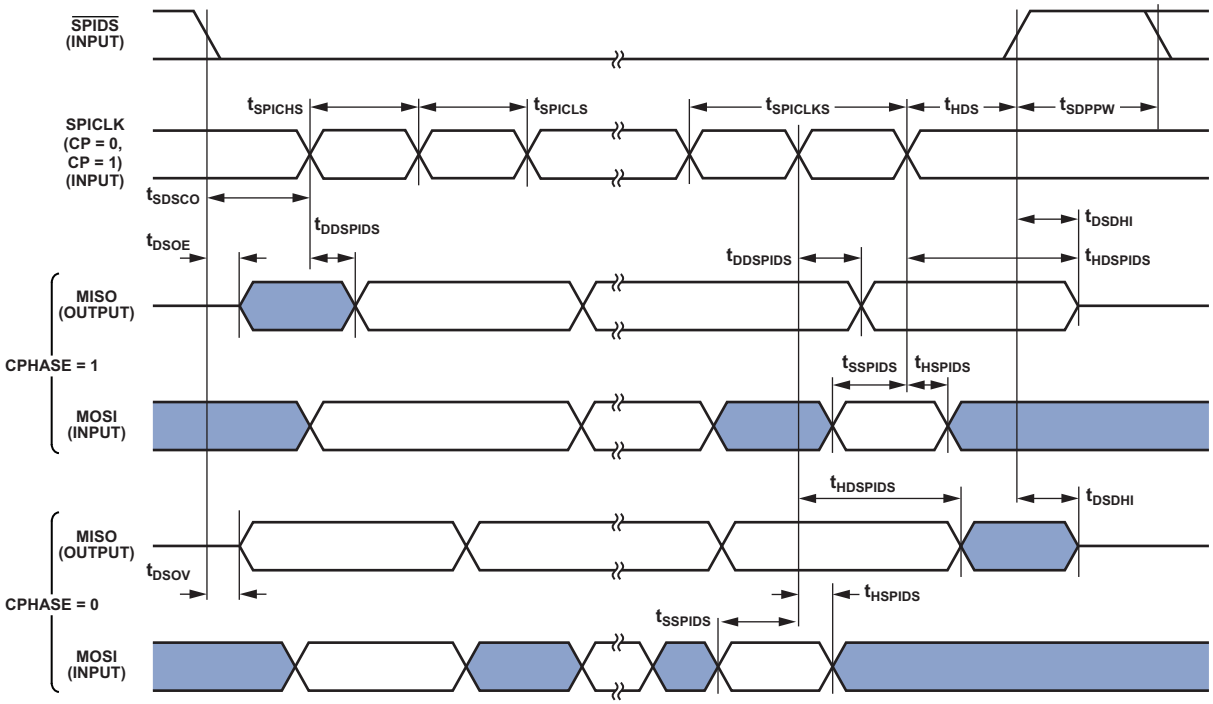

Figure 36. SPI Slave Timing

Note that the thermal characteristics values provided in Table 56 and Table 57 are modeled values.

Table 56. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.8	°C/W
θ_{JMA}	Airflow = 1 m/s	15.4	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.24	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.37	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.51	°C/W

Table 57. Thermal Characteristics for 176-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	16.9	°C/W
θ_{JMA}	Airflow = 1 m/s	14.6	°C/W
θ_{JMA}	Airflow = 2 m/s	13.8	°C/W
θ_{JC}		2.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.21	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.32	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.41	°C/W

Thermal Diode

The ADSP-2148x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann's constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

Table 58 contains the thermal diode specifications using the transistor model.

Table 58. Thermal Diode Parameters – Transistor Model[1]

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}[2]	Forward Bias Current	10		300	µA
I_E	Emitter Current	10		300	µA
n_Q[3, 4]	Transistor Ideality	1.012	1.015	1.017	
R_T[3, 5]	Series Resistance	0.12	0.2	0.28	Ω

[1] See Engineer-to-Engineer Note Using the On-Chip Thermal Diode on Analog Devices Processors (EE-346).
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
[5] The series resistance (R_T) can be used for more accurate readings as needed.

100-LQFP_EP LEAD ASSIGNMENT

Table 59. 100-Lead LQFP_EP Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
V_{DD_INT}	1	V_{DD_EXT}	26	DAI_P10	51	V_{DD_INT}	76
CLK_CFG1	2	DPI_P08	27	V_{DD_INT}	52	FLAG0	77
BOOT_CFG0	3	DPI_P07	28	V_{DD_EXT}	53	V_{DD_INT}	78
V_{DD_EXT}	4	V_{DD_INT}	29	DAI_P20	54	V_{DD_INT}	79
V_{DD_INT}	5	DPI_P09	30	V_{DD_INT}	55	FLAG1	80
BOOT_CFG1	6	DPI_P10	31	DAI_P08	56	FLAG2	81
GND	7	DPI_P11	32	DAI_P04	57	FLAG3	82
NC	8	DPI_P12	33	DAI_P14	58	MLBCLK	83
NC	9	DPI_P13	34	DAI_P18	59	MLBDAT	84
CLK_CFG0	10	DAI_P03	35	DAI_P17	60	MLBDO	85
V_{DD_INT}	11	DPI_P14	36	DAI_P16	61	V_{DD_EXT}	86
CLKIN	12	V_{DD_INT}	37	DAI_P15	62	MLBSIG	87
XTAL	13	V_{DD_INT}	38	DAI_P12	63	V_{DD_INT}	88
V_{DD_EXT}	14	V_{DD_INT}	39	V_{DD_INT}	64	MLBSO	89
V_{DD_INT}	15	DAI_P13	40	DAI_P11	65	$\overline{TRST}$	90
V_{DD_INT}	16	DAI_P07	41	V_{DD_INT}	66	$\overline{EMU}$	91
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	17	DAI_P19	42	V_{DD_INT}	67	TDO	92
V_{DD_INT}	18	DAI_P01	43	GND	68	V_{DD_EXT}	93
DPI_P01	19	DAI_P02	44	THD_M	69	V_{DD_INT}	94
DPI_P02	20	V_{DD_INT}	45	THD_P	70	TDI	95
DPI_P03	21	V_{DD_EXT}	46	V_{DD_THD}	71	TCK	96
V_{DD_INT}	22	V_{DD_INT}	47	V_{DD_INT}	72	V_{DD_INT}	97
DPI_P05	23	DAI_P06	48	V_{DD_INT}	73	$\overline{RESET}$	98
DPI_P04	24	DAI_P05	49	V_{DD_INT}	74	TMS	99
DPI_P06	25	DAI_P09	50	V_{DD_INT}	75	V_{DD_INT}	100
						GND	101*

MLB pins (pins 83, 84, 85, 87, and 89) are available for automotive models only. For non-automotive models, these pins should be connected to ground (GND).

* Pin no. 101 (exposed pad) is the GND supply (see Figure 48 and Figure 49) for the processor; this pad must be **robustly** connected to GND.

176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
NC	1	V_{DD_EXT}	45	DAI_P10	89	V_{DD_INT}	133
$\overline{MS0}$	2	DPI_P08	46	V_{DD_INT}	90	FLAG0	134
NC	3	DPI_P07	47	V_{DD_EXT}	91	FLAG1	135
V_{DD_INT}	4	V_{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V_{DD_INT}	93	GND	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	GND	139
V_{DD_EXT}	8	DPI_P12	52	DAI_P04	96	GND	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V_{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	GND	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V_{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	$\overline{TRST}$	144
ADDR5	13	V_{DD_EXT}	57	DAI_P15	101	GND	145
BOOT_CFG1	14	NC	58	V_{DD_INT}	102	$\overline{EMU}$	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V_{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V_{DD_INT}	105	DATA2	149
NC	18	V_{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V_{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V_{DD_INT}	65	GND	109	V_{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V_{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V_{DD_INT}	68	V_{DD_THD}	112	V_{DD_INT}	156
XTAL	25	NC	69	V_{DD_INT}	113	DATA7	157
ADDR10	26	$\overline{WDTRSTO}$	70	V_{DD_INT}	114	TDI	158
NC	27	NC	71	$\overline{MS1}$	115	NC	159*
V_{DD_EXT}	28	V_{DD_EXT}	72	V_{DD_INT}	116	V_{DD_EXT}	160
V_{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V_{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V_{DD_INT}	34	V_{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V_{DD_INT}	123	DATA14	167
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	36	NC	80	ADDR20	124	DATA13	168
V_{DD_INT}	37	NC	81	ADDR19	125	V_{DD_INT}	169
DPI_P01	38	NC	82	V_{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	NC	171
DPI_P03	40	V_{DD_EXT}	84	ADDR15	128	NC	172
V_{DD_INT}	41	V_{DD_INT}	85	V_{DD_INT}	129	$\overline{RESET}$	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	$\overline{AMI\_WR}$	131	NC	175
DPI_P06	44	DAI_P09	88	$\overline{AMI\_RD}$	132	V_{DD_INT}	176
						GND	177**

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

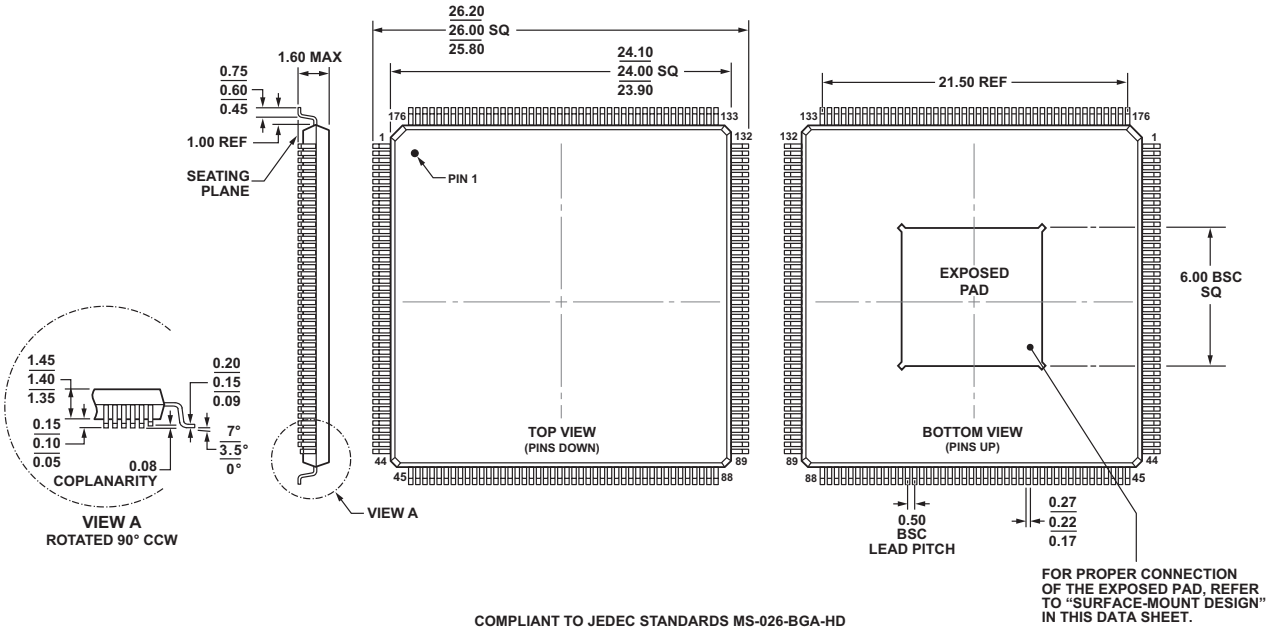

Figure 53. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP][1]
(SW-176-2)
Dimensions shown in millimeters

[1] For information relating to the exposed pad on the SW-176-2 package, see the table endnote on Page 60.

SURFACE-MOUNT DESIGN

The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be robustly connected to the GND plane in the PCB for best electrical and thermal performance. No separate GND pins are provided in the package.

AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications on Page 18 section of this data sheet carefully. Only the automotive grade products shown in Table 63 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 63. Automotive Products

Model[1, 2, 3, 4]	Notes	Temperature Range[5]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
AD21486WBSWZ4Axx	[6]	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Axx	[6]	–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21487WBSWZ4Bxx	[6]	–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ1Axx		–40°C to +85°C	3 Mbit	266 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ2Axx		–40°C to +85°C	3 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
AD21488WBSWZ1Bxx		–40°C to +85°C	2 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ2Bxx		–40°C to +85°C	3 Mbit	266 MHz	176-Lead LQFP_EP	SW-176-2
AD21488WBSWZ4Bxx		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
AD21489WBSWZ4xx		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4xxRL		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
AD21489WBSWZ4Bxx		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z =RoHS Compliant Part.
[2] W = automotive applications.
[3] xx denotes the current die revision.
[4] RL = Tape and Reel.
[5] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification which is the only temperature specification.
[6] This product contains IP from Dolby, DTS and DTLA. Proper software licenses required. Contact Analog Devices, Inc. for information.

ORDERING GUIDE

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21483KSWZ-2B	[3]	0°C to +70°C	3 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3B	[3]	0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21483KSWZ-3AB	[3]	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21483KSWZ-4B	[3]	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2A	[3]	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2B	[3]	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-2AB	[3]	0°C to +70°C	5 Mbit	300 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-2BB	[3]	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3A	[3]	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3B	[3]	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-3AB	[3]	0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-3BB	[3]	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21486KSWZ-4A	[3]	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21486KSWZ-4AB	[3]	0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2

Model[1]	Notes	Temperature Range[2]	RAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21487KSWZ-2B	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-2BB	3	0°C to +70°C	5 Mbit	300 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3B	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-3BB	3	0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4B	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-4BB	3	0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5B	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21487KSWZ-5BB	3, 4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP21487KSWZ5BBRL	5	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3A		–40°C to +85°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A		0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3A1	6	0°C to +70°C	3 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-3B		0°C to +70°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-3B		–40°C to +85°C	3 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4A		0°C to +70°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488BSWZ-4A		–40°C to +85°C	3 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21488KSWZ-4B		0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488BSWZ-4B		–40°C to +85°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21488KSWZ-4B1	6	0°C to +70°C	3 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-3A		0°C to +70°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-3A		–40°C to +85°C	5 Mbit	350 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-3B		0°C to +70°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-3B		–40°C to +85°C	5 Mbit	350 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-4A		0°C to +70°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489BSWZ-4A		–40°C to +85°C	5 Mbit	400 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21489KSWZ-4B		0°C to +70°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489BSWZ-4B		–40°C to +85°C	5 Mbit	400 MHz	176-Lead LQFP_EP	SW-176-2
ADSP-21489KSWZ-5B	4	0°C to +70°C	5 Mbit	450 MHz	176-Lead LQFP_EP	SW-176-2

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature (T_J) specification, which is the only temperature specification.

[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

[4] See Engineer-to-Engineer Note Static Voltage Scaling for ADSP-2148x SHARC Processors (EE-357) for operating ADSP-2148x processors at 450 MHz.

[5] RL = Tape and Reel.

[6] This product contains a –140 dB sample rate converter.

D09018-0-5/16(D)