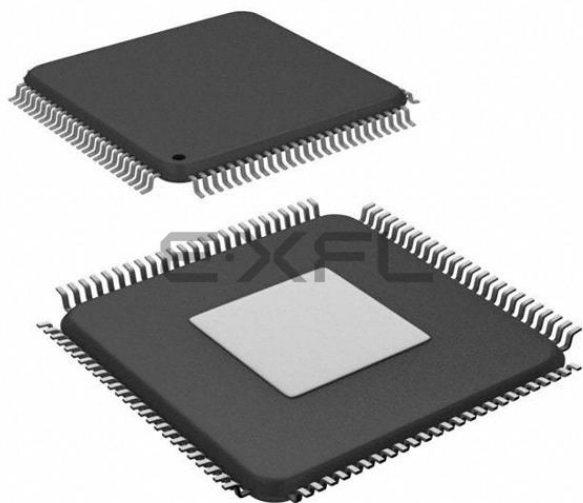




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Floating Point
Interface	EBI/EMI, DAI, I ² C, SPI, SPORT, UART/USART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21489kswz-4a

ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

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The diagram on [Page 1](#) shows the two clock domains that make up the ADSP-2148x processors. The core clock domain contains the following features:

- Two processing elements (PE_x, PE_y), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (5 Mbit) and mask-programmable ROM (4 Mbit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-2148x on [Page 1](#) also shows the peripheral clock domain (also known as the I/O processor) which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 memory-to-memory (MTM) unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP/PDAP) for serial and parallel interconnects, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface (TWI), one UART, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG), pulse width modulation (PWM), and a flexible signal routing unit (DPI SRU2).

As shown in the SHARC core block diagram on [Page 5](#), the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz.

FAMILY CORE ARCHITECTURE

The ADSP-2148x is code compatible at the assembly level with the ADSP-2147x, ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2148x shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x and ADSP-2116x SIMD SHARC processors, as shown in [Figure 2](#) and detailed in the following sections.

SIMD Computational Engine

The ADSP-2148x contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. SIMD mode allows the processor to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

SIMD mode also affects the way data is transferred between memory and the processing elements because twice the data bandwidth is required to sustain computational operation in the processing elements. Therefore, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each memory or register file access.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle and are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Timer

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

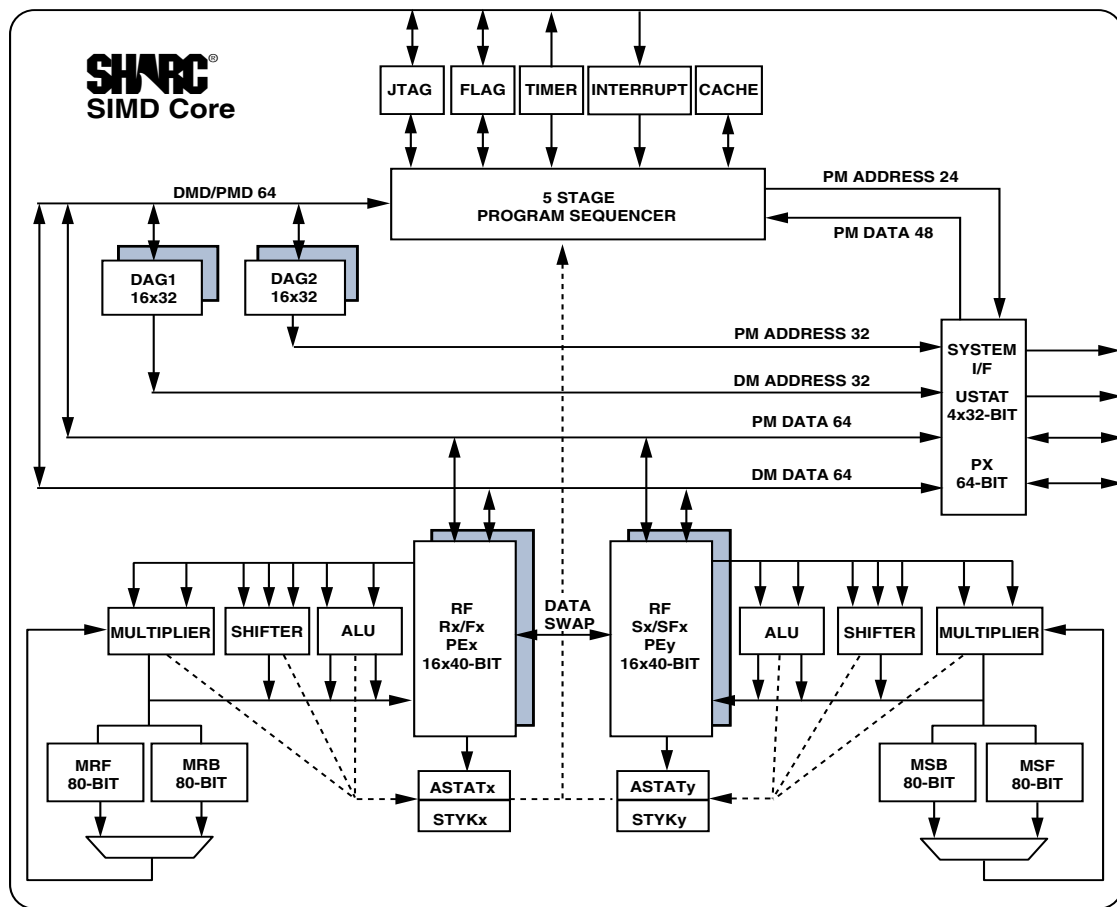


Figure 2. SHARC Core Block Diagram

Universal Registers

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all peripheral registers (control/status).

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-2148x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data. With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose

fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processor can conditionally execute a multiply, an add, and a

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Table 4. Internal Memory Space (5 MBits—ADSP-21486/ADSP-21487/ADSP-21489)¹

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	Extended Precision Normal or Instruction Word (48 Bits)	Normal Word (32 Bits)	Short Word (16 Bits)
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 EFFF	Block 0 SRAM 0x0008 C000–0x0009 3FFF	Block 0 SRAM 0x0009 2000–0x0009 DFFF	Block 0 SRAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 4000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 EFFF	Block 1 SRAM 0x000A C000–0x000B 3FFF	Block 1 SRAM 0x000B 2000–0x000B DFFF	Block 1 SRAM 0x0016 4000–0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B 4000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 3FFF	Block 2 SRAM 0x000C 0000–0x000C 5554	Block 2 SRAM 0x000C 0000–0x000C 7FFF	Block 2 SRAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0006 FFFF	Reserved 0x000C 5555–0x000D FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 3FFF	Block 3 SRAM 0x000E 0000–0x000E 5554	Block 3 SRAM 0x000E 0000–0x000E 7FFF	Block 3 SRAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 5555–0x000F FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

¹ Some ADSP-2148x processors include a customer-definable ROM block and are not reserved as shown on this table. Please contact your Analog Devices sales representative for additional details.

instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

ROM Based Security

The ADSP-2148x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features are available after the correct key is scanned.

On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2 × 64-bits, CCLK speed) and the IOD0/1 buses (2 × 32-bit, PCLK speed).

FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2148x family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

External Memory

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 6M words of external memory in bank 0 and 8M words of external memory in bank 1, bank 2, and bank 3.
- A SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in bank 0, and 64M words of external memory in bank 1, bank 2, and bank 3. NOTE: This feature is not available on the ADSP-21486 product.

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- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

Non-SDRAM external memory address space is shown in [Table 5](#).

Table 5. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	6M	0x0020 0000–0x007F FFFF
Bank 1	8M	0x0400 0000–0x047F FFFF
Bank 2	8M	0x0800 0000–0x087F FFFF
Bank 3	8M	0x0C00 0000–0x0C7F FFFF

External Port

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 176-lead LQFP, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and banks 1, 2, and 3 occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices at speeds up to f_{SDCLK} . Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$ – $\overline{MS3}$), and can be configured to contain between 4M bytes and 256M bytes of memory. SDRAM external memory address space is shown in [Table 6](#). NOTE: this feature is not available on the ADSP-21486 model.

Table 6. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on the SDRAM and AMI interfaces.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This removes the need to explicitly access the complimentary registers when the data is in external SDRAM memory.

VISA and ISA Access to External Memory

The SDRAM controller on the ADSP-2148x processors supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. [Table 7](#) shows the address ranges for instruction fetch in each mode.

Table 7. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000–0x005F FFFF
VISA (SW)	10M	0x0060 0000–0x00FF FFFF

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single-update mode or double-update mode. In single-update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double-update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

MediaLB

The automotive models of the ADSP-2148x processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive models, see [Automotive Products on Page 66](#).

Digital Applications Interface (DAI)

The digital applications interface (DAI) allows the connection of various peripherals to any of the DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes eight serial ports, four precision clock generators (PCG), a S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports (SPORTs)

The ADSP-2148x features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with

another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard serial mode
- Multichannel (TDM) mode
- I²S mode
- Packed I²S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, I²S or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, or the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter (SRC)

The asynchronous sample rate converter contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I²S, left-justified sample pair, or right-justified mode.

The IDP also provides a parallel data acquisition port (PDAP), which can be used for receiving parallel data. The PDAP port has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A, B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

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Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from non contiguous memory blocks.

FFT Accelerator

The FFT accelerator implements a radix-2 complex/real input, complex output FFT with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watchdog Timer

The watchdog timer is used to supervise the stability of the system software. When used in this way, software reloads the watchdog timer in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset, if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer. The watchdog timer resets both the core and the internal peripherals. Note that this feature is available on the 176-lead package only.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2148x boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2-0) pins in [Table 9](#) for the 176-lead package and [Table 10](#) for the 100-lead package.

Table 9. Boot Mode Selection, 176-Lead Package

BOOT_CFG2-0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI User Boot (for 8-bit Flash Boot)
011	No boot (processor executes from internal ROM after reset)
1xx	Reserved

Table 10. Boot Mode Selection, 100-Lead Package

BOOT_CFG1-0	Booting Mode
00	SPI Slave Boot
01	SPI Master Boot
10	Reserved
11	No boot (processor executes from internal ROM after reset)

The “Running Reset” feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the RESETOUT/RUNRSTIN pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the hardware reference.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal supply must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Static Voltage Scaling (SVS)

Some models of the ADSP-2148x feature Static Voltage Scaling (SVS) on the V_{DD_INT} power supply. (See the [Ordering Guide on Page 66](#) for model details.) This voltage specification technique can provide significant performance benefits including 450 MHz core frequency operation without a significant increase in power.

SVS optimizes the required V_{DD_INT} voltage for each individual device to enable enhanced operating frequency up to 450 MHz. The optimized SVS voltage results in a reduction of maximum I_{DD_INT} which enables 450 MHz operation at the same or lower maximum power than 400 MHz operation at a fixed voltage supply. Implementation of SVS requires a specific voltage regulator circuit design and initialization code.

Refer to the Engineer-to-Engineer Note [Static Voltage Scaling for ADSP-2148x SHARC Processors \(EE-357\)](#) for further information. The EE-Note details the requirements and process to implement a SVS power supply system to enable operation up to 450 MHz. This applies only to specific products within the ADSP-2148x family which are capable of supporting 450 MHz operation.

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PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
ADDR ₂₃₋₀	I/O/T (ipu)	High-Z/ driven low (boot)	External Address. The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, and FLAGS ₁₅₋₈ (I/O) and PWM (O). After reset, all ADDR pins are in external memory interface mode and FLAG(0-3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the ADDR ₂₃₋₄ pins for parallel input data.
DATA ₁₅₋₀	I/O/T (ipu)	High-Z	External Data. The data pins can be multiplexed to support the external memory interface data (I/O), and FLAGS ₇₋₀ (I/O).
AMI_ACK	I (ipu)		Memory Acknowledge. External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	Memory Select Lines 0-1. These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS}_1$ pin can be used in EPORT/FLASH boot mode. For more information, see the hardware reference.
$\overline{AMI_RD}$	O/T (ipu)	High-Z	AMI Port Read Enable. $\overline{AMI_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI_WR}$	O/T (ipu)	High-Z	AMI Port Write Enable. $\overline{AMI_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/ $\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	FLAG0/Interrupt Request0.
FLAG1/ $\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	FLAG1/Interrupt Request1.
FLAG2/ $\overline{IRQ2}/\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	FLAG2/Interrupt Request2/Memory Select2.
FLAG3/TMREXP/ $\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	FLAG3/Timer Expired/Memory Select3.

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 k Ω –63 k Ω . The range of an ipd resistor can be between 31 k Ω –85k Ω . The three-state voltage of ipu pads will not reach to the full V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTTL compliant with the exception of the thermal diode pins.

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Reset

Table 21. Reset

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{WRST}^1 $\overline{RESET}$ Pulse Width Low	$4 \times t_{CK}$		ns
t_{SRST} $\overline{RESET}$ Setup Before CLKIN Low	8		ns

¹ Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 μs while $\overline{RESET}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

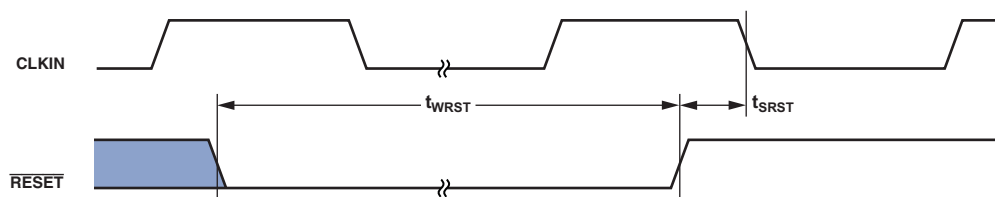


Figure 8. Reset

Running Reset

The following timing specification applies to $\overline{RESETOUT}/\overline{RUNRSTIN}$ pin when it is configured as $\overline{RUNRSTIN}$.

Table 22. Running Reset

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{WRUNRST}$ Running $\overline{RESET}$ Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$ Running $\overline{RESET}$ Setup Before CLKIN High	8		ns

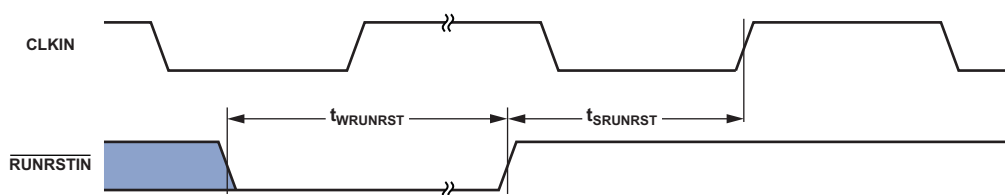


Figure 9. Running Reset

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Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 23. Interrupts

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{IPW} $\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{\text{CLK}} + 2$		ns

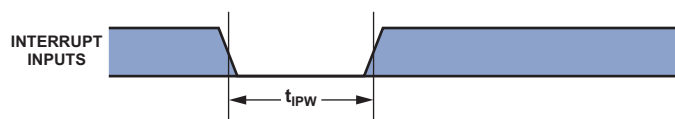


Figure 10. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
t_{WCTIM} TMREXP Pulse Width	$4 \times t_{\text{CLK}} - 1$		ns



Figure 11. Core Timer

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Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
t_{PWO} Timer Pulse Width Output	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

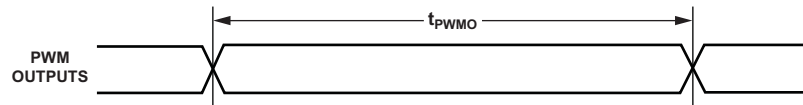


Figure 12. Timer PWM_OUT Timing

Timer WIDTH_CAP Timing

The following timing specification applies to timer0 and timer1, and in WIDTH_CAP (pulse-width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 26. Timer Width Capture Timing

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{PWI} Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

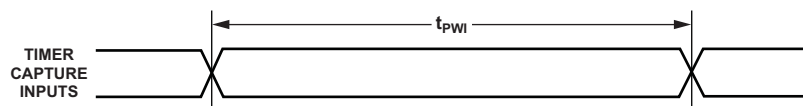


Figure 13. Timer Width Capture Timing

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Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's

inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 29. Precision Clock Generator (Direct Pin Routing)

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{PCGIW} Input Clock Period	$t_{CLK} \times 4$		ns
t_{STRIG} PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG} PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
<i>Switching Characteristics</i>			
t_{DPCGIO} PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	10	ns
$t_{DTRIGCLK}$ PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$10 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$ PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$10 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}^1 Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

$D = FSxDIV$, $PH = FSxPHASE$. For more information, see the "Precision Clock Generators" chapter in the hardware reference.

¹Normal mode of operation.

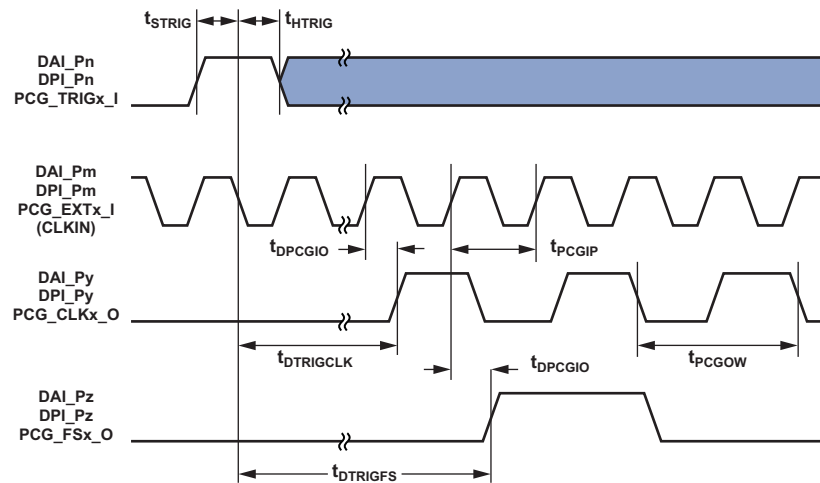


Figure 16. Precision Clock Generator (Direct Pin Routing)

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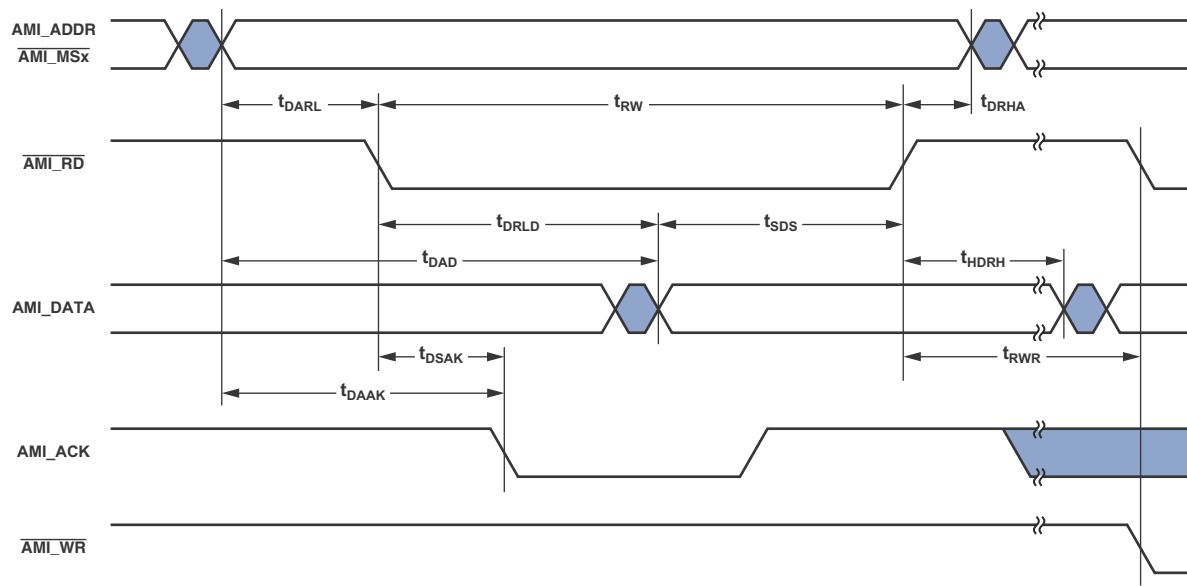


Figure 19. AMI Read

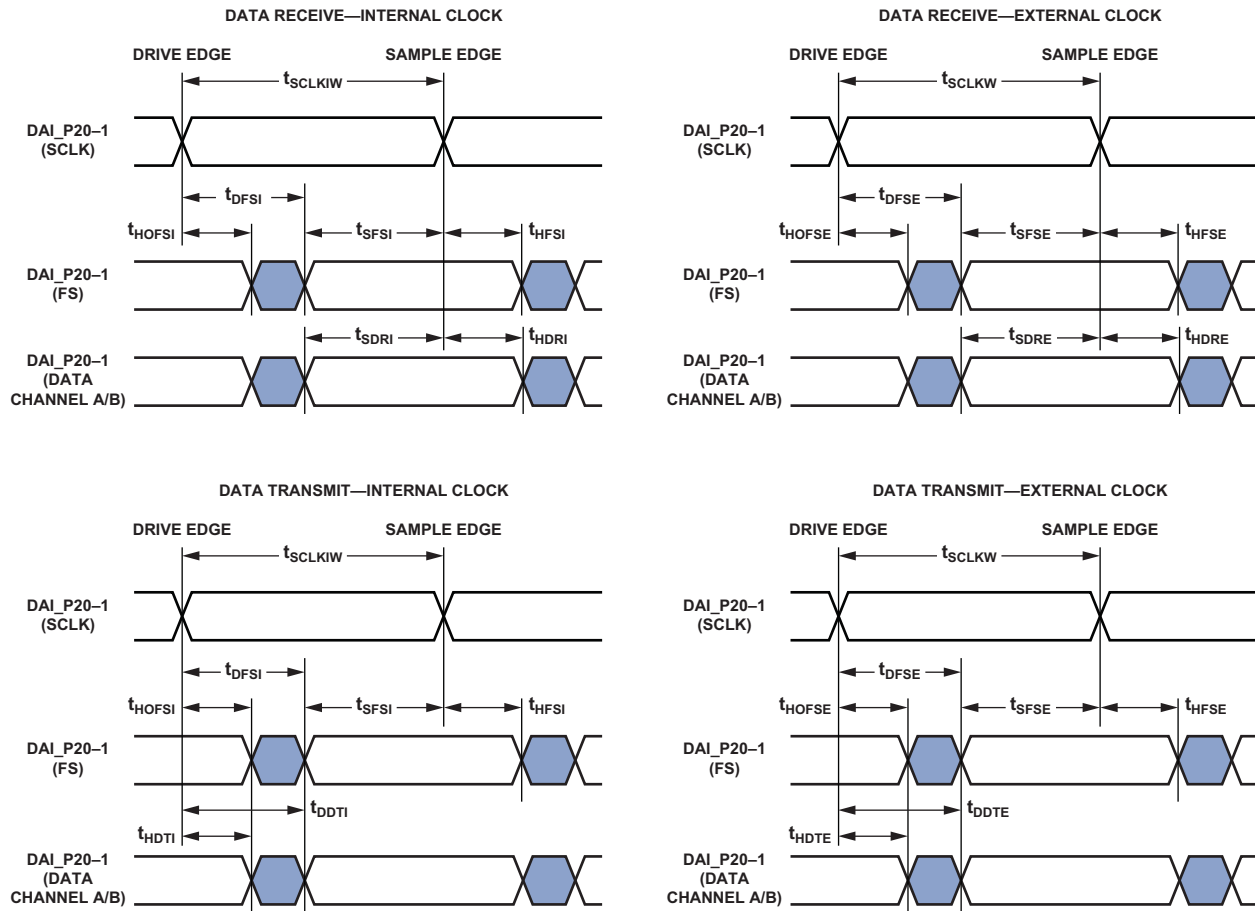


Figure 21. Serial Ports

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Table 36. Serial Ports—External Late Frame Sync

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
$t_{DDTLFSE}^1$ Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		8.5	ns
$t_{DDTENFS}^1$ Data Enable for MCE = 1, MFD = 0	0.5		ns

¹The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified, as well as DSP serial mode, and MCE = 1, MFD = 0.

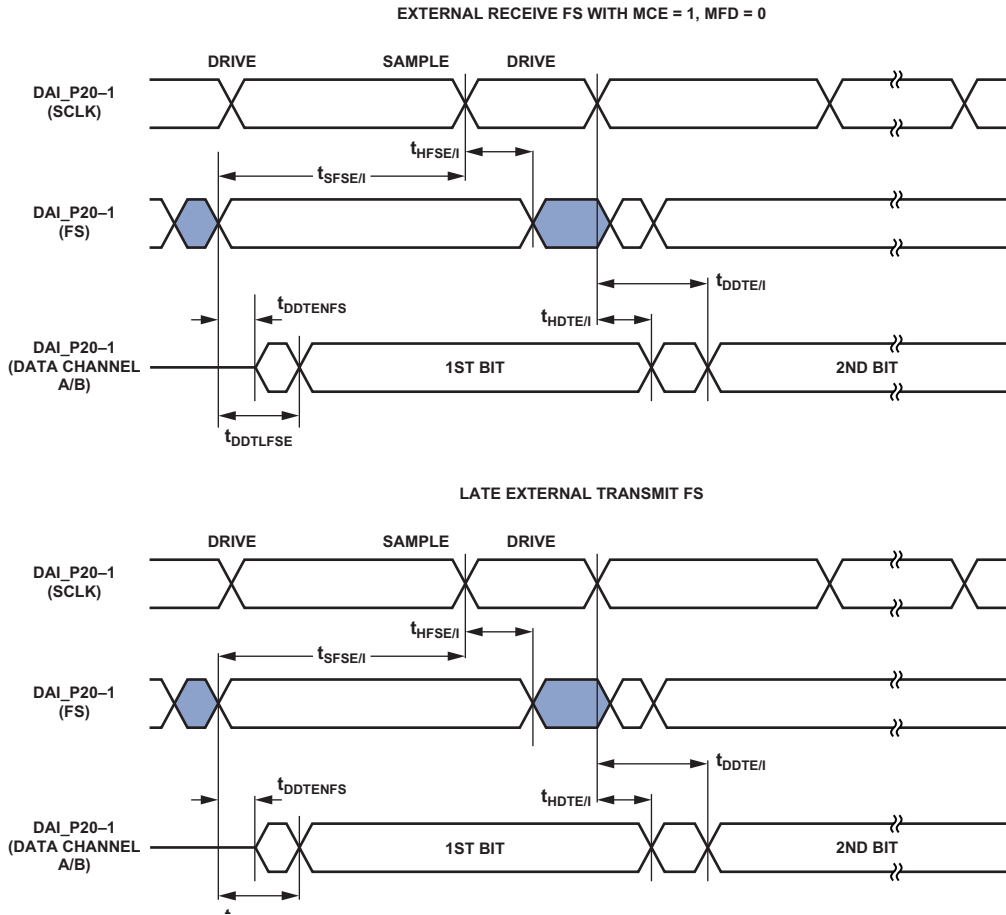


Figure 22. External Late Frame Sync¹

¹This figure reflects changes made to support left-justified mode.

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Table 37. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
<i>Switching Characteristics</i>				
t_{DDTEN}^1	Data Enable from External Transmit SCLK	2		ns
t_{DDTTE}^1	Data Disable from External Transmit SCLK		11.5	ns
t_{DDTIN}^1	Data Enable from Internal Transmit SCLK	-1.5		ns

¹Referenced to drive edge.

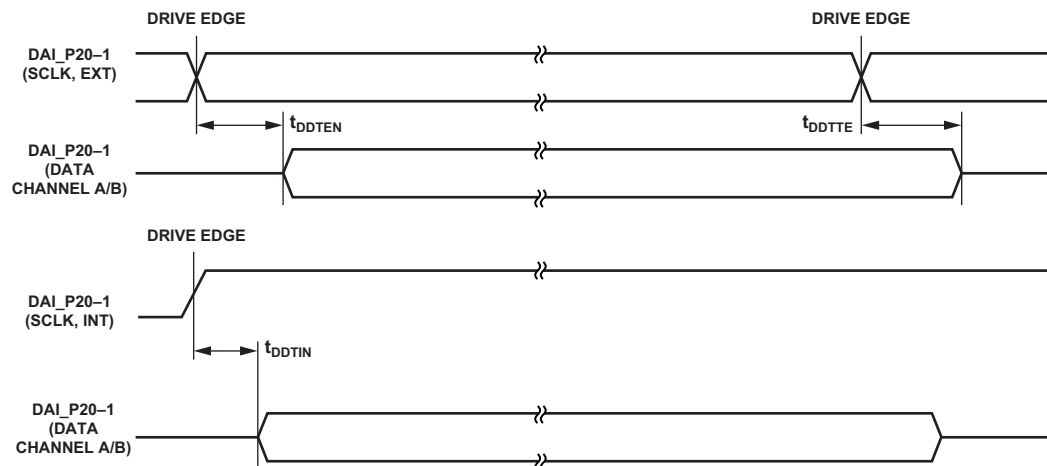


Figure 23. Serial Ports—Enable and Three-State

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S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the $512 \times \text{FS}$ clock.

Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
<i>Switching Characteristics</i>				
t_{DFSI}	Frame Sync Delay After Serial Clock		5	ns
t_{HOFSI}	Frame Sync Hold After Serial Clock	-2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	-2		ns
t_{SCLKIW}^1	Transmit Serial Clock Width	$8 \times t_{\text{PCLK}} - 2$		ns

¹ SCLK frequency is $64 \times \text{FS}$ where FS = the frequency of frame sync.

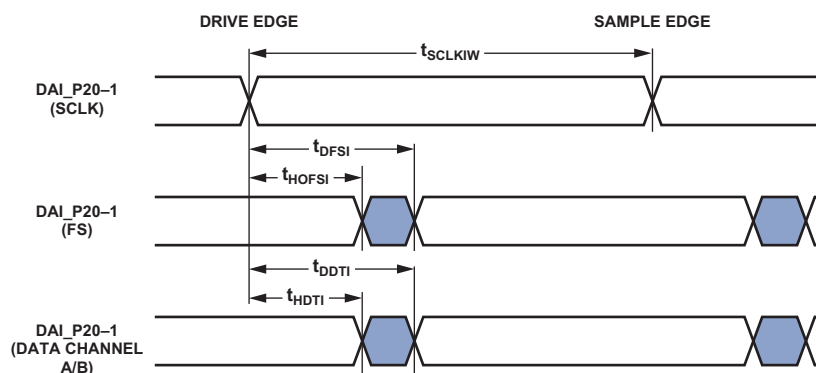


Figure 34. S/PDIF Receiver Internal Digital PLL Mode Timing

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OUTPUT DRIVE CURRENTS

Figure 41 shows typical I-V characteristics for the output drivers of the ADSP-2148x, and Table 55 shows the pins associated with each driver. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 55. Driver Types

Driver Type	Associated Pins
A	FLAG[0–3], AMI_ADDR[0–23], DATA[0–15], AMI_RD, AMI_WR, AMI_ACK, $\overline{MS}[1–0]$, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, $\overline{SDDQM}$, $\overline{SDCKE}$, SDA10, $\overline{EMU}$, $\overline{TDO}$, $\overline{RESETOUT}$, DPI[1–14], DAI[1–20], $\overline{WDTRSTO}$, MLBDAT, MLBSIG, MLBSO, MLBDO, MLBCLK
B	SDCLK

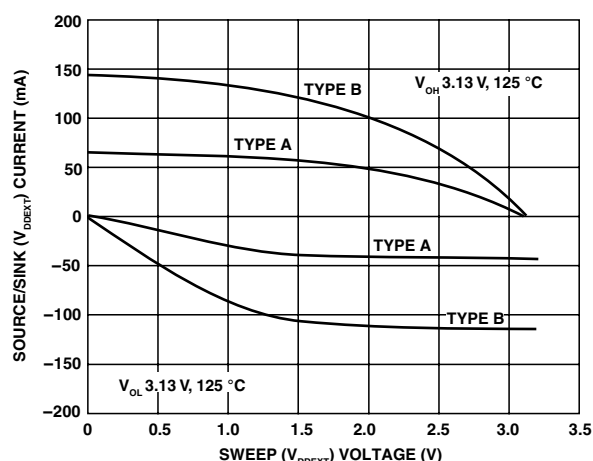


Figure 41. Typical Drive at Junction Temperature

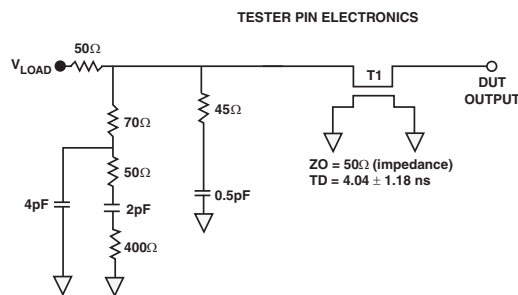
TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 21 on Page 26 through Table 54 on Page 54. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 42.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 43. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.



Figure 43. Voltage Reference Levels for AC Measurements



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.
ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 42. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 42). Figure 46 and Figure 47 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 44 through Figure 47 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

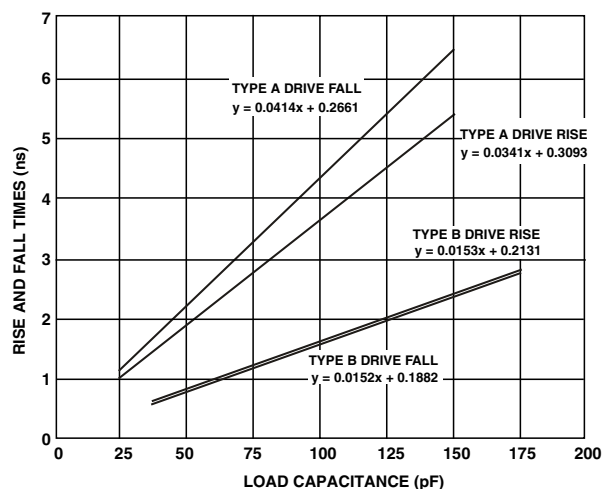


Figure 44. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Max)

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Note that the thermal characteristics values provided in [Table 56](#) and [Table 57](#) are modeled values.

Table 56. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.8	°C/W
θ_{JMA}	Airflow = 1 m/s	15.4	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.24	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.37	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.51	°C/W

Table 57. Thermal Characteristics for 176-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	16.9	°C/W
θ_{JMA}	Airflow = 1 m/s	14.6	°C/W
θ_{JMA}	Airflow = 2 m/s	13.8	°C/W
θ_{JC}		2.3	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.21	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.32	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.41	°C/W

Thermal Diode

The ADSP-2148x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times \ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann's constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

[Table 58](#) contains the thermal diode specifications using the transistor model.

Table 58. Thermal Diode Parameters – Transistor Model¹

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}^2	Forward Bias Current	10		300	μA
I_E	Emitter Current	10		300	μA
$n_Q^{3,4}$	Transistor Ideality	1.012	1.015	1.017	
$R_T^{3,5}$	Series Resistance	0.12	0.2	0.28	Ω

¹ See Engineer-to-Engineer Note [Using the On-Chip Thermal Diode on Analog Devices Processors \(EE-346\)](#).

² Analog Devices does not recommend operation of the thermal diode under reverse bias.

³ Specified by design characterization.

⁴ The ideality factor, n_Q , represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qV_{BE}/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).

⁵ The series resistance (R_T) can be used for more accurate readings as needed.

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176-LEAD LQFP_EP LEAD ASSIGNMENT

Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
NC	1	V _{DD_EXT}	45	DAI_P10	89	V _{DD_INT}	133
MS0	2	DPI_P08	46	V _{DD_INT}	90	FLAG0	134
NC	3	DPI_P07	47	V _{DD_EXT}	91	FLAG1	135
V _{DD_INT}	4	V _{DD_INT}	48	DAI_P20	92	FLAG2	136
CLK_CFG1	5	DPI_P09	49	V _{DD_INT}	93	GND	137
ADDR0	6	DPI_P10	50	DAI_P08	94	FLAG3	138
BOOT_CFG0	7	DPI_P11	51	DAI_P14	95	GND	139
V _{DD_EXT}	8	DPI_P12	52	DAI_P04	96	GND	140
ADDR1	9	DPI_P13	53	DAI_P18	97	V _{DD_EXT}	141
ADDR2	10	DPI_P14	54	DAI_P17	98	GND	142
ADDR3	11	DAI_P03	55	DAI_P16	99	V _{DD_INT}	143
ADDR4	12	NC	56	DAI_P12	100	TRST	144
ADDR5	13	V _{DD_EXT}	57	DAI_P15	101	GND	145
BOOT_CFG1	14	NC	58	V _{DD_INT}	102	EMU	146
GND	15	NC	59	DAI_P11	103	DATA0	147
ADDR6	16	NC	60	V _{DD_EXT}	104	DATA1	148
ADDR7	17	NC	61	V _{DD_INT}	105	DATA2	149
NC	18	V _{DD_INT}	62	BOOT_CFG2	106	DATA3	150
NC	19	NC	63	V _{DD_INT}	107	TDO	151
ADDR8	20	NC	64	AMI_ACK	108	DATA4	152
ADDR9	21	V _{DD_INT}	65	GND	109	V _{DD_EXT}	153
CLK_CFG0	22	NC	66	THD_M	110	DATA5	154
V _{DD_INT}	23	NC	67	THD_P	111	DATA6	155
CLKIN	24	V _{DD_INT}	68	V _{DD_THD}	112	V _{DD_INT}	156
XTAL	25	NC	69	V _{DD_INT}	113	DATA7	157
ADDR10	26	WDTRSTO	70	V _{DD_INT}	114	TDI	158
NC	27	NC	71	MS1	115	NC	159*
V _{DD_EXT}	28	V _{DD_EXT}	72	V _{DD_INT}	116	V _{DD_EXT}	160
V _{DD_INT}	29	DAI_P07	73	WDT_CLKO	117	DATA8	161
ADDR11	30	DAI_P13	74	WDT_CLKIN	118	DATA9	162
ADDR12	31	DAI_P19	75	V _{DD_EXT}	119	DATA10	163
ADDR17	32	DAI_P01	76	ADDR23	120	TCK	164
ADDR13	33	DAI_P02	77	ADDR22	121	DATA11	165
V _{DD_INT}	34	V _{DD_INT}	78	ADDR21	122	DATA12	166
ADDR18	35	NC	79	V _{DD_INT}	123	DATA14	167
RESETOUT/RUNRSTIN	36	NC	80	ADDR20	124	DATA13	168
V _{DD_INT}	37	NC	81	ADDR19	125	V _{DD_INT}	169
DPI_P01	38	NC	82	V _{DD_EXT}	126	DATA15	170
DPI_P02	39	NC	83	ADDR16	127	NC	171
DPI_P03	40	V _{DD_EXT}	84	ADDR15	128	NC	172
V _{DD_INT}	41	V _{DD_INT}	85	V _{DD_INT}	129	RESET	173
DPI_P05	42	DAI_P06	86	ADDR14	130	TMS	174
DPI_P04	43	DAI_P05	87	AMI_WR	131	NC	175
DPI_P06	44	DAI_P09	88	AMI_RD	132	V _{DD_INT}	176
						GND	177**

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 (exposed pad) is the GND supply (see [Figure 50](#) and [Figure 51](#)) for the processor; this pad must be **robustly** connected to GND.