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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	46
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv31f512vlh12

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General

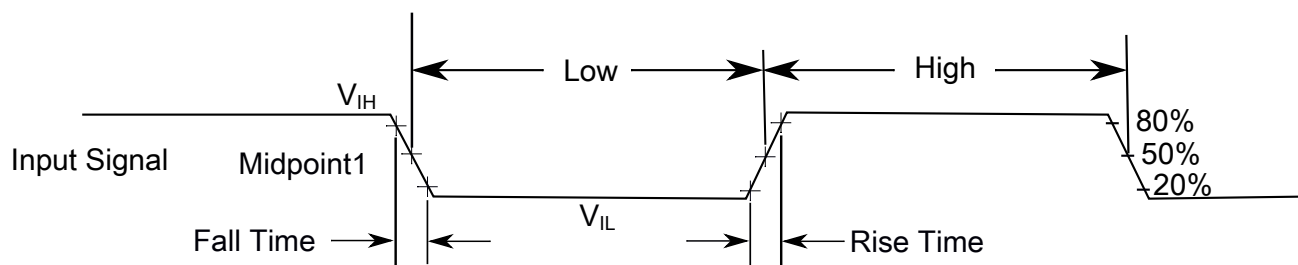
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	169	mA
V_{DIO}	Digital input voltage	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L}	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μ s	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -5\text{ mA}$	$V_{DD} - 0.5$	—	—	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -2.5\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
V_{OH}	Output high voltage — High drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -20\text{ mA}$	$V_{DD} - 0.5$	—	—	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -10\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 5\text{ mA}$	—	—	0.5	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 2.5\text{ mA}$	—	—	0.5	V	
V_{OL}	Output low voltage — High drive pad except RESET_B					
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$	—	—	0.5	V	1
	$1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 10\text{ mA}$	—	—	0.5	V	
V_{OL}	Output low voltage — RESET_B					

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V @ -40°C to 25°C	—	0.73	1.42	μA	
	@ 70°C	—	1.8	3.90	μA	
	@ 85°C	—	3.0	5.25	μA	
	@ 105°C	—	5.9	10.80	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	—	0.43	0.55	μA	
	@ 70°C	—	1.4	2.45	μA	
	@ 85°C	—	2.6	4.00	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.14	0.24	μA	
	@ 70°C	—	1.1	2.15	μA	
	@ 85°C	—	2.3	3.85	μA	
I _{DD_VLLS0}	@ 105°C	—	5.1	9.00	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. Cache on and prefetch on, low compiler optimization.
4. Coremark benchmark compiled using IAR 7.2 with optimization level low.
5. 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
6. 80 MHz core and system clock, 40 MHz bus clock, and 26.67 MHz flash clock. MCG configured for PEE mode. Compute operation.
7. 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
8. 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
9. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. Compute operation.
10. 25MHz core and system clock, 25MHz bus clock, and 25MHz FlexBus and flash clock. MCG configured for FEI mode.
11. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
12. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
13. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
14. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.

Table 6. Low power mode peripheral adders—typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I _{48MIRC}	48 Mhz internal reference clock	350	350	350	350	350	350	μA
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

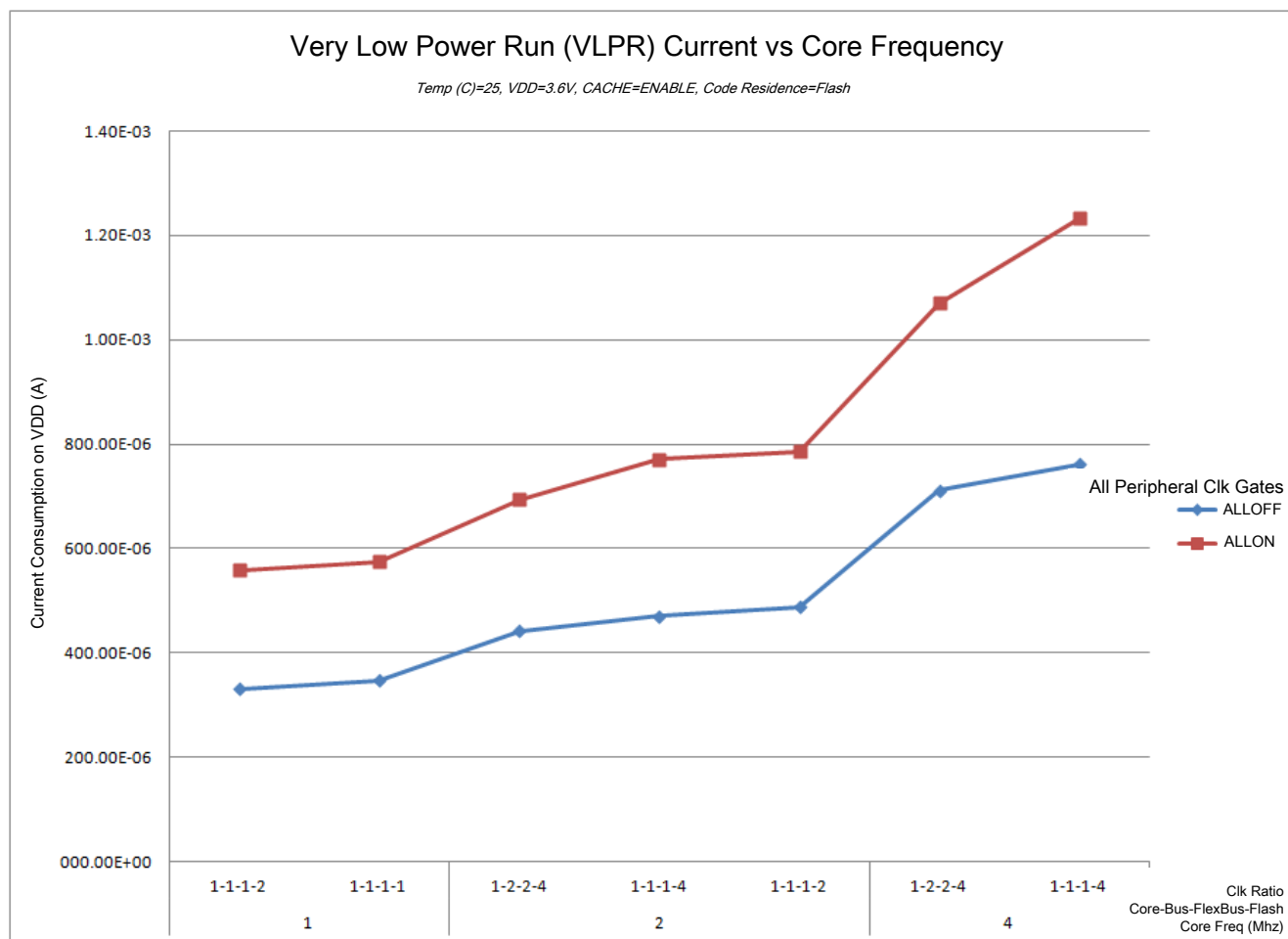


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 64 LQFP package

Parameter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V _{EME}	Device configuration, test conditions and EM testing per standard IEC 61967-2. Supply voltages: • VDD = 3.3 V Temp = 25°C	FSYS = 120 MHz FBUS = 60 MHz External crystal = 8 MHz	150 kHz–50 MHz	14	dBuV	1, 2, 3
			50 MHz–150 MHz	23		
			150 MHz–500 MHz	23		
			500 MHz–1000 MHz	9		
			IEC level	L		4

- Measurements were made per IEC 61967-2 while the device was running typical application code.
- Measurements were performed on a similar 64LQFP device.
- The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	−40	125	°C	
T_A	Ambient temperature	−40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J . The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

2.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	61	67	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	48	48	°C/W	2
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	51	55	°C/W	3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	42	°C/W	3
—	$R_{\theta JB}$	Thermal resistance, junction to board	34	31	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	16	16	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	°C/W	6

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 12. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation Serial wire debug	0	33	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width Serial wire debug	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

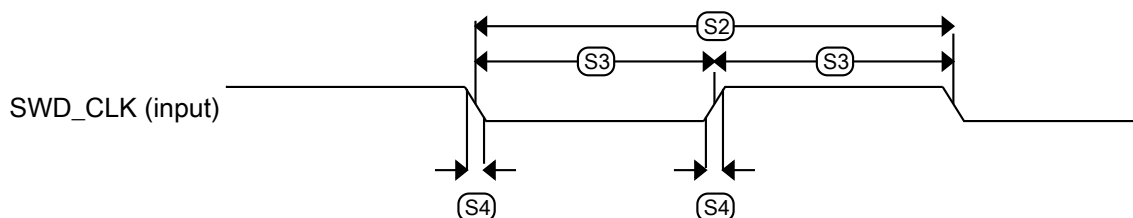


Figure 5. Serial wire clock input timing

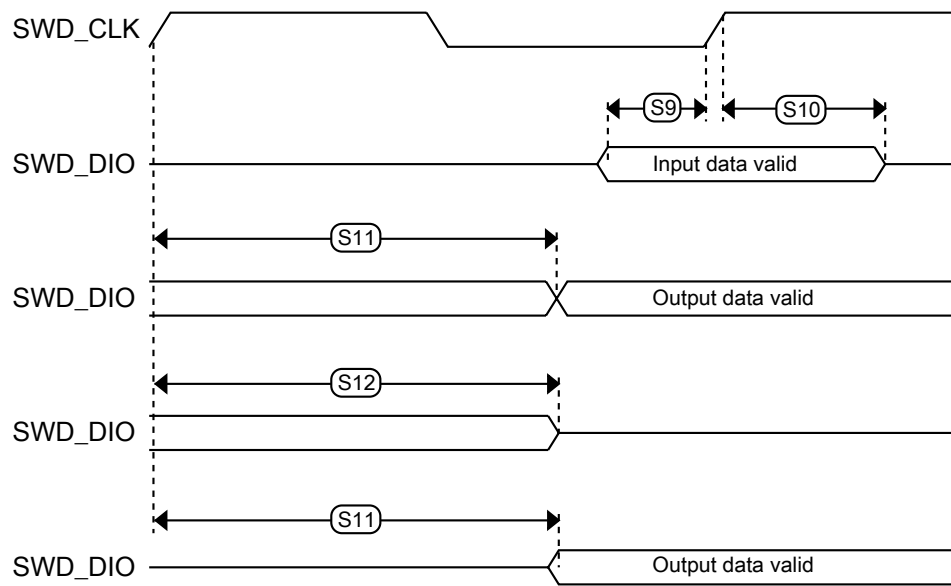


Figure 6. Serial wire data timing

3.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns

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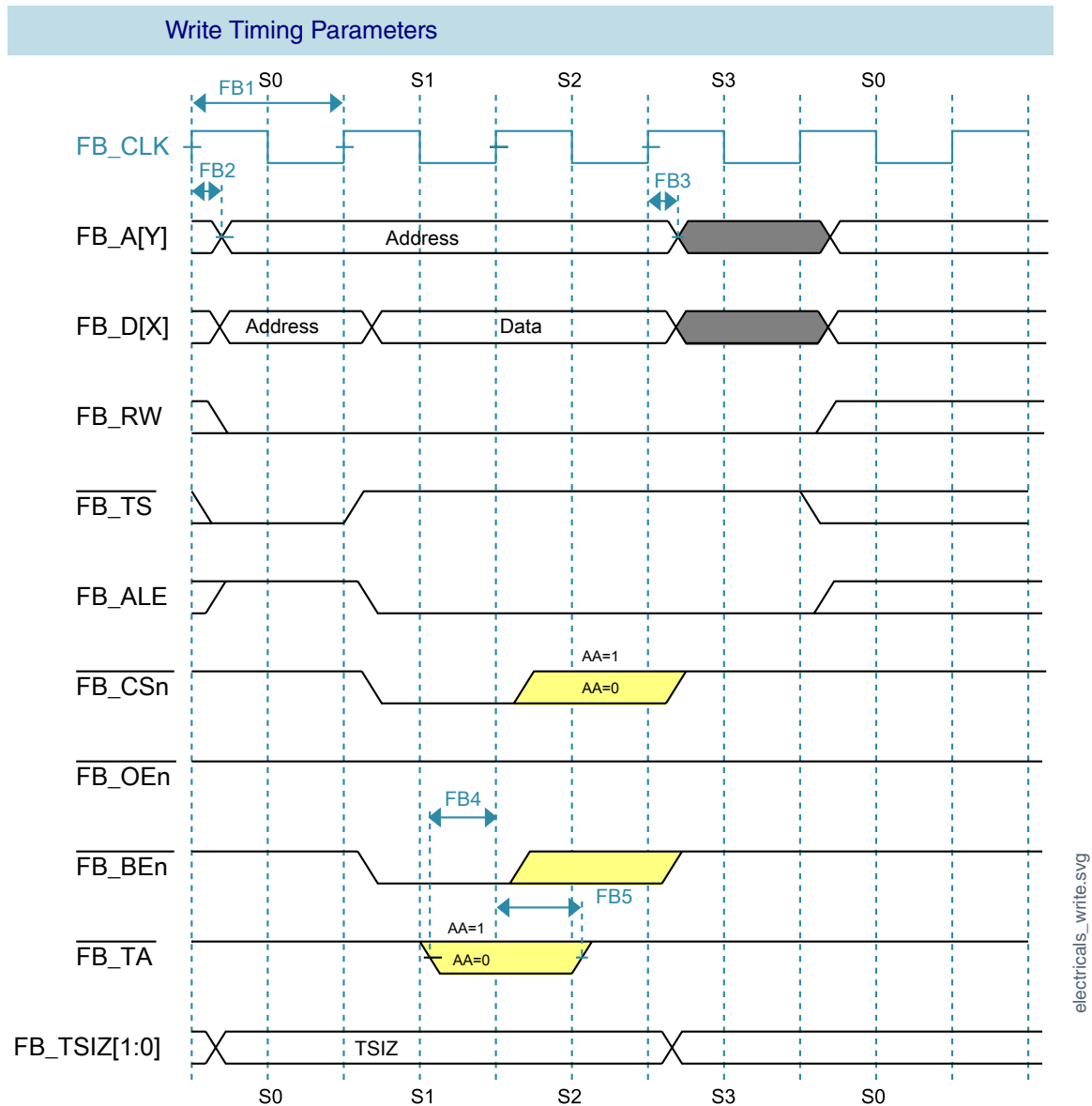


Figure 13. FlexBus write timing diagram

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

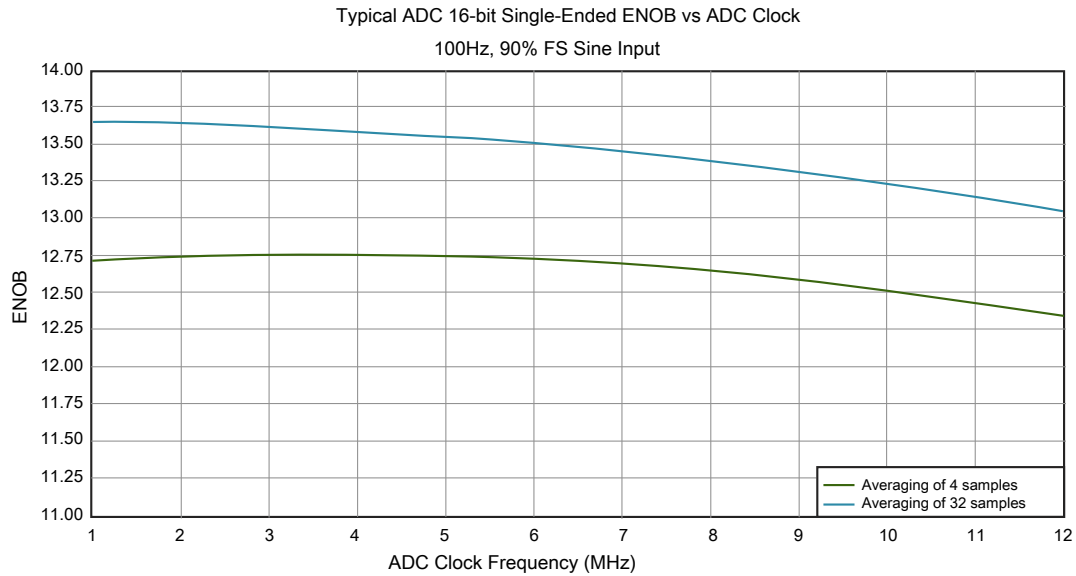


Figure 16. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 28. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μ A
I_{DDLs}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μ A
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹ - CR0[HYSTCTR] = 00 - CR0[HYSTCTR] = 01 - CR0[HYSTCTR] = 10 - CR0[HYSTCTR] = 11	—	5 10 20 30	—	mV mV mV mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

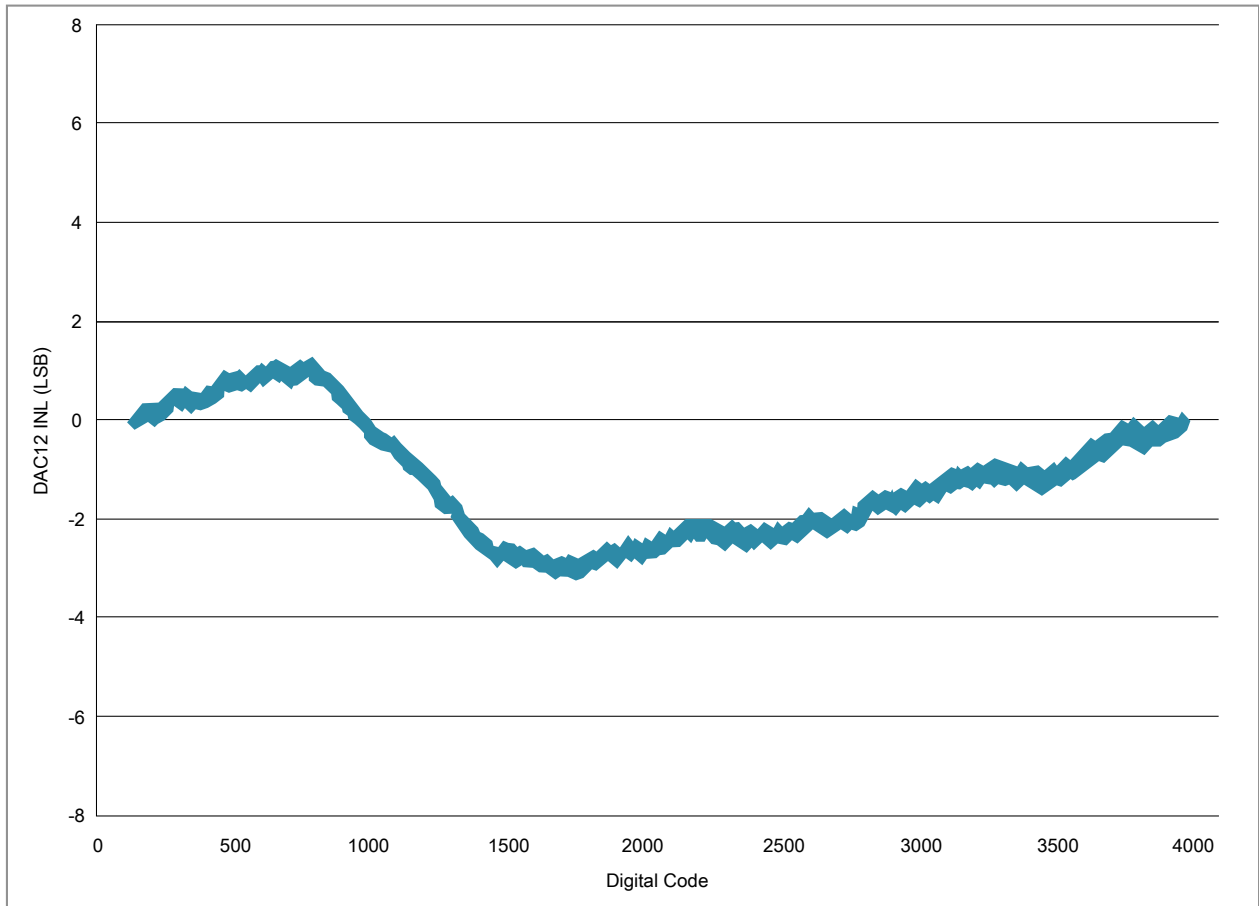


Figure 19. Typical INL error vs. digital code

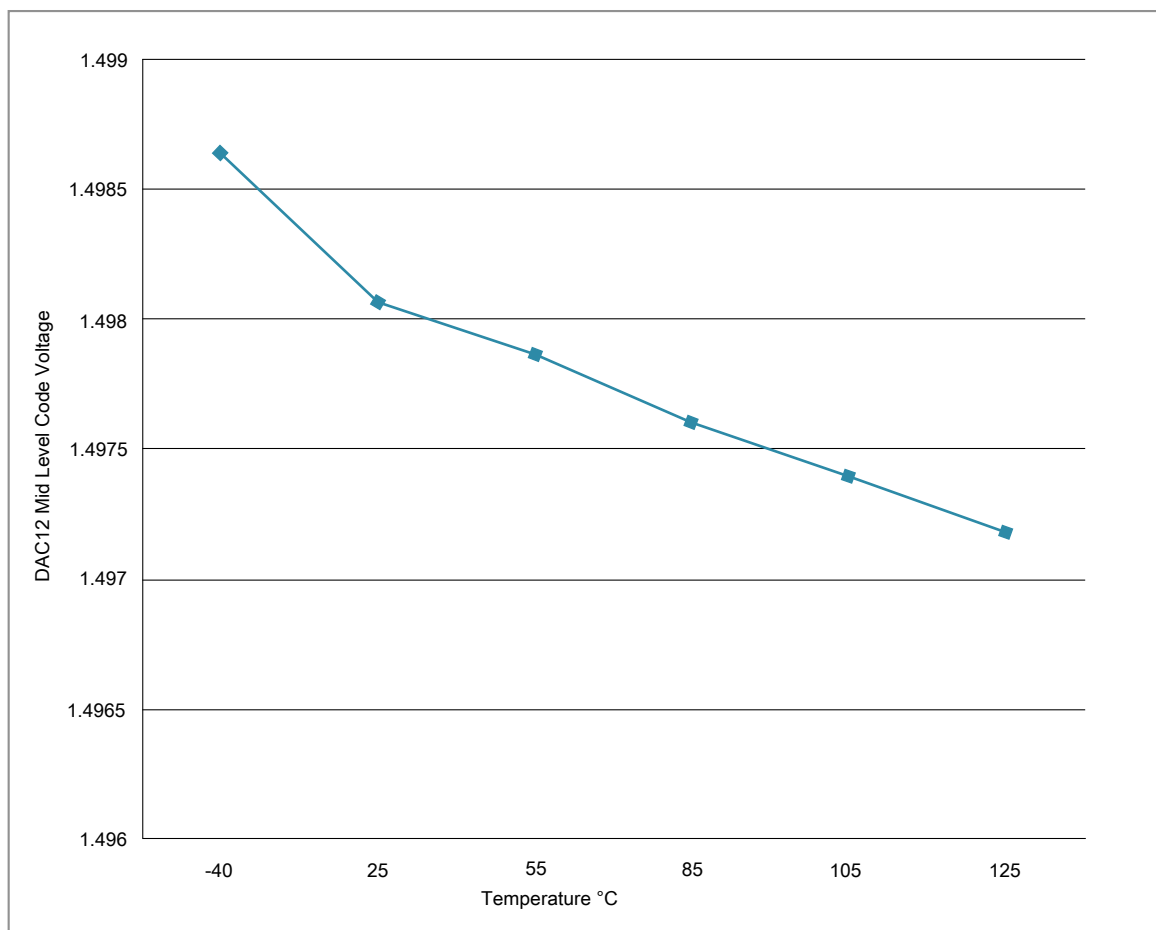


Figure 20. Offset at half scale vs. temperature

3.6.4 Voltage reference electrical specifications

Table 31. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

3.8.1 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 35. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

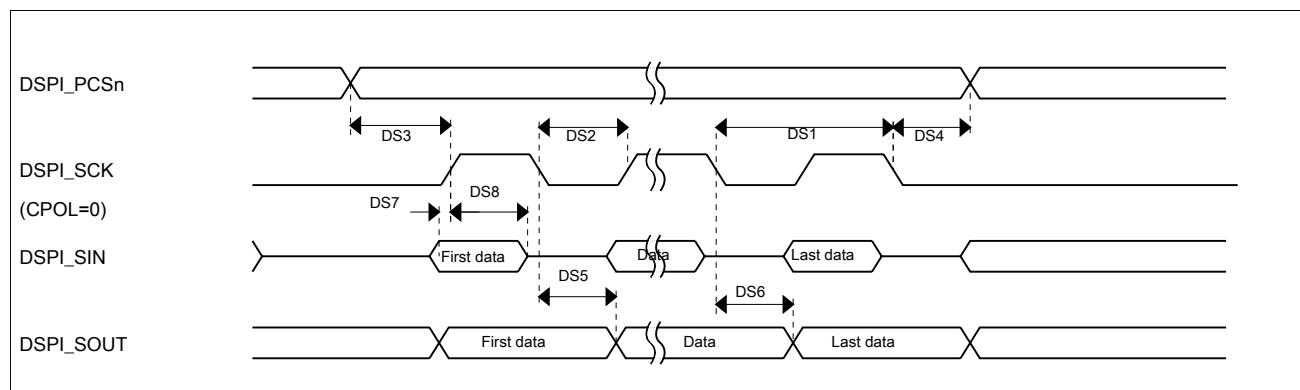
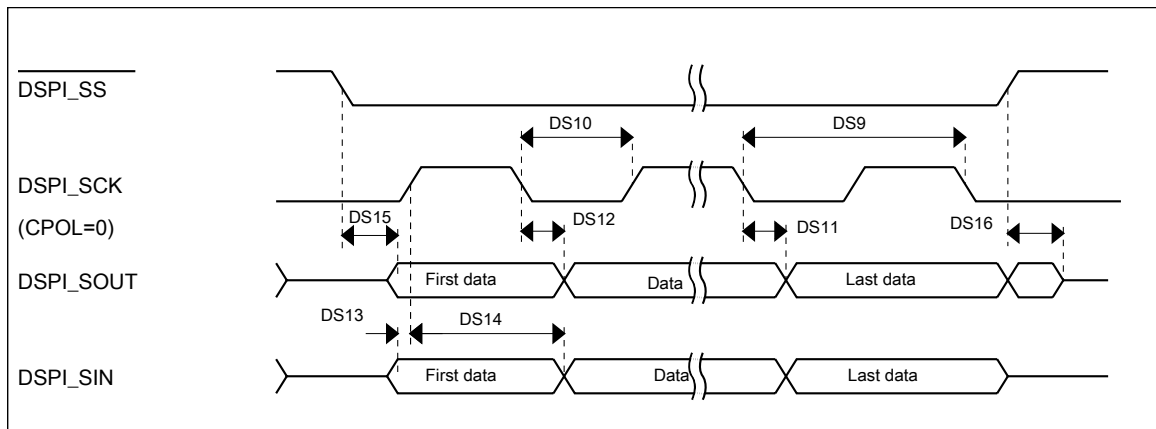


Figure 21. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	25	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	25	ns

**Figure 24. DSPI classic SPI timing — slave mode**

3.8.3 Inter-Integrated Circuit Interface (I²C) timing

Table 39. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD} ; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t_{SU} ; STA	4.7	—	0.6	—	μs

Table continues on the next page...

Table 39. I²C timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Data hold time for I ² C bus devices	t _{HD} ; DAT	0 ²	3.45 ³	0 ⁴	0.9 ²	μs
Data set-up time	t _{SU} ; DAT	250 ⁵	—	100 ^{3, 6}	—	ns
Rise time of SDA and SCL signals	t _r	—	1000	20 + 0.1C _b ⁷	300	ns
Fall time of SDA and SCL signals	t _f	—	300	20 + 0.1C _b ⁶	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t _{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 40. I²C 1 Mbps timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f _{SCL}	0	1 ¹	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	0.26	—	μs
LOW period of the SCL clock	t _{LOW}	0.5	—	μs
HIGH period of the SCL clock	t _{HIGH}	0.26	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	0.26	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0	—	μs
Data set-up time	t _{SU} ; DAT	50	—	ns
Rise time of SDA and SCL signals	t _r	20 + 0.1C _b ²	120	ns
Fall time of SDA and SCL signals	t _f	20 + 0.1C _b ²	120	ns
Set-up time for STOP condition	t _{SU} ; STO	0.26	—	μs
Bus free time between STOP and START condition	t _{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
69	—	PTB23	DISABLED		PTB23		SPI0_PCS5		FB_AD28			
70	43	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14	FTM0_FLT1	SPI0_PCS0	
71	44	PTC1/ LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13		LPUART0_RTS_b	
72	45	PTC2	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12		LPUART0_CTS_b	
73	46	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT		LPUART0_RX	
74	47	VSS	VSS	VSS								
75	48	VDD	VDD	VDD								
76	49	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT	LPUART0_TX	
77	50	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2		FB_AD10	CMP0_OUT	FTM0_CH2	
78	51	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG		FB_AD9		I2C0_SCL	
79	52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN			FB_AD8		I2C0_SDA	
80	53	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4		FB_AD7			
81	54	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5		FB_AD6	FTM2_FLT0		
82	55	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6		FB_AD5			
83	56	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7		FB_RW_b			
84	—	PTC12	DISABLED		PTC12				FB_AD27	FTM3_FLT0		
85	—	PTC13	DISABLED		PTC13				FB_AD26			
86	—	PTC14	DISABLED		PTC14				FB_AD25			
87	—	PTC15	DISABLED		PTC15				FB_AD24			
88	—	VSS	VSS	VSS								
89	—	VDD	VDD	VDD								
90	—	PTC16	DISABLED		PTC16		LPUART0_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_BLS15_8_b			
91	—	PTC17	DISABLED		PTC17		LPUART0_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_BLS7_0_b			
92	—	PTC18	DISABLED		PTC18		LPUART0_RTS_b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_BLS23_16_b			

Table 41. Recommended connection for unused analog interfaces (continued)

Pin Type		Short recommendation	Detailed recommendation
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10k Ω pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 KV31F Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

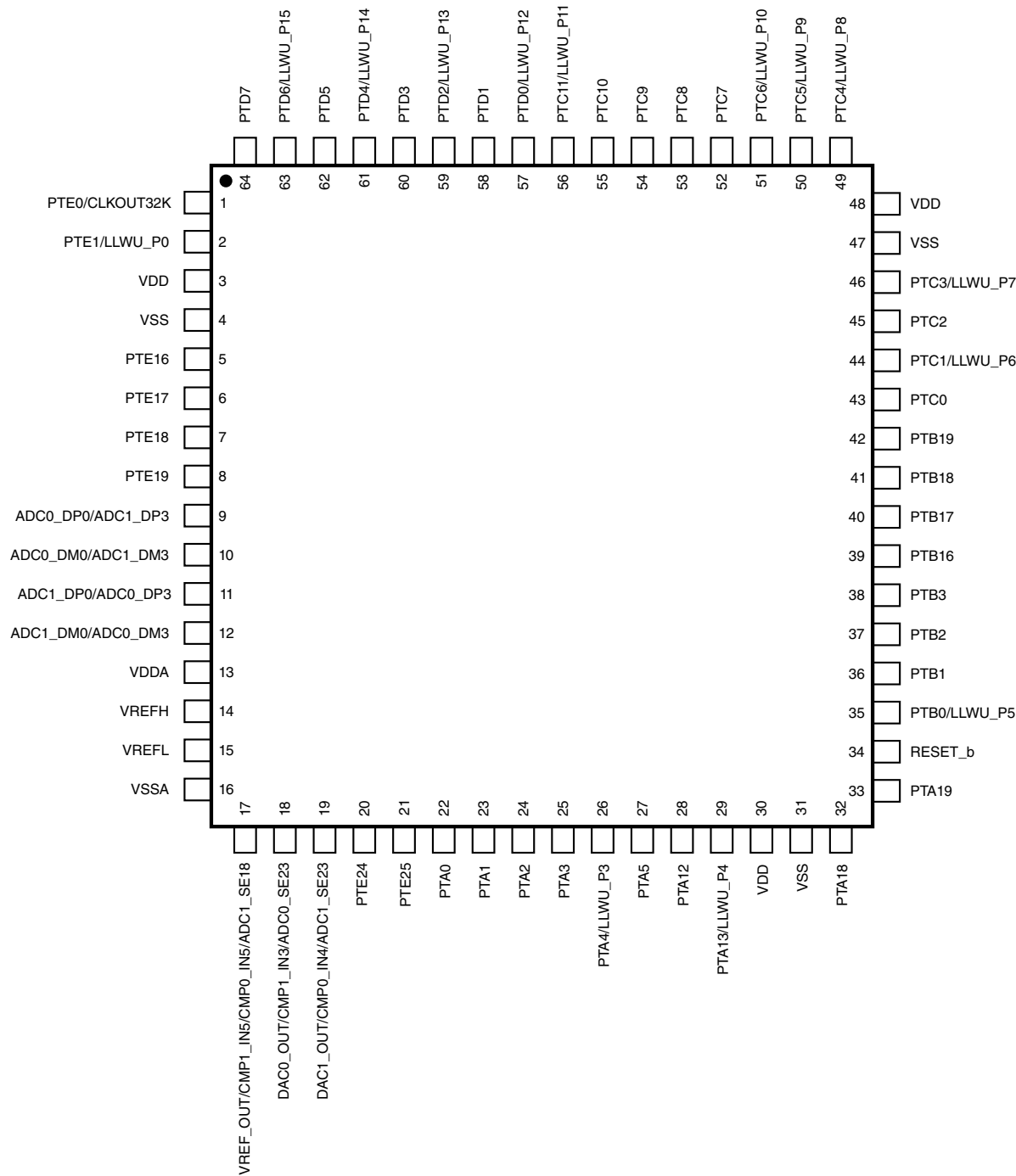


Figure 26. KV31F 64 LQFP Pinout Diagram (top view)

6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

6.2 Format

Part numbers for this device have the following format:

Q KV## A FFF R T PP CC S N

6.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
KV##	Kinetis V Series	KV3x: Cortex-M4 based MCU
A	Key attribute	- D = Cortex-M4 w/ DSP - F = Cortex-M4 w/ DSP and FPU
FFF	Program flash memory size	64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB
R	Silicon revision	(Blank) = Main - A = Revision after main
T	Temperature range (°C)	- V = -40 to 105 - C = -40 to 85
PP	Package identifier	- FM = 32 QFN (5 mm x 5 mm) - LF = 48 LQFP (7 mm x 7 mm) - LH = 64 LQFP (10 mm x 10 mm) - LL = 100 LQFP (14 mm x 14 mm) - MC = 121 XFBGA (8 mm x 8 mm) - DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm)
CC	Maximum CPU frequency (MHz)	10 = 100 MHz 12 = 120 MHz
S	Software type	- P = KMS-PMSM and BLDC (Blank) = Not software enabled
N	Packaging type	- R = Tape and reel (Blank) = Trays