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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c557e8efb-01-55

1 FEATURES

- 80C51 Central Processing Unit (CPU)
- 64 kbytes ROM (only P83C557E8)
- 64 kbytes EPROM (only P87C557E8)
- ROM/EPROM Code protection
- 2048 bytes RAM, expandable externally to 64 kbytes
- Two standard 16-bit timers/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog inputs and programmable autoscan
- Two 8-bit resolution, Pulse Width Modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip Watchdog Timer
- 15 interrupt sources with 2 priority levels (2 to 6 external sources possible)
- Phase-Locked Loop (PLL) oscillator with 32 kHz reference and software-selectable system clock frequency
- Seconds timer
- Software enable/disable of ALE output pulse
- Electromagnetic compatibility improvements
- Wake-up from Power-down by external or seconds interrupt
- Frequency range for 80C51-family standard oscillator: 3.5 to 16 MHz
- Extended temperature range: –40 to +85 C
- Supply voltage: 4.5 to 5.5 V.

2 GENERAL DESCRIPTION

The 8-bit microcontrollers P80C557E8, P83C557E8 and P87C557E8 - hereafter referred to as P8xC557E8 - are manufactured in an advanced CMOS process and are derivatives of the 80C51 microcontroller family.

The P8xC557E8 contains a volatile 2048 bytes read/write Data Memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual Digital-to-Analog Convertor (DAC), Pulse Width Modulated interface, two serial interfaces (UART and I^2C-bus), a Watchdog Timer, an on-chip oscillator and timing circuits.

The P8xC557E8 is available in 3 versions:

- P80C557E8: ROMless version
- P83C557E8: containing a non-volatile 64 kbytes mask programmable ROM
- P87C557E8: containing 64 kbytes programmable EPROM/OTP.

The P8xC557E8 is a control-oriented CPU with on-chip Program and Data Memory; it cannot be extended with external Program Memory. It can access up to 64 kbytes of external Data Memory. For systems requiring extra capability, the P8xC557E8 can be expanded using standard TTL compatible memories and peripherals.

In addition, the P8xC557E8 has two software selectable reduced power modes: Idle mode and Power-down mode. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.The Power-down mode can be terminated by an external reset, by the seconds interrupt and by any one of the two external interrupts; see Section 15.3.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic as well as bit-handling capabilities. The instruction set of the P8xC557E8 is the same as the 80C51 and consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16 MHz system clock, 58% of the instructions are executed in 0.75 µs and 40% in 1.5 µs. Multiply and divide instructions require 3 µs.

7 FUNCTIONAL DESCRIPTION

The P8xC557E8 is a stand-alone high-performance microcontroller designed for use in real time applications such as instrumentation, industrial control, medium to high-end consumer applications and specific automotive control applications.

In addition to the 80C51 standard functions, the device provides a number of dedicated hardware functions for these applications.

The P8xC557E8 is a control-oriented CPU with on-chip program and Data Memory, but it cannot be extended with external Program Memory. It can access up to 64 kbytes of external Data Memory. For systems requiring extra capability, the P8xC557E8 can be expanded using standard memories and peripherals.

The functional description of the device is described in:

- Chapter 8 “Memory organization”
- Chapter 9 “I/O facilities”
- Chapter 10 “Pulse Width Modulated outputs”
- Chapter 11 “Analog-to-Digital Converter (ADC)”
- Chapter 12 “Timers/counters”
- Chapter 13 “Serial I/O ports”
- Chapter 14 “Interrupt system”
- Chapter 15 “Reduced power modes”
- Chapter 16 “Oscillator circuits”
- Chapter 17 “Reset circuitry”.

8 MEMORY ORGANIZATION

The Central Processing Unit (CPU) manipulates operands in three memory spaces; these are the 64 kbytes external Data Memory, 2048 bytes internal Data Memory (consisting of 256 bytes standard RAM and 1792 bytes AUX-RAM) and the 64 kbytes internal or 64 kbytes external Program Memory (see Fig.4).

8.1 Program Memory

The Program Memory of the P8xC557E8 consists of 64 kbytes ROM or 64 kbytes EPROM. If, during reset, the $\overline{EA}$ pin was held HIGH, the P8xC557E8 always executes out of the internal Program Memory. If the $\overline{EA}$ pin was held LOW during reset the P8xC557E8 fetches all instructions from the external Program Memory. The $\overline{EA}$ input is latched during reset and is don't care after reset.

The internal Program Memory content is protected by setting a mask programmable security bit (ROM) or by the software programmable security bits (EPROM) respectively, i.e. it cannot be read out at any time by any test mode or by any instruction in the external Program Memory space. The MOVC instructions are the only ones which have access to program code in the internal or external Program Memory. The $\overline{EA}$ input is latched during reset and is don't care after reset. This implementation prevents from reading internal program code by switching from external Program Memory to internal Program Memory during MOVC instruction or an instruction that handles immediate data. Table 2 lists the access to the internal and external Program Memory with MOVC instructions whether the security feature has been activated or not.

Due to the maximum size of the internal Program Memory, the MOVC instructions can always operate either in the internal or in the external Program Memory.

Table 2 Memory access by the MOVC instruction

For code protection of the P87C557E8 see Section 23.2.

MOVC INSTRUCTION	PROGRAM MEMORY ACCESS	
	INTERNAL	EXTERNAL
MOVC in internal Program Memory	YES	NO(1)
MOVC in external Program Memory	NO(1)	YES

Note

1. Not applicable due to 64 kbytes internal Program Memory.

8.2 Internal Data Memory

The internal Data Memory is divided into three physically separated parts: 256 bytes of RAM, 1792 bytes of AUX-RAM, and a 128 bytes Special Function Registers (SFRs) area. These parts can be addressed each in a different way as described in Sections 8.2.1 to 8.2.2 and Table 3.

Table 3 Internal Data Memory map

MEMORY	LOCATION	ADDRESS MODE
RAM	0 to 127	Direct and indirect
	128 to 255	Indirect only
SFR	128 to 255	Direct only
AUX-RAM	0 to 1791	Indirect only with MOVX

8.2.1 RAM

- RAM 0 to 127 can be addressed directly and indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
- RAM 128 to 255 can only be addressed indirectly. Address pointers are R0 and R1 of the selected register bank.

Four register banks, each 8 registers wide, occupy locations 0 through 31 in the lower RAM area. Only one of these banks may be enabled at a time. The next 16 bytes, locations 32 through 47, contain 128 directly addressable bit locations. The stack can be located anywhere in the internal 256 bytes RAM. The stack depth is only limited by the available internal RAM space of 256 bytes (see Fig.6). All registers except the Program Counter and the four register banks reside in the Special Function Register address space.

8.2.2 Special Function Registers

The Special Function Registers can only be addressed directly in the address range from 128 to 255 (see Fig.7).

8.2.3 AUX-RAM

- AUX-RAM 0 to 1791 is indirectly addressable via page register (XRAMP) and MOVX-Ri instructions, unless it is disabled by setting ARD = 1 (see Fig.5). When executing from internal Program Memory, an access to AUX-RAM 0 to 1791 will not affect the ports P0, P2, P3.6 and P3.7.
- AUX-RAM 0 to 1791 is also indirectly addressable as external Data Memory locations 0 to 1791 via MOVX-Ri instructions, unless it is disabled by setting ARD = 1.

An access to external Data Memory locations higher than 1791 will be performed with the MOVX @DPTR instructions in the same way as in the 80C51 structure, so with P0 and P2 as data/address bus and P3.6 and P3.7 as write and read timing signals.

Note that the external Data Memory cannot be accessed with R0 and R1 as address pointer if the AUX-RAM is enabled (ARD = 0, default).

8.2.4 AUX-RAM Page Register (XRAMP)

The AUX-RAM Page Register is used to select one of seven 256-bytes pages of the internal 1792 bytes AUX-RAM for MOVX-accesses via R0 or R1. Its reset value is 'XXXX X000B'.

Table 4 AUX-RAM Page Register (address FAH)

7	6	5	4	3	2	1	0
XRAMPx	XRAMPx	XRAMPx	XRAMPx	XRAMPx	XRAMP2	XRAMP1	XRAMP0

Table 5 Description of XRAMP bits

BIT	SYMBOL	FUNCTION
7 to 3	XRAMPx	Reserved for future use. During read XRAMPx = undefined; a write operation must write logic 0s to these locations.
2 to 0	XRAMP2 to XRAMP0	AUX-RAM page select bits 2 to 0; see Table 6.

Table 6 Memory locations for all possible MOVX-accesses

X = don't care.

ARD[1]	XRAMP2	XRAMP1	XRAMP0	MEMORY LOCATIONS
MOVX @Ri,A and MOVX A,@Ri instructions access				
0	0	0	0	AUX-RAM locations 0 to 255 (reset condition)
0	0	0	1	AUX-RAM locations 256 to 511
0	0	1	0	AUX-RAM locations 512 to 767
0	0	1	1	AUX-RAM locations 768 to 1023
0	1	0	0	AUX-RAM locations 1024 to 1279
0	1	0	1	AUX-RAM locations 1280 to 1535
0	1	1	0	AUX-RAM locations 1536 to 1791
0	1	1	1	No valid memory access; reserved for future use
1	X	X	X	External RAM locations 0 to 255
MOVX @DPTR,A and MOVX A,@DPTR instructions access				
0	X	X	X	AUX-RAM locations 0 to 1791 (reset condition); External RAM locations 1792 to 65535
1	X	X	X	External RAM locations 0 to 65535

Note

1. ARD: AUX-RAM disable, is a bit in SFR PCON (bit PCON.6); see Section 15.5.

11 ANALOG-TO-DIGITAL CONVERTER (ADC)

11.1 ADC features

- 10-bit resolution
- 8 multiplexed analog inputs
- Programmable autoscan of the analog inputs
- Bit oriented 8-bit scan-select register to select analog inputs
- Continuous scan or one time scan configurable from 1 to 8 analog inputs
- Start of a conversion by software or with an external signal
- Eight 10-bit buffer registers, one register for each analog input channel
- Interrupt request after one channel scan loop
- Programmable prescaler (dividing by 2, 4, 6, 8) to adapt to different system clock frequencies
- Conversion time for one analog-to-digital conversion: 15 to 50 µs
- Differential non-linearity (DL_e): ±1 LSB
- Integral non-linearity (IL_e): ±2 LSB
- Offset error (OS_e): ±2 LSB
- Gain error (G_e): ±4%
- Absolute voltage error (A_e): 3 LSB
- Channel-to-channel matching (M_{ctc}): ±1 LSB
- Crosstalk between analog inputs (C_t): < 60 dB at 100 kHz
- Monotonic and no missing codes
- Separated analog (V_{DDA}, V_{SSA}) and digital (V_{DD}, V_{SS}) supply voltages
- Reference voltage at two special pins: $V_{ref(n)(A)}$ and $V_{ref(p)(A)}$.

For information on the ADC characteristics, refer to Chapter 21.

11.2 ADC functional description

The P8xC557E8 has a 10-bit successive approximation ADC with 8 multiplexed analog input channels, comprising a high input impedance comparator, DAC (built with 1024 series resistors and analog switches), registers and control logic. Input voltage range is from $V_{ref(n)(A)}$ (typical 0 V) to $V_{ref(p)(A)}$ (typical +5 V).

Each of the set of 8 buffer registers (10-bit wide) store the conversion results of the proper analog input channel.

Eleven Special Function Registers (SFRs) perform the user software interface to the ADC; see Table 14 for an overview of the ADC SFRs. In order to have a minimum of ADC service overhead in the microcontroller program, the ADC is able to operate autonomously within its user configurable autoscan function.

Figure 10 shows the functional diagram of the ADC.

11.3 ADC timing

A programmable prescaler is controlled by the user selectable bits ADPR1 and ADPR0 in SFR ADCON to adapt the conversion time for different microcontroller clock frequencies.

Table 13 shows conversion times (t_{ADC}) for one analog-to-digital conversion at some convenient system clock frequencies (f_{clk}) and ADC programmable prescaler divisors: **m**.
Conversion time $t_{ADC} = (6 \times m + 1)$ machine cycles.

A conversion time t_{ADC} consists of one sample time period (which equals two bit conversion times), 10 bit conversion time periods and one machine cycle to store the result. After result storage an extra initializing time period follows to select the next analog input channel (according to the contents of SFR ADPSS), before the input signal is sampled.Thus the time period between two adjacent conversions within an autoscan loop is larger than the pure time t_{ADC}. This autoscan cycle time is $(7 \times m)$ machine cycles.

At the start of an autoscan conversion the time between writing to SFR ADCON and the first analog input signal sampling depends on the current prescaler value (**m**) and the relative time offset between this write operation and the internal (divided) ADC clock. This gives a variation range for the analog-to-digital conversion start time of $(\frac{1}{2} \times m)$ machine cycles.

Table 13 Conversion time configuration examples

m	t_{ADC} (µs) at f_{CLK}:			
	6 MHz	8 MHz	12 MHz	16 MHz
2	26.00	19.50	13.00(1)	9.75(1)
4	50.00	37.50	25.00	18.75
6	74.00(1)	55.50(1)	37.00	27.75
8	98.00(1)	73.50(1)	49.00	36.75

Note

1. Prohibited t_{ADC} values; for t_{ADC} outside the limits of $15\ \mu s \leq t_{ADC} \leq 50\ \mu s$, the specified ADC characteristics are not guaranteed.

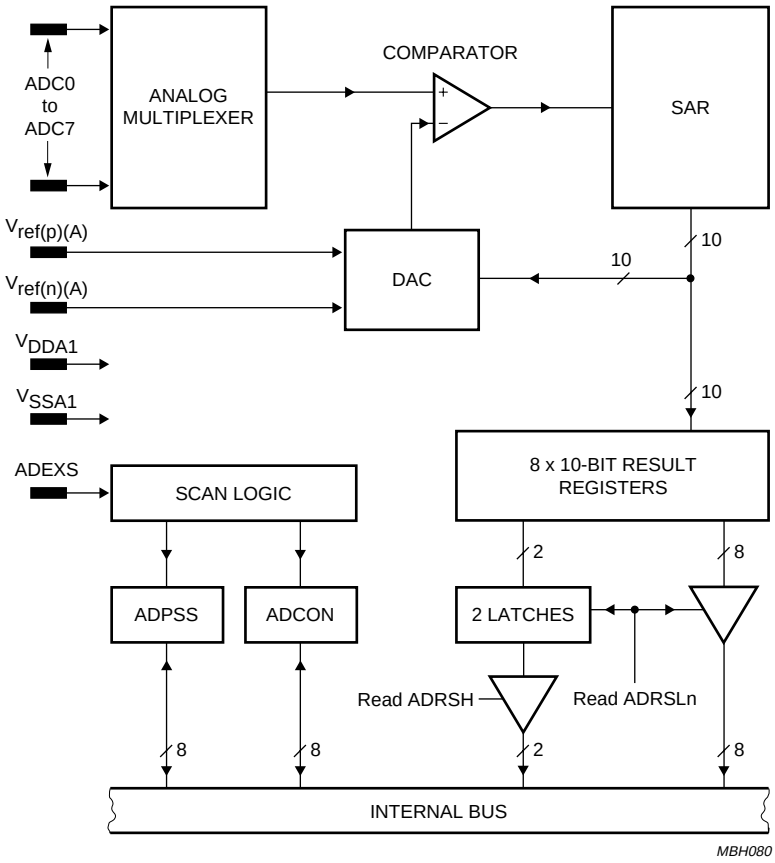


Fig.10 Functional diagram of ADC.

11.4 ADC configuration and operation

Every analog-to-digital conversion is an autoscan conversion. The two user selectable general operation modes are continuous scan and one-time scan mode.

The desired analog input port channel(s) for conversion is(are) selected by programming analog-to-digital input port scan-select bits in SFR ADPSS. An analog input channel is included in the autoscan loop if the corresponding bit in SFR ADPSS is logic 1, a channel is skipped if the corresponding bit in SFR ADPSS is logic 0.

An autoscan is always started according to the lowest bit position of SFR ADPSS that contains a logic 1.

An autoscan conversion is started by setting the flag ADSST in register ADCON either by software or by an external start signal at input pin ADEXS, if enabled.

Either no edge (external start totally disabled), a rising edge or/and a falling edge of ADEXS is selectable for external conversion start by the bits ADSRE and ADSFE in register ADCON.

After completion of an analog-to-digital conversion the 10-bit result is stored in the corresponding 10-bit buffer register. Then the next analog input is selected according to the next higher set bit position in ADPSS, converted and stored, and so on.

When the result of the last conversion of this autoscan loop is stored, the ADC interrupt flag ADINT (SFR ADCON), is set. It is not cleared by interrupt hardware - it must be cleared by software.

14.2 Interrupt Handling

The interrupt sources are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the previous machine cycle, the polling cycle will detect it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware generated LCALL is not blocked by any of the following conditions:

1. An interrupt of higher or equal priority level is already in progress.
2. The current machine cycle is not the final cycle in the execution of the instruction in progress. (No interrupt request will be serviced until the instruction in progress is completed.).
3. The instruction in progress is RETI or any access to the interrupt priority or interrupt enable registers. (No interrupt will be serviced after RETI or after a read or write to IP0, IP1, IE0, or IE1 until at least one other instruction has been subsequently executed.).

The polling cycle is repeated every machine cycle, and the values polled are the values present at S5P2 of the previous machine cycle. Note that if an interrupt flag is active but is not being responded to because of one of the above conditions, and if the flag is inactive when the blocking condition is removed, then the blocked interrupt will not be serviced. Thus, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate service routine. In some cases it also clears the flag which generated the interrupt, and in others it does not. It clears the Timer 0, Timer 1, and external interrupt flags.
An external interrupt flag (IE0 or IE1) is cleared only if it was transition-activated. All other interrupt flags are not cleared by hardware and must be cleared by the software.

The LCALL pushes the contents of the program counter on to the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to as shown in Table 60.

Execution proceeds from the vector address until the RETI instruction is encountered. The RETI instruction clears the ‘priority level active’ flip-flop that was set when this interrupt was acknowledged. It then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from where it was interrupted.

14.3 Interrupt Priority Structure

Each interrupt source can be assigned one of two priority levels: high and low. Interrupt priority levels are defined by the interrupt priority SFRs IP0 and IP1, which are described in Tables 66 and 68.

Interrupt priority levels are as follows:

logic 0 = low priority

logic 1 = high priority.

A low priority interrupt may be interrupted by a high priority interrupt. A high priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority occur simultaneously, the high priority level request is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level, there is a second priority structure determined by the polling sequence. This second priority structure is shown in Table 60.

14.4 Interrupt vectors

The vector indicates the Program Memory location where the appropriate interrupt service routine starts; Table 60.

Table 60 Interrupt vectors and priority structure

SOURCE	SYMBOL(1)	VECTOR ADDRESS (HEX)
External 0	X0 (highest)	0003
Serial I/O: SIO1 (I^2C-bus)	S1	002B
ADC completion	ADC	0053
Timer 0 overflow	T0	000B
T2 capture 0	CT0	0033
T2 compare 0	CM0	005B
External 1/ seconds interrupt	X1/SEC	0013
T2 capture 1	CT1	0033
T2 compare 1	CM1	0063
Timer 1 overflow	T1	001B
T2 capture 2	CT2	0043
T2 compare 2	CM2	006B
Serial I/O SIO0 (UART)	S0	0023
T2 capture 3	CT3	004B
T2 overflow	T2 (lowest)	0073

Note

1. X0 has the highest priority; T2 the lowest.

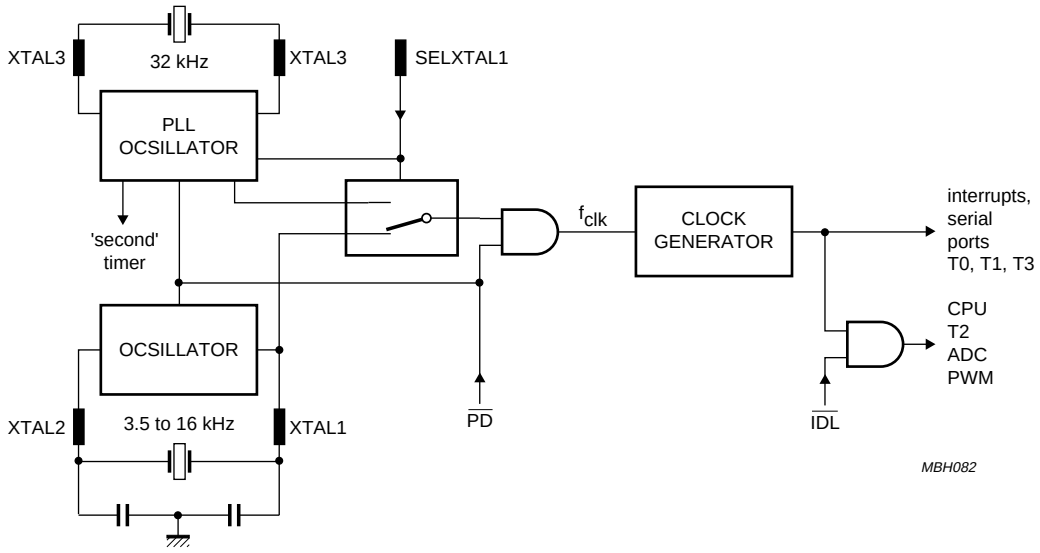


Fig.16 Idle and Power-down hardware for clock generation.

15.5 Power Control Register (PCON)

PCON is not bit addressable and the value after reset is 00H.

Table 70 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	ARD	RFI	WLE	GF1	GF0	PD	IDL

Table 71 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
7	SMOD	**Double Baud rate**. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in Modes 1, 2 and 3.
6	ARD	**AUX-RAM disable.** When set to logic 1 the internal 1792 bytes AUX-RAM is disabled, so that all MOVX-Instructions access the external Data Memory - as it is with the standard 80C51.
5	RFI	**RFI-Reduction Mode.** When set to HIGH the toggling of ALE pin is prohibited. This bit is cleared on reset and can be set and cleared by software. When set, ALE pin will be pulled down internally, switching an external address latch to a quiet state. See also Sections 2.1 and 6.2.
4	WLE	**Watchdog Load Enable**. This flag must be set by software prior to loading T3 (Watchdog Timer). It is cleared when T3 is loaded.
3	GF1	**General purpose flag bits**.
2	GF0	
1	PD	**Power-down mode select**. Setting this bit activates Power-down mode. It can only be set if input $\overline{EW}$ is HIGH.
0	IDL	**Idle mode select**. Setting this bit activates the Idle mode.

16 OSCILLATOR CIRCUITS

16.1 XTAL1; XTAL2 oscillator: standard 80C51

The XTAL1; XTAL2 oscillator: standard 80C51 is selected when input SELXTAL1 = 1. The oscillator circuit is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between pins XTAL1 and XTAL2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance.

XTAL1 is the high gain amplifier input, and XTAL2 is the output; see Fig.17. To drive the P8xC557E8 externally, XTAL1 is driven from an external source and XTAL2 is left open-circuit; see Fig.18.

When the 'XTAL1; XTAL2 oscillator' is selected the 'XTAL3; XTAL4 oscillator' is halted; pins XTAL3 and XTAL4 must not be connected.

16.2 XTAL3; XTAL4 oscillator: 32 kHz PLL oscillator (with Seconds timer)

The XTAL3; XTAL4 oscillator: 32 kHz oscillator and the Phase Locked Loop (PLL) are selected when SELXTAL1 = 0 (XTAL1; XTAL2 oscillator is halted). In this case pin XTAL2 is kept floating.

16.2.1 32 kHz OSCILLATOR

The 32 kHz oscillator consists of an inverter, which forms a Pierce oscillator with the on-chip components C1, C2, R_f and an external crystal of 32768 Hz. The inverter is switched to 3-state and pin XTAL3 is pulled to V_{SS}:

- During Power-down mode, when RUN32 (PLLCON.7) = 0
- During reset, RSTIN = 1
- When the XTAL1; XTAL2 oscillator is selected (SELXTAL1 = 1).

16.2.2 PLL CURRENT CONTROLLED OSCILLATOR

A Current Controlled Oscillator (CCO) generates a clock frequency f_{CCO} of approximately 32, 38, 44 or 50 MHz. This CCO is controlled by the PLL, with the 32 kHz oscillator as the reference clock.

The system clock frequency f_{clk} is derived from f_{CCO} and can be varied under software control by changing the contents of the PLL Control Register (PLLCON) bits FSEL.4 to FSEL.0. The CCO frequency f_{CCO} can be changed via the PLLCON bits FSEL.1 and FSEL.0 and the maximum locking time is 10 ms (this parameter is characterized). During the stabilization phase, no time critical routines should be executed.

Changing f_{clk} has to be done in two steps:

- From **high** to **low** frequencies; first change FSEL.4 to FSEL.2, then FSEL.1 to FSEL.0
- From **low** to **high** frequencies; first change FSEL.1 to FSEL.0 only, and after a stabilization phase of 10 ms, change FSEL.4 to FSEL.2.

If only FSEL.4 to FSEL.2 is changed, and FSEL.1 to FSEL.0 not, then it takes approximately 1 µs until the new frequency is available. The frequency selection is shown in Table 73.

16.2.3 PLL CONTROL REGISTER (PLLCON)

PLLCON is a Special Function Register, which can be read and written by software. It contains the control bits:

- to select the system clock frequencies (f_{clk})
- the seconds interrupt flag (SECINT)
- to enable the seconds interrupt flag (ENSECI)
- the RUN32 bit, which defines if during Power-down mode the 32 kHz oscillator is halted or not.

PLLCON is initialized to 0DH upon reset (RSTIN = 1) or Watchdog Timer overflow. PLLCON = 0DH corresponds to a system clock frequency f_{clk} = 11.01 MHz.

18 SPECIAL FUNCTION REGISTERS OVERVIEW

The P8xC557E8 has 67 SFRs available to the user.

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
FF	T3[1]	XXXX0000	Watchdog Timer
FE	PWMP[1]	00000000	Prescaler Frequency Control Register
FD	PWM1[1]	00000000	Pulse Width Register 1
FC	PWM0[1]	00000000	Pulse Width Register 0
FA	XRAMP[1]	XXXXX000	AUX-RAM Page Register
F9	PLLCON[1]	00001101	PLL Control Register
F8	IP1[1]	00000000	Interrupt Priority Register 1
F7	ADRSH[1]	000000XX	ADC Result Register High Byte
F6	ADRSL7	XXXXXXXX	ADC Result Register Low Byte
F0	B[2]	00000000	B Register
EF	RTE[2]	00000000	Reset/Toggle Enable Register
EE	STE[2]	11000000	Set Enable Register
ED	TMH2[2]	00000000	T2 Register High Byte
EC	TML2[2]	00000000	T2 Register Low Byte
EB	CTCON[2]	00000000	Capture Control Register
EA	TM2CON[2]	00000000	T2 Control Register
E8	IEN1[2]	00000000	Interrupt Enable Register 1
E7	ADPSS	00000000	ADC Input Port Scan-Select Register
E6	ADRSL6	XXXXXXXX	ADC Result Register Low Byte
E0	ACC[2]	00000000	Accumulator
DB	S1ADR	XXXXXXXX	Address Register
DA	S1DAT	XXXXXXXX	Data Shift Register
D9	S1STA	00001100	Serial Status Register
D8	S1CON	00000000	The Serial Control Register
D7	ADCON	XX000000	ADC Control Register
D6	ADRSL5	XXXXXXXX	ADC Result Register Low Byte
D0	PSW[2]	00000000	Program Status Word
CF	CTH3	XXXXXXXX	T2 Capture Register 3 High Byte
CE	CTH2	XXXXXXXX	T2 Capture Register 2 High Byte
CD	CTH1	XXXXXXXX	T2 Capture Register 1 High Byte
CC	CTH0	XXXXXXXX	T2 Capture Register 0 High Byte
CB	CMH2	00000000	T2 Compare Register 2 High Byte
CA	CMH1	00000000	T2 Compare Register 1 High Byte
C9	CMH0	00000000	T2 Compare Register 0 High Byte
C8	TM2IR[2]	00000000	Interrupt Flag Register
C7	P5[1]	11111111	Digital Input Port Register
C6	ADRSL4	XXXXXXXX	ADC Result Register Low Byte
C0	P4[1][2]	11111111	Digital Input Port Register

19.3 Instruction set description

For the description of the **Data Addressing Modes** and **Hexadecimal opcode cross-reference** see Table 80.

Table 76 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A and B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 78 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 80 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

21 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified;
T_{amb} = –40 to +85 °C for the **P8xC557E8EFB**; V_{DDA} = 5 V ±10%; V_{SSA} = 0 V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply (digital part)					
V_{DD}	supply voltage		4.5	5.5	V
I_{DD}	operating supply current	V_{DD} = 5.5 V; notes 1 and 2	–	40	mA
$I_{DD(ID)}$	supply current Idle mode	V_{DD} = 5.5 V; notes 1 and 3	–	12	mA
$I_{DD(PD)}$	supply current Power-down mode	2 V < V_{DD} < V_{DDmax}; note 4	–	100	µA
	supply current Power-down mode; 32 kHz/PLL operation	V_{DD} = 5.5 V; note 17	–	100	µA
Inputs					
V_{IL}	LOW level input voltage (except $\overline{EA}$, SCL, SDA)		–0.5	$0.2V_{DD}$ – 0.15	V
V_{IL1}	LOW level input voltage $\overline{EA}$		–0.5	$0.2V_{DD}$ – 0.35	V
V_{IL2}	LOW level input voltage SCL and SDA; note 5		–0.5	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage (except XTAL1, RSTIN, SCL, SDA, ADEXS)		$0.2V_{DD}$ + 1.0	V_{DD} + 0.5	V
V_{IH1}	HIGH level input voltage XTAL1, RSTIN, ADEXS		$0.7V_{DD}$ + 0.1	V_{DD} + 0.5	V
V_{IH2}	HIGH level input voltage SCL and SDA; note 5		$0.7V_{DD}$	6.0	V
I_{IL}	LOW level input current Ports 1, 2, 3 and 4	V_{IN} = 0.45 V	–	–75	µA
I_{TL}	input current HIGH-to-LOW transition Ports 1, 2, 3 and 4	note 6	–	–750	µA
I_{LI1}	input leakage current Port 0, $\overline{EA}$, ADEXS, $\overline{EW}$, SELXTAL1	0.45 V < V_I < V_{DD}	–	±10	µA
I_{LI2}	input leakage current SCL and SDA	0 V < V_I < 6 V 0 V < V_{DD} < 5.5 V	–	±10	µA
I_{LI3}	input leakage current Port 5	0.45 V < V_I < V_{DD}	–	±1	µA
Outputs					
V_{OL}	LOW level output voltage Ports 1, 2, 3 and 4	I_{OL} = 1.6 mA; note 7	–	0.45	V
V_{OL1}	LOW level output voltage Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$, RSTOUT	I_{OL} = 3.2 mA; note 7	–	0.45	V
V_{OH}	HIGH level output voltage Ports 1, 2, 3 and 4	I_{OH} = –60 µA I_{OH} = –25 µA I_{OH} = –10 µA	2.4 $0.75V_{DD}$ $0.9V_{DD}$	– – –	V V V
V_{OH1}	HIGH level output voltage Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$, RSTOUT; note 8	I_{OH} = –800 µA I_{OH} = –300 µA I_{OH} = –80 µA	2.4 $0.75V_{DD}$ $0.9V_{DD}$	– – –	V V V

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{HYS}	hysteresis of Schmitt Trigger inputs SCL and SDA (Fast Mode)		$0.05V_{DD}$[20]	–	V
R_{RST}	RST pull-down resistor		50	150	kΩ
$C_{I/O}$	I/O pin capacitance	test frequency = 1 MHz; T_{amb} = 25 °C	–	10	pF
Supply (analog part)					
V_{DDA}	supply voltage	$V_{DDA} = V_{DD} \pm 0.2$ V	4.5	5.5	V
I_{DDA}	supply current operating	Port 5 = 0 V to V_{DDA}; notes 1 and 2	–	1.2	mA
	supply current operating 32 kHz / PLL operation	Port 5 = 0 V to V_{DDA}; notes 17 and 18	–	7.2	mA
$I_{DDA(ID)}$	supply current Idle mode	notes 1 and 3	–	70	µA
	supply current Idle mode 32 kHz / PLL operation	notes 17 and 18	–	6.0	mA
$I_{DDA(PD)}$	supply current Power-down mode	2 V < V_{DD} <$V_{DD(max)}$; note 4	–	50	µA
	supply current Power-down mode 32 kHz/PLL operation	V_{DD} = 5.5 V; note 17	–	200	µA
Analog inputs					
$V_{in(A)}$	analog input voltage		V_{SSA} – 0.2	V_{DDA} + 0.2	V
$V_{ref(n)(A)}$	reference voltage		V_{SSA} – 0.2	–	V
$V_{ref(p)(A)}$			–	V_{DDA} + 0.2	V
R_{REF}	resistance between $V_{ref(p)(A)}$ and $V_{ref(n)(A)}$		10	50	kΩ
C_{IA}	analog input capacitance		–	15	pF
DL_e	differential non-linearity	notes 9, 10 and 11	–	±1	LSB
IL_e	integral non-linearity	notes 9 and 12	–	±2	LSB
OS_e	offset error	notes 9 and 13	–	±2	LSB
G_e	gain error	notes 9 and 14	–	±0.4	%
A_e	absolute voltage error	notes 9 and 15	–	±3	LSB
M_{ctc}	channel-to-channel matching		–	±1	LSB
C_t	crosstalk between P5 inputs	0 to 100 kHz; note 16	–	–60	dB

Notes to the DC characteristics

1. See Figs 22, 25 and 24 for I_{DD} test conditions.
2. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 5ns$; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2, XTAL3 not connected; Port 0 = $\overline{EW}$ = SCL = SDA = SELXTAL1 = V_{DD}; $\overline{EA}$ = RSTIN = ADEXS = XTAL4 = V_{SS}.
3. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 5$ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2, XTAL3 not connected; $\overline{EA}$ = RSTIN = Port 0 = $\overline{EW}$ = SCL = SDA = SELXTAL1 = V_{DD}; ADEXS = XTAL4 = V_{SS}.
4. The Power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = $\overline{EW}$ = SCL = SDA = SELXTAL1 = V_{DD}; $\overline{EA}$ = RSTIN = ADEXS = XTAL1 = XTAL4 = V_{SS}.
5. The input threshold voltage of SCL and SDA (SIO1) meets the I^2C specification, so an input voltage below 0.3 V_{DD} will be recognized as a logic 0 while an input voltage above 0.7 V_{DD} will be recognized as a logic 1.
6. Pins of Ports 1, 2, 3 and 4 source a transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
7. Capacitive loading on Ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and Ports 1, 3 and 4. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
8. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address bits are stabilizing.
9. $V_{ref(n)(A)} = 0$ V; $V_{DDA} = 5.0$ V, $V_{ref(p)(A)} = 5.12$ V. $V_{DD} = 5.0$ V, $V_{SS} = 0$ V, ADC is monotonic with no missing codes. Measurement by continuous conversion of $V_{in(A)} = -20$ mV to 5.12 V in steps of 0.5 mV, deriving parameters from collected conversion results of ADC. ADC prescaler programmed according to the actual oscillator frequency, resulting in a conversion time within the specified range for t_{ADC} (15 to 50 µs).
10. The differential non-linearity (D_{Le}) is the difference between the actual step width and the ideal step width.
11. The ADC is monotonic; there are no missing codes.
12. The integral non-linearity (I_{Le}) is the peak difference between the centre of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error.
13. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. The offset error is constant at every point of the actual transfer curve.
14. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve.
15. The absolute voltage error (A_e) is the maximum difference between the centre of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
16. This should be considered when both analog and digital signals are simultaneously input to Port 5.
17. The supply current with 32 kHz oscillator running and PLL operation (SELXTAL1 = 0) is measured with all output pins disconnected; XTAL4 driven with $t_r = t_f = 5$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; Port 0 = $\overline{EW}$ = SCL = SDA = V_{DD}; $\overline{EA}$ = RSTIN = ADEXS = SELXTAL 1 = XTAL1 = V_{SS}.
18. Not 100% tested; sum of $I_{DDA(ID)}$ (PLL) and I_{DDA} (HF-Oscillator).
19. The parameter meets the I^2C-bus specification for standard-mode and fast-mode devices.
20. Not 100% tested.

Table 82 I^2C-bus interface timing

All values referred to $V_{IH(min)}$ and $V_{IL(max)}$ levels; see Fig.31.

SYMBOL	PARAMETER	I^2C-BUS				UNIT
		STANDARD MODE		FAST MODE		
		MIN.	MAX.	MIN.	MAX.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	bus free time between STOP and START condition	4.7	–	1.3	–	µs
$t_{HD;STA}$	hold time (repeated) START condition; after this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$	data hold time: for CBUS compatible masters (see Chapter 21; notes 1 and 3)	5.0	–	–	–	µs
	for I^2C-bus devices (notes 1 and 2)	0		0	0.9	µs
$t_{SU;DAT}$	data set-up time	250	–	100(3)	–	ns
t_{RD}; t_{RC}	rise time of SDA and SCL signals	–	1000	20 + 0.1C_b(4)	300	ns
t_{FD}; t_{FC}	fall time of SDA and SCL signals	–	300			
$t_{SU;STO}$	set-up time for STOP condition	4.0	–	0.6	–	µs
C_b	capacitive load for each bus line	–	400	–	400	pF
t_{SP}	pulse width of spikes which must be suppressed by the input filter	–	–	0	50	ns

Notes

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU,\ DAT} > 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R(max)} + t_{SU,DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I^2C-bus specification) before the SCL line is released.
4. C_b = total capacitance of one bus line in pF.

Table 83 External clock drive XTAL1

SYMBOL	PARAMETER	VARIABLE CLOCK (f_{clk} = 3.5 to 16 MHz)		UNIT
		MIN.	MAX.	
t_{clk}	oscillator clock period	63	286	ns
t_{HIGH}	HIGH time	20	$t_{clk} - t_{LOW}$	ns
t_{LOW}	LOW time	20	$t_{clk} - t_{HIGH}$	ns
t_r	rise time	–	20	ns
t_f	fall time	–	20	ns
t_{CYC}	cycle time ($12 \times t_{clk}$)	0.75	3.4	µs

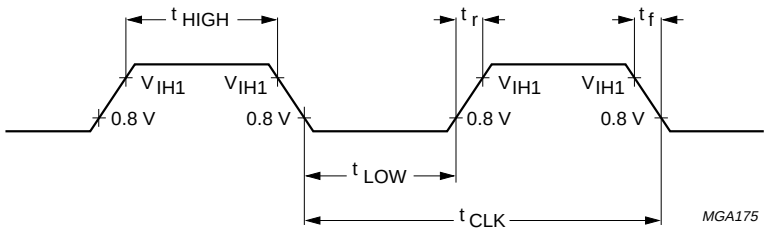
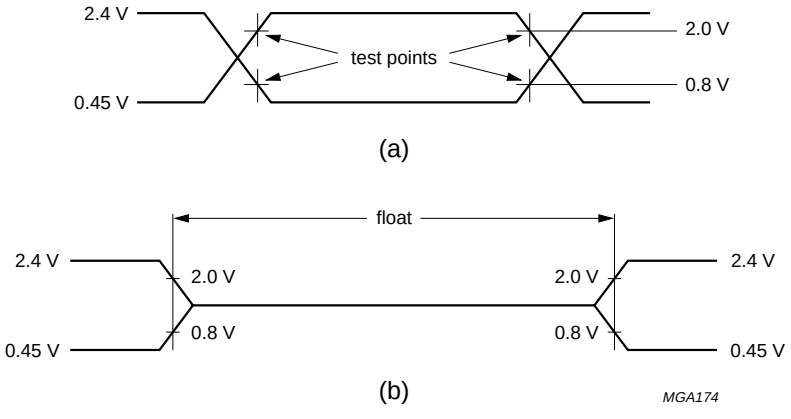


Fig.24 External clock drive XTAL1.



AC testing inputs are driven at 2.4 V for a HIGH and 0.45 V for a LOW.
Timing measurements are taken at 2.0 V for a HIGH and 0.8 V for a LOW, see Fig.25 (a).
The float state is defined as the point at which a Port 0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels, see Fig.25 (b).

Fig.25 AC testing input, output waveform (a) and float waveform (b).

Table 86 EPROM programming modes

MODE	RSTIN	$\overline{\text{PSEN}}$	ALE/$\overline{\text{PROG}}$	$\overline{\text{EA}}$/V_{PP}	P2.7	P2.6	P3.7	P3.6	P3.3
Read Signature	HIGH	LOW	HIGH	HIGH	LOW	LOW	LOW	LOW	LOW
Program code data	HIGH	LOW	LOW (1)	V_{PP}(2)	HIGH	LOW	HIGH	HIGH	HIGH
Verify code data	HIGH	LOW	HIGH	HIGH	LOW	LOW	HIGH	HIGH	LOW
Program Encryption table	HIGH	LOW	LOW(1)	V_{PP}(2)	HIGH	LOW	HIGH	LOW	HIGH
Program Lock bit 1	HIGH	LOW	LOW(1)	V_{PP}(2)	HIGH	HIGH	HIGH	HIGH	HIGH
Program Lock bit 2	HIGH	LOW	LOW(1)	V_{PP}(2)	HIGH	HIGH	LOW	LOW	HIGH
Program Lock bit 3	HIGH	LOW	LOW(1)	V_{PP}(2)	LOW	HIGH	LOW	HIGH	HIGH

Notes

1. Each programming pulse is:
   a) LOW for 50 ± 5 µs.
   b) HIGH for at least 5 µs.
2. ALE/$\overline{\text{PROG}}$ receives 5 programming pulses while V_{PP} is held at 12.75 ± 0.25 V.

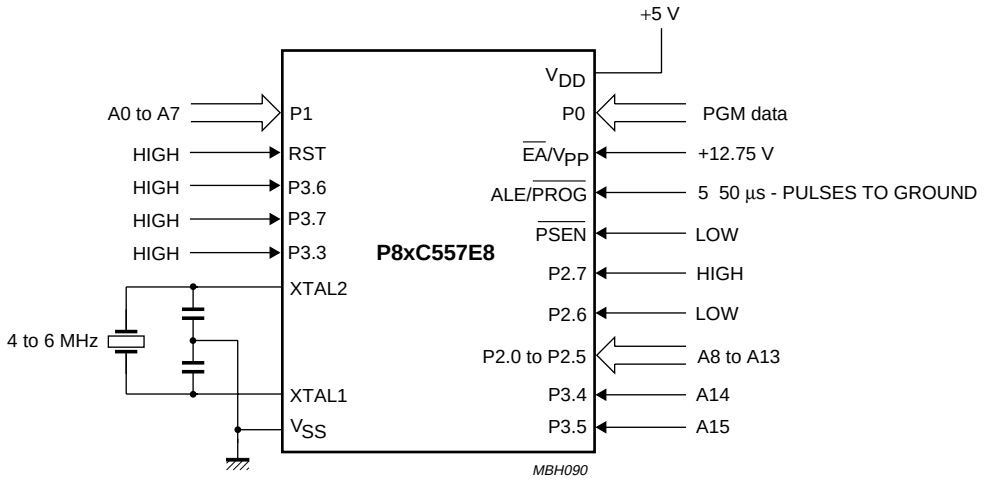
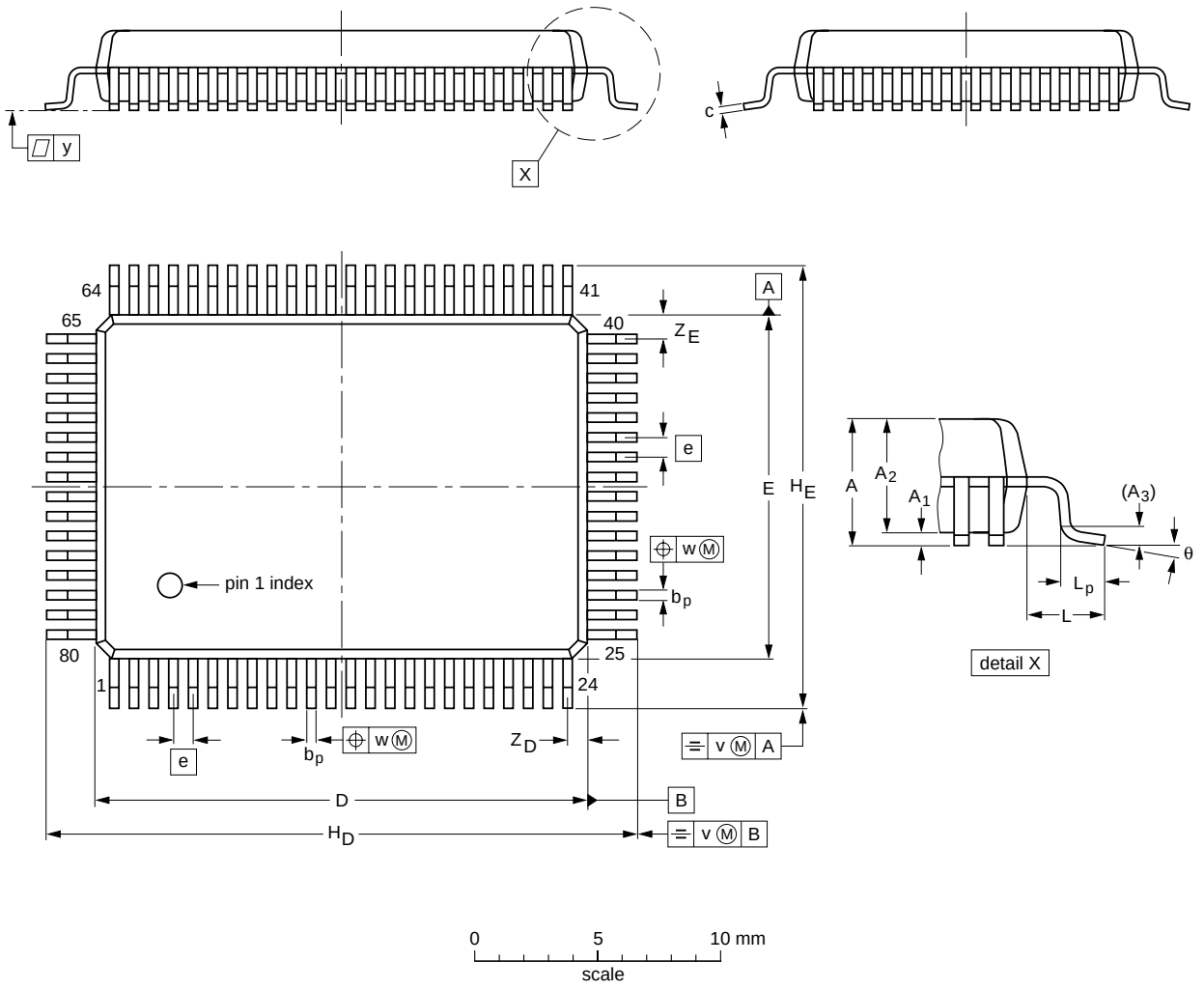


Fig.32 Programming configuration.

24 PACKAGE OUTLINE

QFP80: plastic quad flat package;
80 leads (lead length 1.95 mm); body 14 x 20 x 2.7 mm; high stand-off height **SOT318-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.3	0.36 0.10	2.87 2.57	0.25	0.45 0.30	0.25 0.13	20.1 19.9	14.1 13.9	0.8	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.0 0.6	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT318-1						~~95-02-04~~ 97-08-01