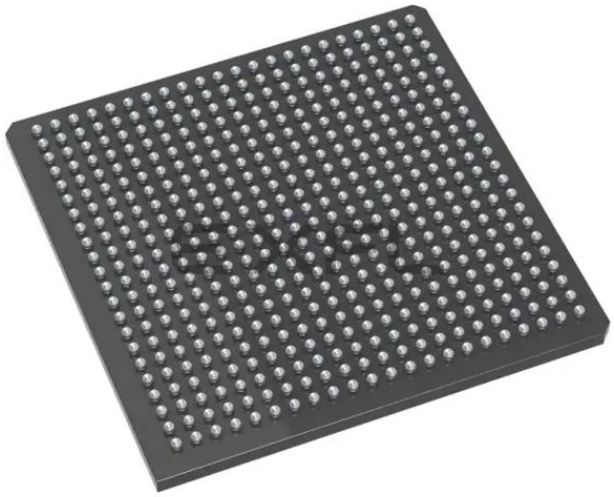

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	56520
Total RAM Bits	1869824
Number of I/O	267
Number of Gates	-
Voltage - Supply	1.14V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-55°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2gl060t-1fg484m

- Two AHB/APB Interfaces to FPGA Fabric (Master/Slave Capable)
- Two DMA Controllers to Offload Data Transactions
  - 8-Channel Peripheral DMA (PDMA) for Data Transfer Between HPMS Peripherals and Memory
- High-Performance DMA (HPDMA) for Data Transfer Between eSRAM and DDR Memories

Clocking Resources

- Clock Sources
  - High Precision 32 kHz to 20 MHz Main Crystal Oscillator
  - 1 MHz Embedded RC Oscillator
  - 50 MHz Embedded RC Oscillator
- Up to 8 Clock Conditioning Circuits (CCCs) with Up to 8 Integrated Analog PLLs
  - Output Clock with 8 Output Phases and 45° Phase Difference (Multiply/Divide, and Delay Capabilities)
- Frequency: Input 1 MHz to 200 MHz, Output 20 MHz to 400 MHz

Operating Voltage and I/Os

- 1.2 V Core Voltage
- Multi-Standard User I/Os (MSIO/MSIOD)
  - LVTTL/LVCMOS 3.3 V (MSIO only)
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
  - DDR (SSTL2_1, SSTL2_2)
  - LVDS, MLVDS, Mini-LVDS, RSDS Differential Standards
  - PCI
  - LVPECL (receiver only)
- DDR I/Os (DDRIO)
  - DDR, DDR2, DDR3, LPDDR, SSTL2, SSTL18, HSTL
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
- Market Leading Number of User I/Os with 5G SERDES

Security

- Design Security Features (available on all devices)
  - Intellectual Property (IP) Protection through Unique Security Features and Use Models New to the PLD Industry
  - Encrypted User Key and Bitstream Loading, Enabling Programming in Less-Trusted Locations
  - Supply-Chain Assurance Device Certificate
  - Enhanced Anti-Tamper Features
  - Zeroization
- Data Security Features (available on premium devices)
  - Non-Deterministic Random Bit Generator (NRBG)
  - User Cryptographic Services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) Engine)
  - User Physically Unclonable Function (PUF) Key Enrollment and Regeneration
  - CRI Pass-Through DPA Patent Portfolio License
  - Hardware Firewalls Protecting Microcontroller Subsystem (HPMS) Memories

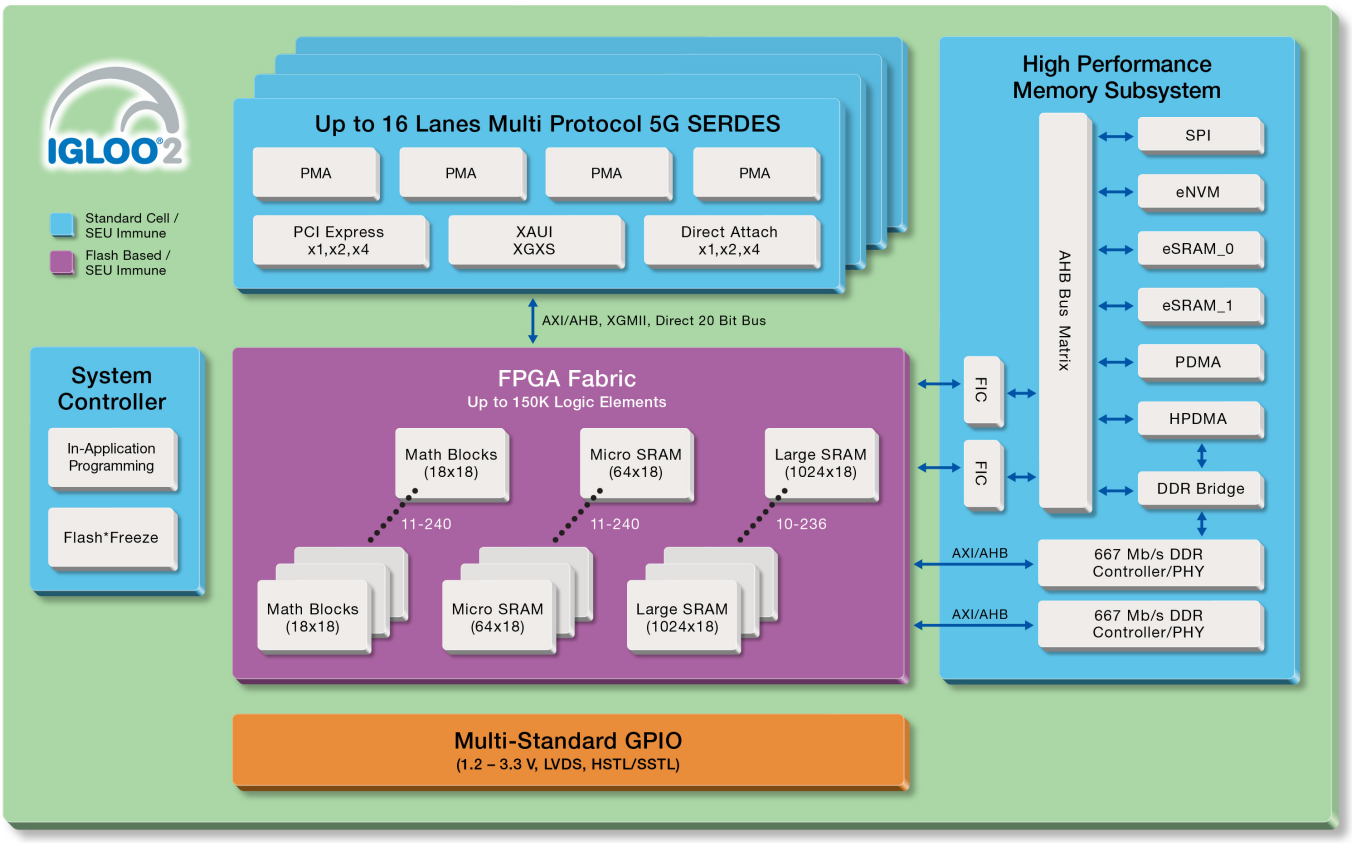
Reliability

- Single Event Upset (SEU) Immune
  - Zero FIT FPGA Configuration Cells
- Junction Temperature: 125°C – Military Temperature, 100°C – Industrial Temperature, 85°C – Commercial Temperature
- Single Error Correct Double Error Detect (SECDED) Protection on the Following:
  - Embedded Memory (eSRAMs)
  - PCIe Buffer
  - DDR Memory Controllers with Optional SECDED Modes
- Buffers Implemented with SEU Resistant Latches on the Following:
  - DDR Bridges (HPMS, MDDR, FDDR)
  - SPI FIFO
- NVM Integrity Check at Power-Up and On-Demand
- No External Configuration Memory Required—Instant-On, Retains Configuration When Powered Off

Low Power

- Low Static and Dynamic Power
  - Flash*Freeze Mode for Fabric
- Power as low as 13 mW/Gbps per lane for SERDES devices
- Up to 25% lower total power than competing devices

IGLOO2 FPGA Block Diagram



Acronyms

AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
COMM_BLK	Communication Block
DDR	Double Data Rate
DPA	Differential Power Analysis
ECC	Elliptical Curve Cryptography
EDAC	Error Detection And Correction
FDDR	DDR2/3 Controller in FPGA Fabric
FIC	Fabric Interface Controller
HPMS	High-Performance Memory Subsystem
IAP	In-Application Programming
MACC	Multiply-Accumulate
MDDR	DDR2/3 Controller in HPMS
SECDED	Single Error Correct Double Error Detect
SEU	Single Event Upset
SHA	Secure Hashing Algorithm
XAUI	10 Gbps Attachment Unit Interface
XGMII	10 Gigabit Media Independent Interface
XGXS	XGMII Extended Sublayer

Table 1 • IGLOO2 FPGA Product Family

	Features [2, 3]	M2GL005 (S)	M2GL010 (S/T/TS)	M2GL025 (T/TS)	M2GL050 (T/TS)	M2GL060 (T/TS)	M2GL090 (T/TS)	M2GL150 (T/TS)
Logic/DSP	Maximum Logic Elements (4LUT + DFF)[1]	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Math Blocks (18x18)	11	22	34	72	72	84	240
	PLLs and CCCs	2		6				8
	SPI/HPDMA/PDMA	1 each						
	Fabric Interface Controllers (FICs)	1			2	1		2
	Data Security	AES256, SHA256, RNG				AES256, SHA256, RNG, ECC, PUF		
Memory	eNVM (K Bytes)	128	256				512	
	LSRAM 18K Blocks	10	21	31	69	69	109	236
	uSRAM1K Blocks	11	22	34	72	72	112	240
	eSRAM (K Bytes)	64						
	Total RAM (K bits)	703	912	1104	1826	1826	2586	5000
High Speed	DDR Controllers	1x18			2x36	1x18	1x18	2x36
	SERDES Lanes (T)	0	4		8	4	4	16
	PCIe End Points	0	1		2			4
User I/Os	MSIO (3.3 V)	119	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40	40	62	40	40	106
	DDRIO (2.5 V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M), Automotive (T1/T2)	C, I, T1, T2	C, I, M, T1, T2					C, I, M

Notes:

1. *Total logic may vary based on utilization of DSP and memories in your design. See the UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide for details.*
2. *Feature availability is package dependent.*
3. *Data security features are only available in "S" and "TS" devices.*

I/Os Per Package

Table 2 • I/Os per Package and Package Options

	Package Options[4]																			
Type	**FCS(G)325** [5]		**VF(G)256** [5, 9]		**FCS(G)536** [5]		**VF(G)400** [5, 9]		**FCV(G)484** [5, 9]		**TQ(G)144** [5, 11]		**FG(G)484** [5, 10]		**FG(G)676** [5, 9]		**FG(G)896** [5]		**FC(G)1152** [5]	
Pitch (mm)	0.5		0.8		0.5		0.8		0.8		0.5		1.0		1.0		1.0		1.0	
Length x Width (mm)	11x11		14x14		16x16		17x17		19x19		20x20		23x23		27x27		31x31		35x35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2GL005 (S)			161	-			171	-			84	-	209	-						
M2GL010 (T/TS) [1, 6]			138	2			195	4			84	-	233	4						
M2GL025 (T/TS) [1]	180	2	138	2			207	4					267	4						
M2GL050 (T/TS) [1]	200	2					207	4					267	4			377	8		
M2GL060 (T/TS) [1]	200	2					207	4					267	4	387	4				
M2GL090 (T/TS) [1, 2, 7]	180	4											267	4	425	4				
M2GL150 (T/TS) [2]					293	4			248	4									574	16

Notes:

1. *Mil Temp 010/025/050/060/090 devices are only available in the FG(G)484 package.*
2. *Mil Temp 150 devices are only available in the FC(G)1152 package.*
3. *090 FCS(G)325 is 11x13.5 pkg dimension.*
4. *All the packages mentioned above are available with lead and lead free.*
5. *(G) indicates that the package is RoHS 6/6 Compliant/Pb-free*
6. *M2GL010 (S) device is only available in TQ(G)144 package. M2GL010 (T/TS) devices are not available in TQ(G)144 package.*
7. *The M2GL090 (T/TS) device in the FCSG325 package is available with an ordering code of XZ48. The XZ48 ordering code pre-configures the device for Auto Update mode. Minimum Order quantities apply, contact your local Microsemi sales office for details.*
8. *Shaded cells indicate that the device packages have vertical migration capability.*
9. *Automotive T2 grade devices are available in the VF(G)256, VF(G)400, FG(G)484, and FG(G)676 packages.*
10. *Automotive T1 grade devices are available in the FG(G)484 package.*
11. *The TQ(G)144 package will be available in T2 grade by the end of February, 2017.*

Table 3 • Features per Device/Package Combination

Package	Devices	MDDR	FDDR	Crystal Oscillators	5G[5] SERDES Lanes	PCIe Endpoints	MSIO (3.3V max) [6]	MSIOD (2.5V max) [7]	DDRIO (2.5V max)	Total User I/O
TQ(G)144 [8]	M2GL005 (S)	-	-	1	-	-	52	9	23	84
	M2GL010 (S)	-	-	1	-	-	50	11	23	84
VF(G)256 [8]	M2GL005 (S)	-	-	1	-	-	119	12	30	161
	M2GL010 (T/TS)	x18[1]	-	1	2	1	66	8	64	138
	M2GL025 (T/TS)	x18[1]	-	1	2	1	66	8	64	138
FCS(G)325 [8]	M2GL025 (T/TS)	x18[1]	-	1	2	1	94	22	64	180
	M2GL050 (T/TS)	x18[2]	-	1	2	1	90	22	88	200
	M2GL060 (T/TS)	x18[1]	-	1	4	2	114	22	64	200
	M2GL090 (T/TS)	x18[1]	-	1	4	2	104	12	64	180

Table 3 • Features per Device/Package Combination (continued)

VF(G)400 [8]	M2GL005 (S)	x18[1]	-	1	-	-	79	28	64	171
	M2GL010 (T/TS)	x18[1]	-	1	4	1	99	32	64	195
	M2GL025 (T/TS)	x18[1]	-	1	4	1	111	32	64	207
	M2GL050 (T/TS)	x18[2]	-	1	4	1	87	32	88	207
	M2GL060 (T/TS)	x18[1]	-	1	4	2	111	32	64	207
FCV(G)484 [8]	M2GL150 (T/TS)	x18[1]	x18[1]	1	4	4[9]	91	34	123	248
FG(G)484 [8]	M2GL005 (S)	x18[1]	-	1	-	-	115	28	66	209
	M2GL010 (T/TS)	x18[1]	-	1	4	1	123	40	70	233
	M2GL025 (T/TS)	x18[1]	-	1	4	1	157	40	70	267
	M2GL050 (T/TS)	x18[2]	-	1	4	1	105	40	122	267
	M2GL060 (T/TS)	x18[1]	-	1	4	2	157	40	70	267
	M2GL090 (T/TS)	x18[1]	-	1	4	2	157	40	70	267
FC(G)536 [8]	M2GL150 (T/TS)	x18[1]	x18[1]	1	4	4[9]	151	16	126	293
FG(G)676 [8]	M2GL060 (T/TS)	x18[1]	-	1	4	2	271	40	76	387
	M2GL090 (T/TS)	x18[1]	-	1	4	2	309	40	76	425
FG(G)896 [8, 10]	M2GL050 (T/TS)	x36[4]	x36[4]	1	8	2	139	62	176	377
FC(G)1152 [8]	M2GL150 (T/TS)	x36[3]	x36[3]	1	16	4	292	106	176	574

1. *DDR supports x18, x16, x9, and x8 modes*
2. *DDR supports x18 and x16 modes*
3. *DDR supports x36, x32, x18, x16, x9, and x8 modes*
4. *DDR supports x36, x32, x18, and x16 modes*
5. *Maximum SERDES rate for Mil temp devices is 3.125Gbps*
6. *Number of differential MSIO is Number of MSIOs/2 for even and (Number of MSIOs - 1)/2 for odd*
7. *Number of differential MSIOD is Number of MSIODs/2 for even and (Number of MSIODs - 1)/2 for odd*
8. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*
9. *4 PCIe Gen1/Gen2 endpoints x1 lane configuration.*
10. *DDR3 is non-compliant. Call technical support for details.*
11. *SERDES is not available in Automotive T1 grade.*

Table 4 • Available Programming Interfaces

Package	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
TQ(G)144 [1]	M2GL005 (S)	Yes	Yes	No	No
	M2GL010 (S)	Yes	Yes	No	No
VF(G)256 [1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	No
	M2GL025 (T/TS)	Yes	Yes	Yes	No
FCS(G)325 [1]	M2GL025 (T/TS)	Yes	Yes	No	No
	M2GL050 (T/TS)	Yes	Yes	No	No
	M2GL060 (T/TS)	Yes	Yes	No	No
	M2GL090 (T/TS)	Yes	Yes	No	No
VF(G)400 [1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	Yes
	M2GL025 (T/TS)	Yes	Yes	Yes	Yes
	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
FCV(G)484 [1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)484 [1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	Yes
	M2GL025 (T/TS)	Yes	Yes	Yes	Yes
	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
	M2GL090 (T/TS)	Yes	Yes	Yes	Yes
FCS(G)536 [1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)676 [1]	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
	M2GL090 (T/TS)	Yes	Yes	Yes	Yes
FG(G)896 [1]	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
FC(G)1152 [1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes

Notes:

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

IGLOO2 Commercial and Industrial Temperature Grade Devices

Table 6 • IGLOO2 Devices without Data Security (All Speed Grades, C and I Temperature)[1]

Density	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
M2GL005										
M2GL010		T		T			T			
M2GL025	T	T		T			T			
M2GL050	T			T			T		T	
M2GL060	T			T			T	T		
M2GL090	T						T	T		
M2GL150			T		T					T

Notes:

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*
2. *T indicates that the devices are available with Transceiver. Example ordering code: M2GL025T-FCSG325*
3. *Shaded cells indicate that the devices are available without Transceiver. Example ordering code: M2GL025-FCSG325*

Table 7 • IGLOO2 Data Security "S" Devices (All Speed Grades, C and I Temperature)[1]

Density	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
M2GL005		S		S		S	S			
M2GL010		TS		TS		S	TS			
M2GL025	TS	TS		TS			TS			
M2GL050	TS			TS			TS		TS	
M2GL060	TS			TS			TS	TS		
M2GL090	TS						TS	TS		
M2GL150			TS		TS					TS

Notes:

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*
2. *S indicates that the devices are available with Data Security. Example ordering code: M2GL005S-VFG400*
3. *TS indicates that the devices are available with Transceiver and Data Security. Example ordering code: M2GL025TS-FCSG325*

IGLOO2 Military Temperature Grade Devices

Table 8 • IGLOO2 Military Temperature Device Offering

M2GL010 (T/TS)-1FG(G)484M
M2GL025 (T/TS)-1FG(G)484M
M2GL050 (T/TS)-1FG(G)484M
M2GL060 (T/TS)-1FG(G)484M
M2GL090 (T/TS)-1FG(G)484M
M2GL150 (T/TS)-1FC(G)1152M

Notes:
1. *Gold Wire bonds are available for the FG484 package by appending X399 to the part number when ordering, for example: M2GL090 (T/TS)-1FG484MX399.*
2. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

IGLOO2 Device Status

Refer to the *DS0128: IGLOO2 and SmartFusion2 Datasheet* for device status.

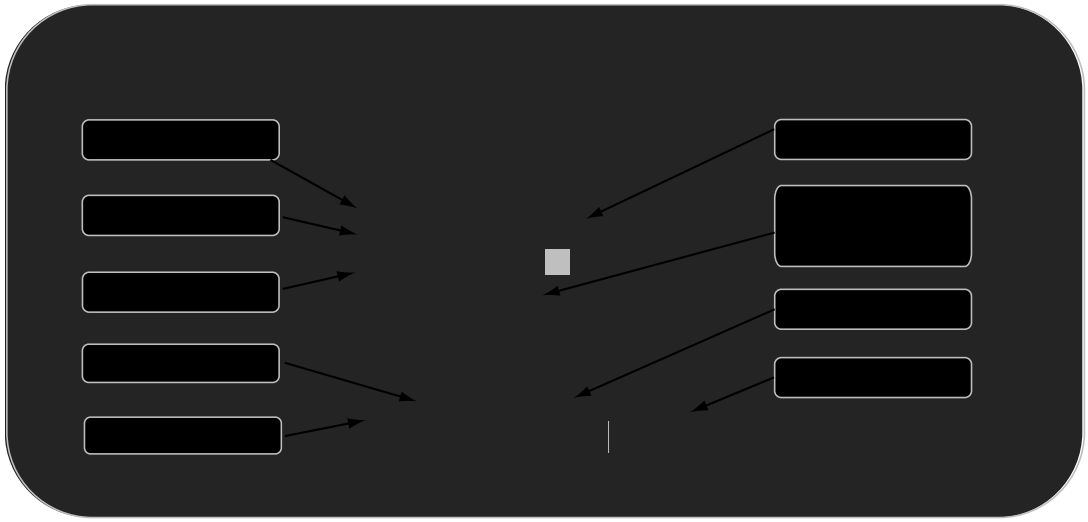
IGLOO2 Datasheet and Pin Descriptions

The datasheet and pin descriptions are published separately:

- *DS0128: IGLOO2 and SmartFusion2 Datasheet*
- *DS0124: IGLOO2 Pin Descriptions Datasheet*
- *DS0138: IGLOO2 Automotive Grade 1 Datasheet*
- *DS0134: SmartFusion2 and IGLOO2 Automotive Grade 2 Datasheet*
- *PB0135: Automotive Grade 2 IGLOO2 FPGAs Product Brief*

Marking Specification Details

Microsemi normally topside marks the full ordering part number on each device. The figure below provides the details for each character code present on Microsemi's IGLOO2 FPGA devices.



- Country of Origin (CCD): Assembly house country location

  Country name: Country Code

  China: CHN

  Hong Kong: HKG

  Japan: JPN

  Korea, South: KOR

  Philippines: PHL

  Taiwan: TWN

  Singapore: SGP

  United States: USA

  Malaysia: MYS

1 – IGLOO2 Device Family Overview

Microsemi's IGLOO2 FPGAs integrate fourth generation flash-based FPGA fabric and high-performance communications interfaces on a single chip. The IGLOO2 family is the industry's lowest power, highest reliability and most secure programmable logic solution. This next generation IGLOO2 architecture offers up to 3.6X gate count, implemented with 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and mathblocks for DSP. High speed serial interfaces enable PCIe, XAUI / XGXS plus native SERDES communication while DDR2/DDR3 memory controllers provide high speed memory interfaces.

Reliability

IGLOO2 flash-based fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. The flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, IGLOO2 devices add reliability to many other aspects of the device. Single Error Correct Double Error Detect (SECDED) protection is implemented on the embedded SRAM (eSRAM), and is optional on the DDR memory controllers. This means that if a one-bit error is detected, it will be corrected. Errors of more than one bit are detected only and not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are more resistant to SEUs. Therefore, no correction is needed in these locations: DDR bridges (HPMS, MDDR, FDDR), SPI, and PCIe FIFOs.

Highest Security Devices

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the IGLOO2 family incorporates essentially all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO®, and ProASIC®3 third-generation flash FPGAs and cSoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion2 and IGLOO2 FPGAs add many unique design and data security features and use models new to the PLD industry.

Design Security vs. Data Security

When classifying security attributes of programmable logic devices (PLDs), a useful distinction is made between design security and data security.

Design Security

Design security is protecting the intent of the owner of the design, such as keeping the design and associated bitstream keys confidential, preventing design changes (for example, insertion of Trojan Horses), and controlling the number of copies made throughout the device life cycle. Design security may also be known as intellectual property (IP) protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following are the main design security features supported.

Table 1-1 • **Design Security Features**

Features	**All Devices**	
	M2GL005	**M2GL060**
	M2GL010	**M2GL090**
	M2GL025	**M2GL150**
	M2GL050	
FlashLock™ Passcode Security (256-bit)	x	x
Flexible security settings using flash lock-bits	x	x
Encrypted/Authenticated Design Key Loading	x	x
Symmetric Key Design Security (256-bit)	x	x
Design Key Verification Protocol	x	x
Encrypted/Authenticated Configuration Loading	x	x
Certificate-of-Conformance (C-of-C)	x	x
Back-Tracking Prevention (also know as, Versioning)	x	x
Device Certificate(s) (Anti-Counterfeiting)	x	x
Support for Configuration Variations	x	x
Fabric NVM and eNVM Integrity Tests	x	x
Information Services (S/N, Cert., USERCODE, and others)	x	x
Tamper Detection	x	x
Tamper Response (includes Zeroization)	x	x
ECC Public Key Design Security (384-bit)		x
Hardware Intrinsic Design Key (SRAM-PUF)		x

Data Security

Data Security is protecting the information the FPGA is storing, processing, or communicating in its role in the end application. If, for example, the configured design is implementing the key management and encryption portion of a secure military radio, data security could entail encrypting and authenticating the radio traffic, and protecting the associated application-level cryptographic keys. Data security is closely related to the terms information assurance (IA) and information security. All IGLOO2 devices incorporate enhanced design security, making them the most secure programmable logic devices ever made. Select IGLOO2 models also include an advanced set of on-chip data security features that make designing secure information assurance applications easier and better than ever before.

Table 1-2 • **Data Security Features**

Features	**S Devices**	
	M2GL005S	**M2GL060TS**
	M2GL010S **M2GL010TS**	**M2GL090TS**
	M2GL025TS	**M2GL150TS**
	M2GL050TS	
CRI Pass-through DPA Patent License	x	x
Hardware Firewalls protecting access to memories	x	x
Non-Deterministic Random Bit Generator Service	x	x
AES-128/256 Service (ECB, OFB, CTR, CBC modes)	x	x
SHA-256 Service	x	x
HMAC-SHA-256 Service	x	x
Key Tree Service	x	x
PUF Emulation (Pseudo-PUF)	x	
PUF Emulation (SRAM-PUF)		x
ECC Point-Multiplication Service		x
ECC Point-Addition Service		x
User SRAM-PUF Enrollment Service		x
User SRAM-PUF Activation Code Export Service		x
SRAM-PUF Intrinsic Key Gen. & Enrollment Service		x
SRAM-PUF Key Import & Enrollment Service		x
SRAM-PUF Key Regeneration Service		x

Low Power

Microsemi's flash-based FPGA fabric results in extremely low power design implementation with static power as low as 7.5 mW (for 6,060 LE device). Flash*Freeze (F*F) technology provides an ultra-low power static mode (Flash*Freeze mode) for IGLOO2 devices, with power less than 11 mW for the largest device (146,124 LEs). F*F mode entry retains all the SRAM and register information and the exit from F*F mode achieves rapid recovery to active mode.

DDR Bridge

The DDR bridge is a data bridge between two AHB bus masters and a single AXI bus slave. The DDR bridge accumulates AHB writes into write combining buffers prior to bursting out to external DDR memory. The DDR bridge also includes read combining buffers, allowing AHB masters to efficiently read data from the external DDR memory from a local buffer. The DDR bridge optimizes reads and writes from multiple masters to a single external DDR memory. Data coherency rules between the masters and the external DDR memory are implemented in hardware. The DDR bridge contains two write combining / read buffers. All buffers within the DDR bridge are implemented with SEU tolerant latches and are not subject to the single event upsets (SEUs) that SRAM exhibits. IGLOO2 devices implement three DDR bridges in the HPMS, FDDR, and MDDR subsystems.

AHB Bus Matrix (ABM)

The AHB bus matrix (ABM) is a non-blocking, AHB-Lite multi-layer switch, supporting 4 master interfaces and 8 slave interfaces. The switch decodes access attempts by masters to various slaves, according to the memory map and security configurations. When multiple masters are attempting to access a particular slave simultaneously, an arbiter associated with that slave decides which master gains access, according to a configurable set of arbitration rules. These rules can be configured by the user to provide different usage patterns to each slave. For example, a number of consecutive access opportunities to the slave can be allocated to one particular master, to increase the likelihood of same type accesses (all reads or all writes), which makes more efficient usage of the bandwidth to the slave.

Fabric Interface Controller (FIC)

The FIC block provides two separate interfaces between the HPMS and the FPGA fabric: the HPMS master (MM) and fabric master (FM). Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks present in the HPMS (FIC_0 and FIC_1).

Embedded SRAM (eSRAM)

The HPMS contains two blocks of 32 KB eSRAM, giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the parallelism that exists in the HPMS.

The eSRAM is designed for Single Error Correct Double Error Detect (SECDED) protection. When SECDED is disabled, the SRAM usually used to store SECDED data may be reused as an extra 16 KB of eSRAM.

Embedded NVM (eNVM)

The HPMS contains up to 512 KB of eNVM (64 bits wide).

DMA Engines

Two DMA engines are present in the HPMS: high-performance DMA and peripheral DMA.

High-Performance DMA (HPDMA)

The high-performance DMA (HPDMA) engine provides efficient memory to memory data transfers between an external DDR memory and internal eSRAM. This engine has two separate AHB-Lite interfaces—one to the MDDR bridge and the other to the AHB bus matrix. All transfers by the HPDMA are full word transfers.

Peripheral DMA (PDMA)

The peripheral DMA engine (PDMA) is tuned for offloading byte-intensive operations, involving HPMS peripherals, to and from the internal eSRAMs. Data transfers can also be targeted to user logic/RAM in the FPGA fabric.

APB Configuration Bus

On every IGLOO2 device memory, an APB configuration bus is present to allow the user to initialize the SERDES ASIC blocks, the fabric DDR memory controller, and user instantiated peripherals in the FPGA fabric.

Peripherals

A large number of communications and general purpose peripherals are implemented in the HPMS.

Communication Block (COMM_BLK)

The COMM block provides a UART-like communications channel between the HPMS and the system controller. System services are initiated through the COMM block. System services such as *Enter Flash*Freeze Mode* are initiated though this block.

SPI

The serial peripheral interface controller is compliant with the Motorola SPI, Texas Instruments synchronous serial, and National Semiconductor MICROWIRE™ formats. In addition, the SPI supports interfacing to large SPI flash and EEPROM devices by way of the slave protocol engine. The SPI controller supports both Master and Slave modes of operation.

The SPI controller embeds two 4×32 (depth × width) FIFOs for receive and transmit. These FIFOs are accessible through RX data and TX data registers. Writing to the TX data register causes the data to be written to the transmit FIFO. This is emptied by transmit logic. Similarly, reading from the RX data register causes data to be read from the receive FIFO.

Clock Sources: On-Chip Oscillators, PLLs, and CCCs

IGLOO2 devices have two on-chip RC oscillators—a 1 MHz RC oscillator and a 50 MHz RC oscillator—and the main crystal oscillator (32 KHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. These oscillators can be used in conjunction with the integrated user phase-locked loops (PLLs) and FAB_CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, power-on reset circuitry, and HPMS during the Flash*Freeze mode.

IGLOO2 devices have up to eight fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the eight PLLs and CCCs to generate the fabric clocks and the internal HPMS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the HPMS (HPMS_CCC) and an associated PLL (MPLL) for HPMS clocking and de-skewing the CLK_BASE clock. The fabric alignment clock controller (FACC), part of the HPMS CCC, is responsible for generating various aligned clocks required by the HPMS for correct operation of the HPMS blocks and synchronous communication with the user logic in the FPGA fabric.

High Speed Serial Interfaces

SERDES Interface

IGLOO2 FPGA has up to four 5 Gbps SERDES transceivers, each supporting the following:

- 4 SERDES/PCS lanes
- The native SERDES interface facilitates implementation of Serial RapidIO (SRIO) in fabric or a SGMII interface for a soft Ethernet MAC

PCI Express (PCIe)

PCIe is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 family has two hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block and following are the main features supported:

- Supports x1, x2, and x4 lane configuration
- Endpoint configuration only
- PCI Express Base Specification Revision 2.0
- 2.5 and 5.0 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 Kbytes maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL Master and Slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 x 64 bit base address registers
- 1 virtual channel (VC)

XAUI/XGXS Extension

The XAUI/XGXS extension allows the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the XGMII fabric interface through an appropriate soft IP block in the fabric.

High Speed Memory Interfaces: DDRx Memory Controllers

There are up to two DDR subsystems, MDDR (HPMS DDR) and FDDR (fabric DDR) present in IGLOO2 devices. Each subsystem consists of a DDR controller, PHY, and a wrapper. The MDDR has an interface to/from the HPMS and fabric, and FDDR provides an interface to/from the fabric.

The following are the main features supported by the FDDR and MDDR:

- Support for LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance
- Supports 1, 2, or 4 ranks of memory
- Supports different DRAM bus width modes: x8, x9, x16, x18, x32, and x36
- Supports DRAM burst length of 2, 4, or 8 in full bus-width mode; supports DRAM burst length of 2, 4, 8, or 16 in half bus-width mode
- Supports memory densities up to 4 GB
- Supports a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and Write buffers in fully associative CAMs, configurable in powers of 2, up to 64 Reads plus 64 Writes
- Support for dynamically changing clock frequency while in self-refresh
- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

MDDR Subsystem

The MDDR subsystem has two interfaces to the DDR. One is an AXI 64-bit bus from the DDR bridge within the HPMS. The other is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the MDDR subsystem after reset. This APB configuration bus is mastered by a master in the FPGA fabric. Support for 3.3 V Single Data Rate DRAMs (SDRAM) can be obtained by instantiating a soft AHB or AXI SDRAM memory controller in the FPGA fabric and connecting I/O ports to 3.3 V MSIO.

FDDR Subsystem

The FDDR subsystem has one interface to the DDR. This is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus can be mastered by a master in the FPGA fabric.

2 – Product Brief Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 13 (June 2016)	Updated Table 1 and Table 2 for grade 1 and 2 entries (SAR 80231). Updated the "IGLOO2 Ordering Information" image for grade 1 and 2 entries (SAR 80231). Added the grade 1 and grade 2 references in "IGLOO2 Datasheet and Pin Descriptions" (SAR 80231). Added grade 1 and 2 entries in "Description" (SAR 80231).	1-IV, 1-V 1-IX 1-XI 1-XII
Revision 12 (April 2016)	Updated Table 3 with more footnotes. (SAR 66079, SAR 77444, and SAR 73335).	V–VII
Revision 11 (October 2015)	Updated Table 1 (SAR 71995). Updated "Marking Specification Details" (SAR 71995). Updated "Low Power" (SAR 71995).	IV XI 1-3
Revision 10 (August 2015)	Updated Table 2 (SAR 69876). Added Table 5, Table 6, and Table 7 (SAR 69876). Updated "Marking Specification Details" (SAR 69876).	V VIII, X, X XI
Revision 9 (February 2015)	Updated Table 1, Table 2, Table 3, Table 4, and Table 8 Removed all instances of and references to M2GL100. VQ144 is replaced with TQ144 (SAR 62858). Updated Table 1-1 and Table 1-2 Updated "IGLOO2 Ordering Information" Added "IGLOO2 Development Tools"	IV, V, V, VII, XI 1-2 and 1-3 IX 1-9
Revision 8 (August 2014)	Updated Device Packages 005-VF256 and 150-FCS536 in Table 2–Table 4.	V–VII
Revision 7 (June 2014)	Updated Table 2, Table 3, and Table 4.	V, VII
Revision 6 (March 2014)	Table 1 to Table 4 and "IGLOO2 Ordering Information" were update with Military device data. The "Marking Specification Details" section and the "Available Programming Interfaces" table were added.	IV, VIII X, VII
Revision 5 (Dec 2013)	Tables 3-6 were combined into Table 4. Fabric Interface Controller features were added to "IGLOO2 FPGA Product Family" table. Packages VQ144 and FCV484 were added to Table 2 and Table 4.	VII, IV V, VII
Revision 4 (Nov 2013)	The Data Security Features section, table and the Device Status table were removed. “IGLOO2 FPGA Block Diagram” was updated.	N/A, III
Revision 3 (Oct 2013)	Packages FCS325 and VF256 were added to "I/Os Per Package". "IGLOO2 Ordering Information" was updated. Typo fixed in "IGLOO2 FPGA Block Diagram".	V, III

Revision	Changes	Page
Revision 2 (Sept 2013)	LSRAM x32/36 widths added. "IGLOO2 FPGA Product Family" table note added referring to updates in Table 4 –Table 6.	IV, V–VII
	"IGLOO2 Ordering Information" was updated. Part Numbers (tables 7 and 8) were removed. "IGLOO2 Device Status" section was updated.	VIII, XI
	M2GL090-FG676 and M2GL005-VF400 package pinouts finalized.	V
Revision 1	Initial release	NA

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO2 Device Status", is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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