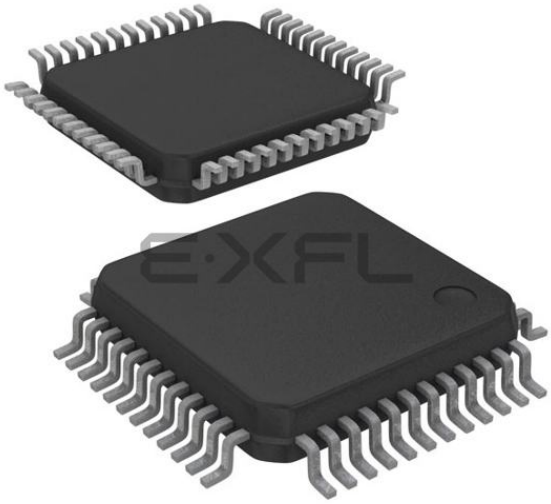
Renesas Electronics America Inc - R7FS128783A01CFL#AA0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, DALI, I²C, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 15x14b; D/A 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs128783a01cfl-aa0

1. Overview

The S128 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

Based on the energy-efficient ARM Cortex®-M0+ 32-bit core, this MCU is particularly suited for cost-sensitive and low-power applications. The MCU in this series has the following features:

- Up to 256 KB code flash memory
- 24-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- 14-bit A/D Converter (ADC14)
- 8-bit D/A Converter (DAC8)
- Security features.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M0+	• Maximum operating frequency: up to 32 MHz • ARM Cortex-M0+ - Revision: r0p1-00rel0 - ARMv6-M architecture profile - Single-cycle integer multiplier. • ARM Memory Protection Unit (MPU) - ARMv6 Protected Memory System Architecture - 8 protection regions. • SysTick timer - Driven by LOCO clock.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB code flash memory. See section 42, Flash Memory in User's Manual.
Data flash memory	4 KB data flash memory. See section 42, Flash Memory in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 6, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 41, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating mode	Two operating modes: • Single-chip mode • SCI boot mode. See section 3, Operating Modes in User's Manual.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC*1 = AVCC0 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5V, VREFH0 = 1.6 to AVCC0,

VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

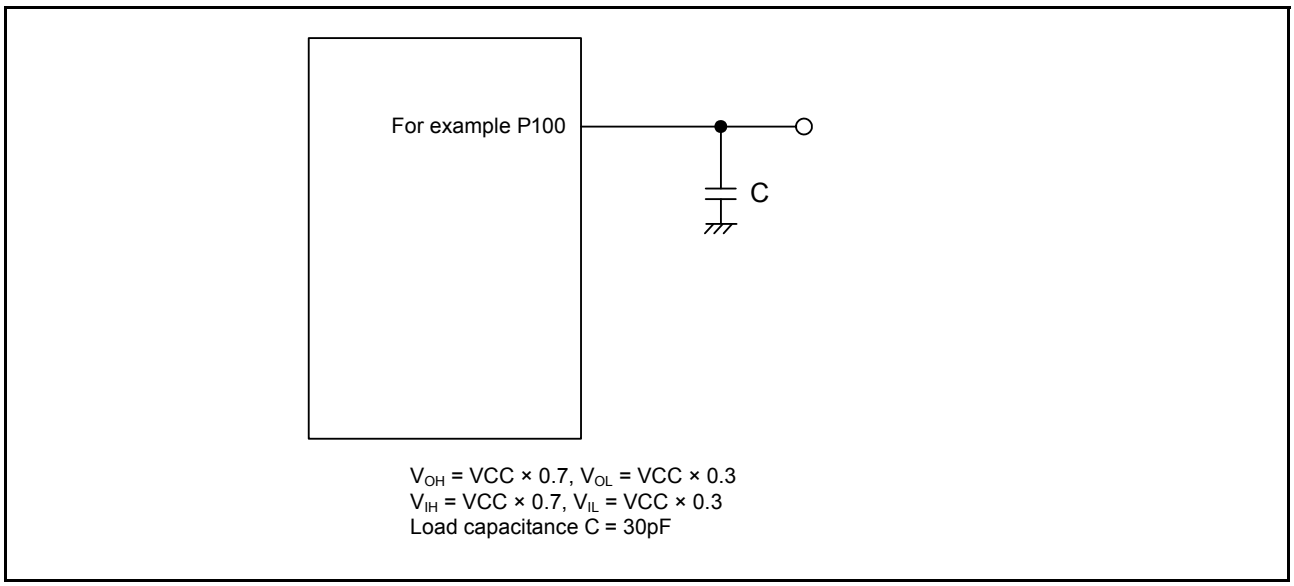


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

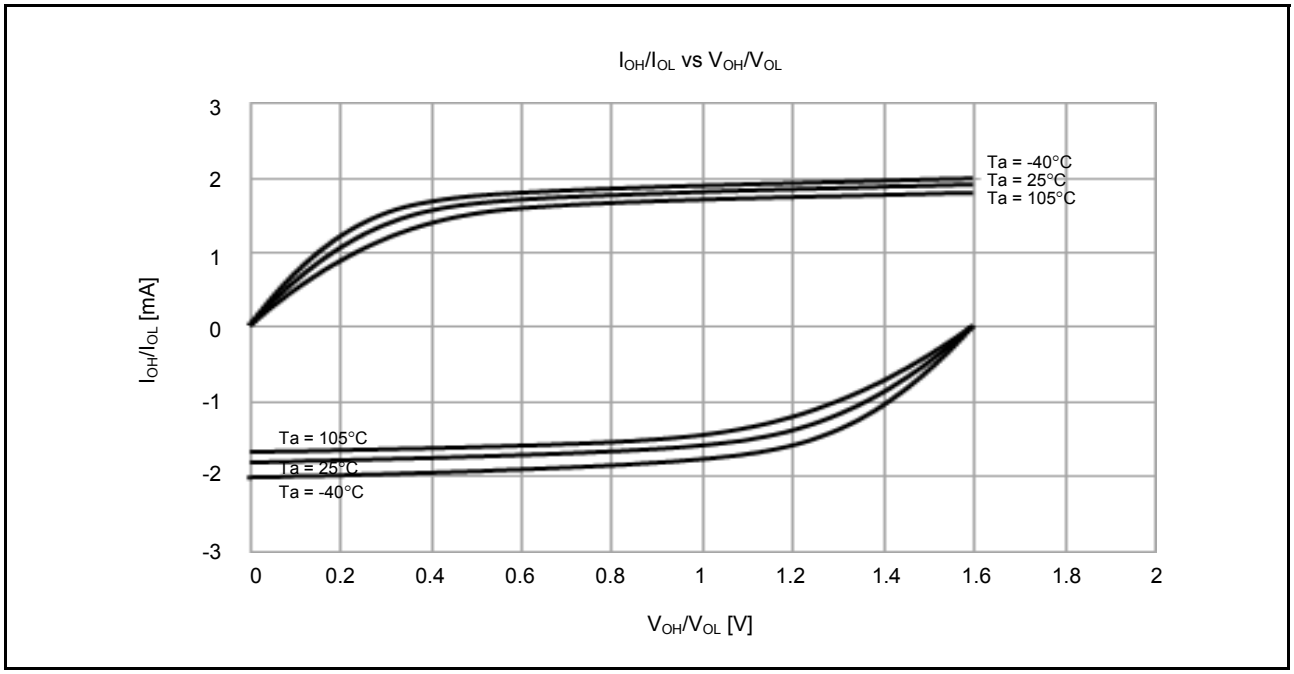


Figure 2.3 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when low drive output is selected (reference data, except for P914 and P915)

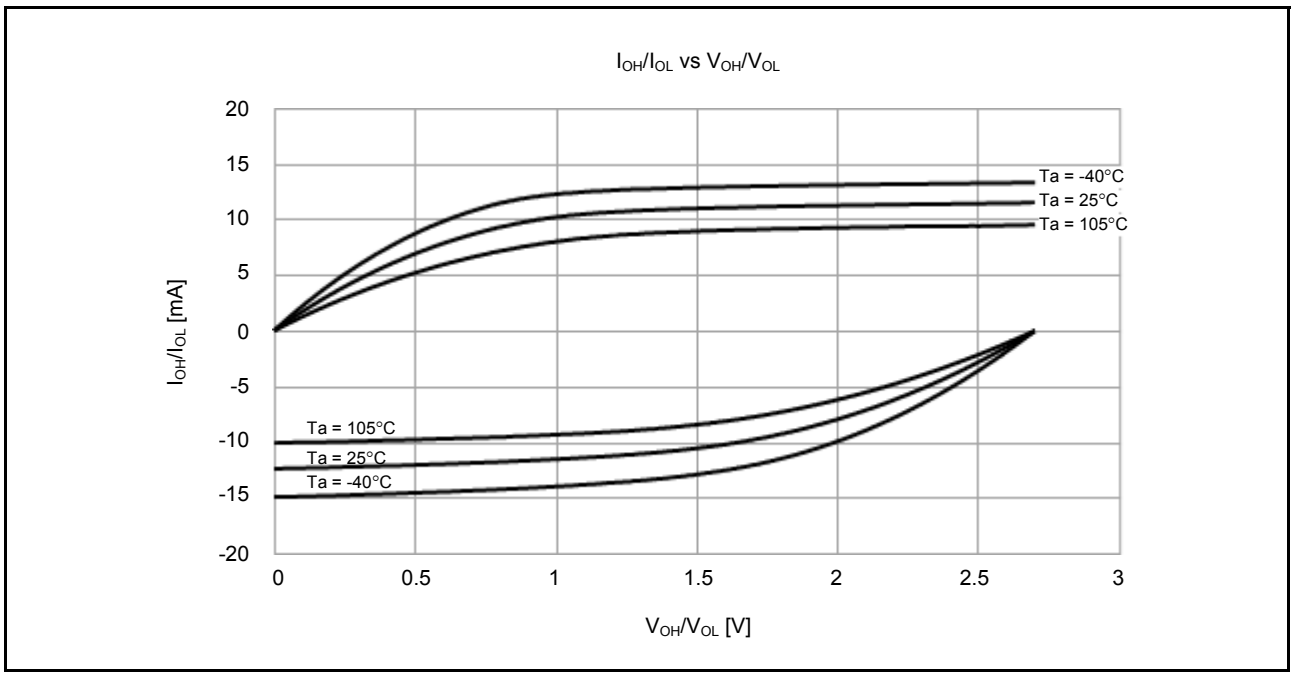
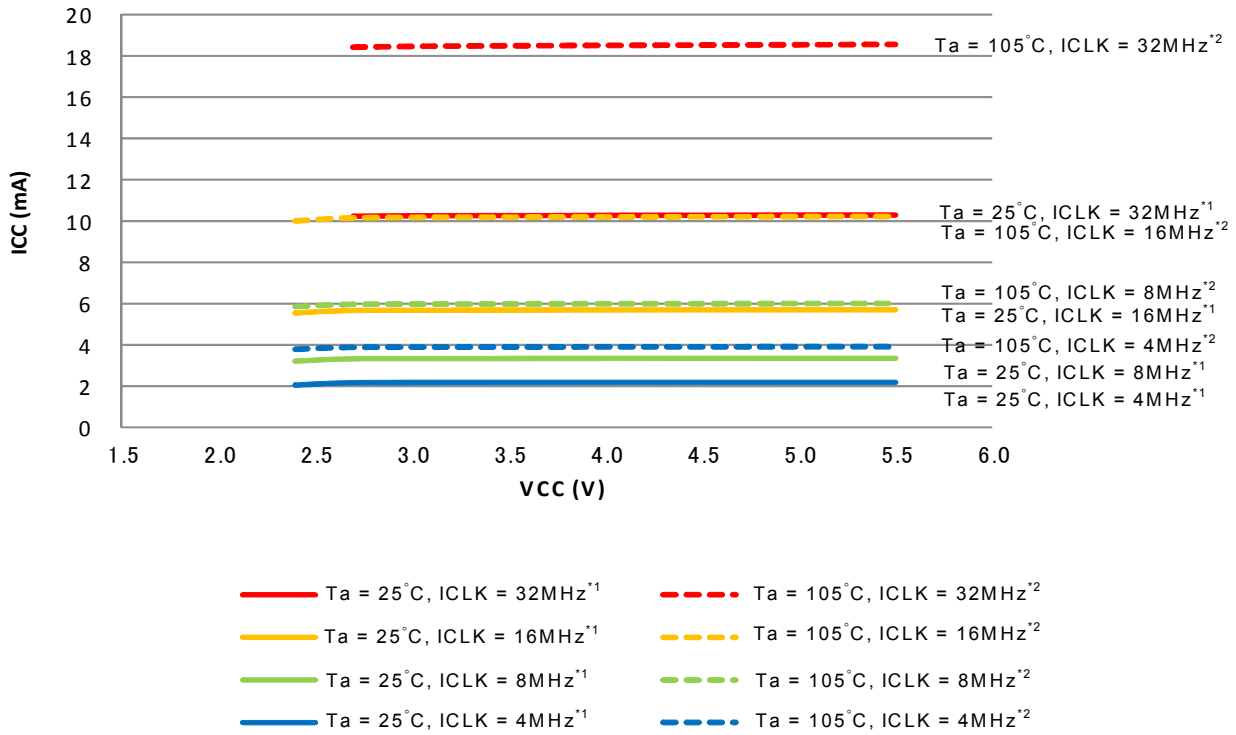


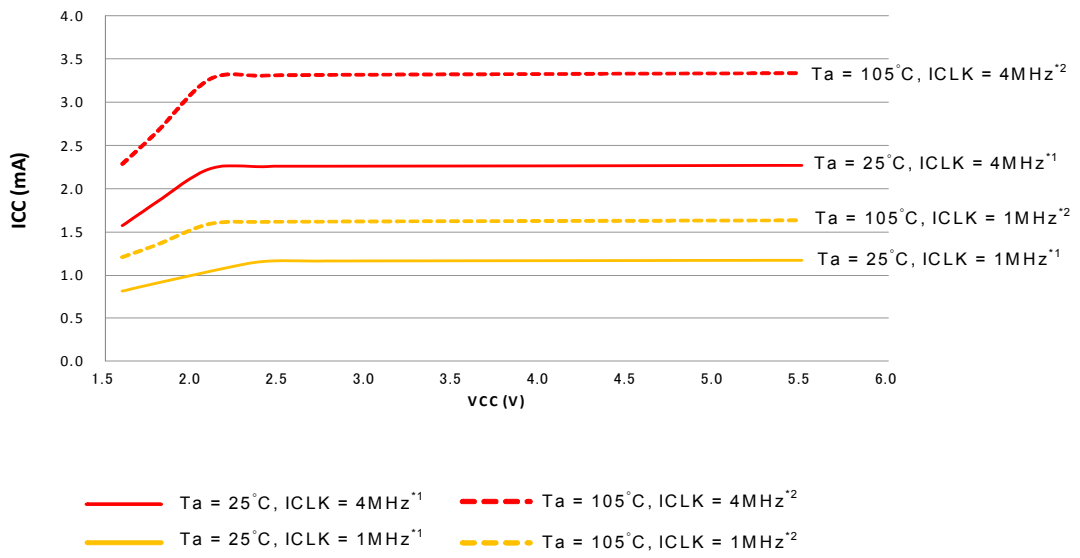
Figure 2.4 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when low drive output is selected (reference data, except for P914 and P915)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

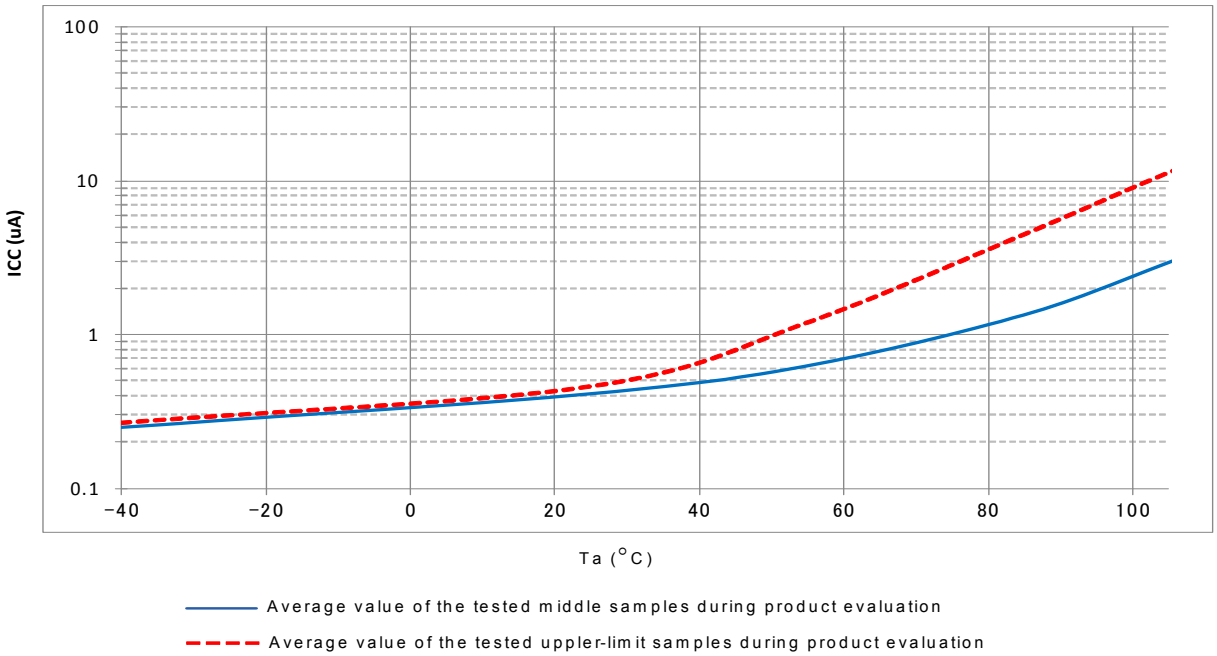
Figure 2.17 Voltage dependency in high-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.20 Voltage dependency in low-voltage mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.
Note 3. MOCO and DAC are stopped.

Figure 2.22 Temperature dependency in Software Standby mode (reference data)

Table 2.13 Operating and standby current (3)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Operational Amplifier operating current	Low power mode	1-unit operating	I_{AMP}	-	1.0	2.0	µA	-
		2-unit operating		-	1.5	3.0	µA	-
		3-unit operating		-	2.0	3.5	µA	-
		4-unit operating		-	2.5	4.5	µA	-
	High speed mode	1-unit operating		-	200	280	µA	-
		2-unit operating		-	320	450	µA	-
		3-unit operating		-	440	620	µA	-
		4-unit operating		-	560	790	µA	-
USB operating current	During USB communication under the following settings and conditions: • Function controller is in Full-Speed mode and - Bulk OUT transfer is (64 bytes) × 1 - Bulk IN transfer is (64 bytes) × 1 • Host device is connected by a 1-meter USB cable from the USB port.		I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	During suspended state under the following setting and conditions: • Function controller is in Full-Speed mode (the USB_DP pin is pulled up) • Software Standby mode • Host device is connected by a 1-meter USB cable from the USB port.		I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	µA	-
PWM Delay Generation Circuit current	PCLKD = 64 MHz, DLL Mode = 5-bit mode		I_{CC}	-	3.3	4.6	mA	-
	PCLKD = 64 MHz, DLL Mode = 4-bit mode			-	3.0	4.2	mA	-
	PCLKD = 32 MHz, DLL Mode = 5-bit mode			-	2.0	2.8	mA	-

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current is consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU in the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.

Note 5. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC140 module-stop bit) is in the module-stop state.

2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

Table 2.30 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.35
	Input/output data cycle (P002, P003, P010, P011)		t_{POcyc}	10	-	μs	-
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 2.36
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.37
		Dual edge		2.5	-		
AGT	AGTIO, AGTEE input cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	-	ns	Figure 2.38
		2.4 V ≤ VCC < 2.7 V		500	-	ns	
		1.8 V ≤ VCC < 2.4 V		1000	-	ns	
		1.6 V ≤ VCC < 1.8 V		2000	-	ns	
	AGTIO, AGTEE input high level width, low-level width	2.7 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		2.4 V ≤ VCC < 2.7 V		200	-	ns	
		1.8 V ≤ VCC < 2.4 V		400	-	ns	
		1.6 V ≤ VCC < 1.8 V		800	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output frequency	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	-	ns	Figure 2.38
		2.4 V ≤ VCC < 2.7 V		125	-	ns	
		1.8 V ≤ VCC < 2.4 V		250	-	ns	
		1.6 V ≤ VCC < 1.8 V		500	-	ns	
ADC14	14-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.39
KINT	Key interrupt input low-level width		t_{KR}	250	-	ns	Figure 2.40

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

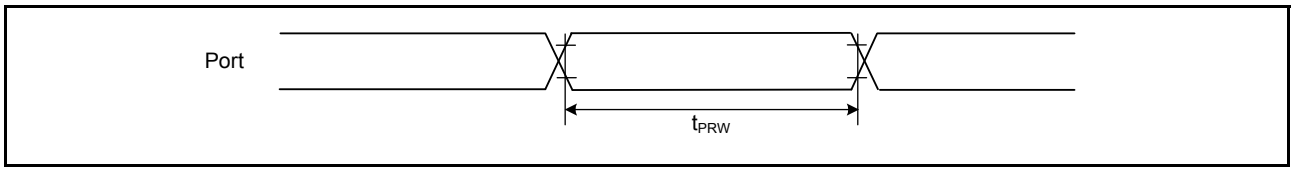


Figure 2.35 I/O ports input timing

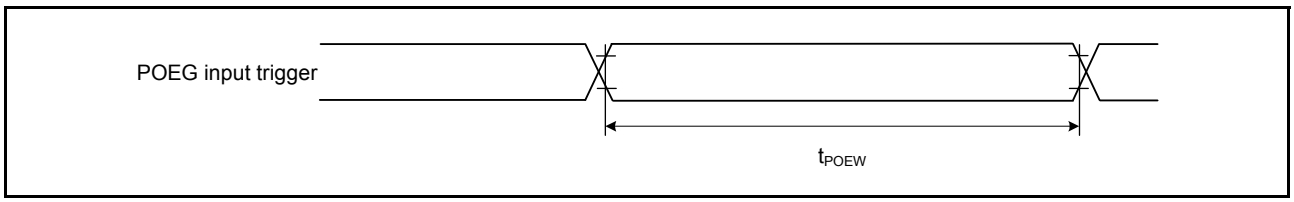


Figure 2.36 POEG input trigger timing

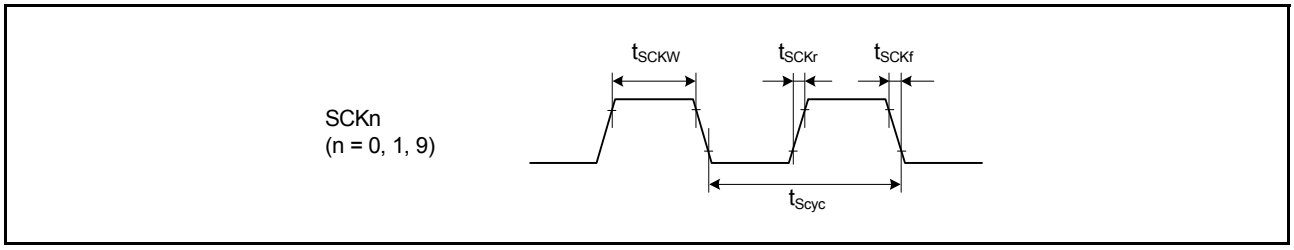


Figure 2.41 SCK clock input timing

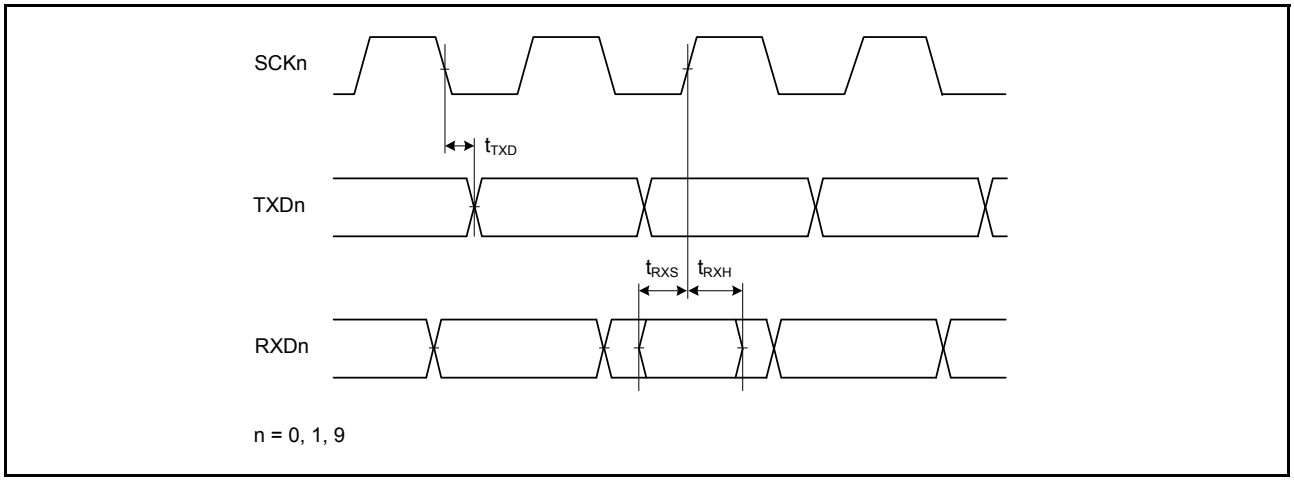


Figure 2.42 SCI input/output timing in clock synchronous mode

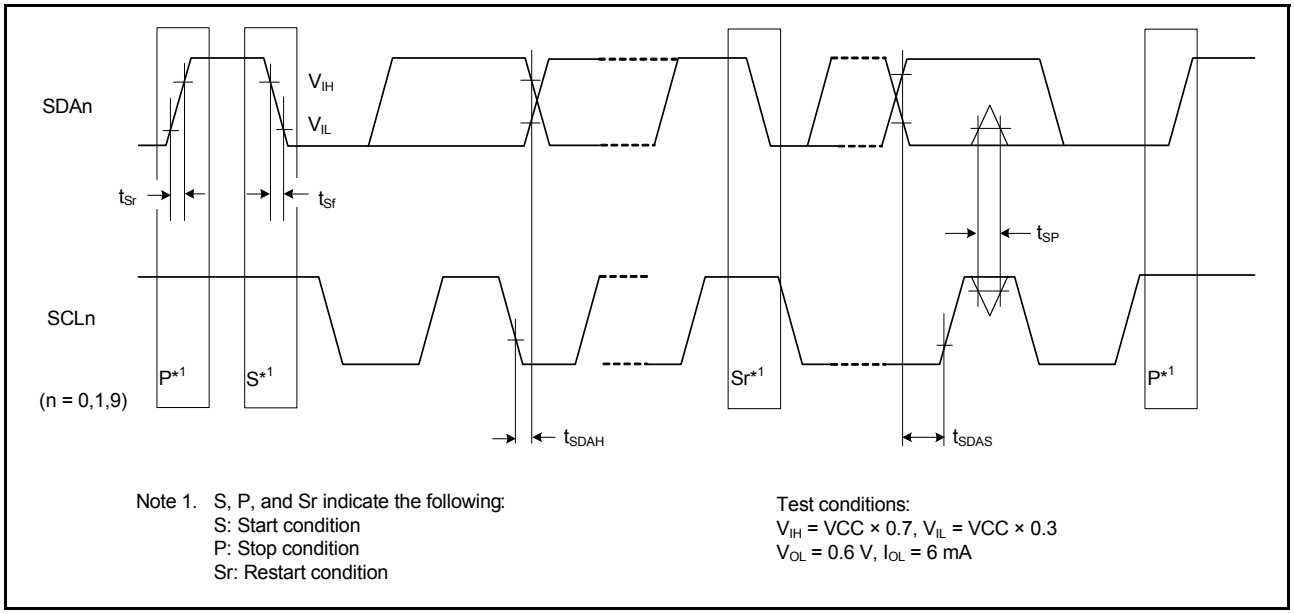


Figure 2.48 SCI simple IIC mode timing

2.3.10 SPI Timing

Table 2.36 SPI timing (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.49 C = 30pF
		Slave			6	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Output	2.7V or above	t_{SPCKr}, t_{SPCKf}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	µs	

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.

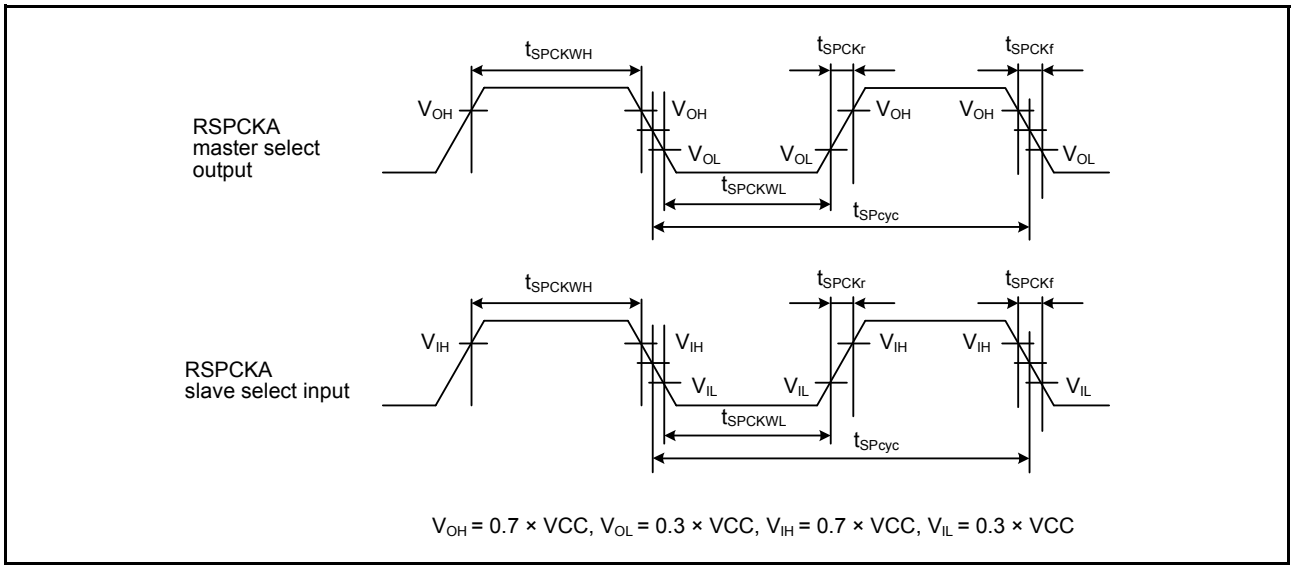


Figure 2.49 SPI clock timing

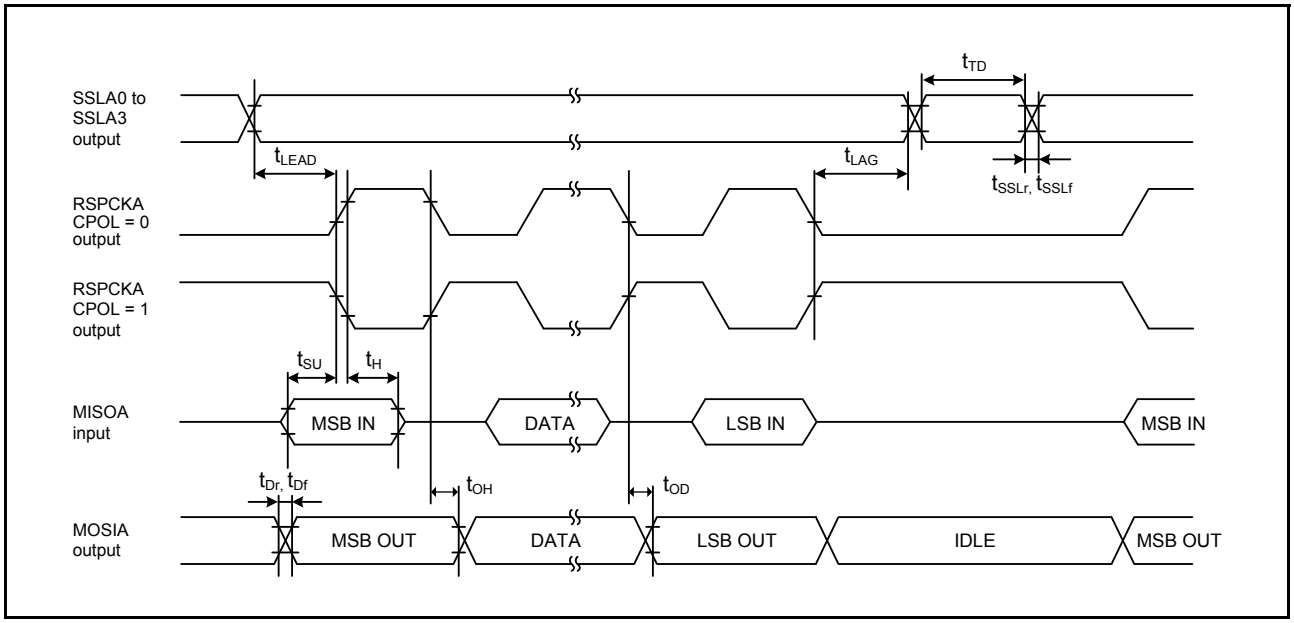


Figure 2.50 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

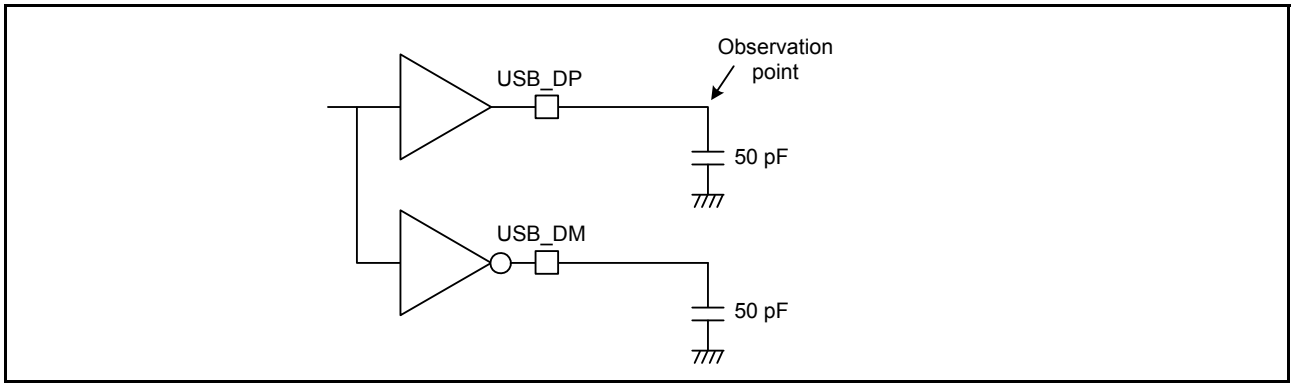


Figure 2.59 Test circuit for Full-Speed (FS) connection

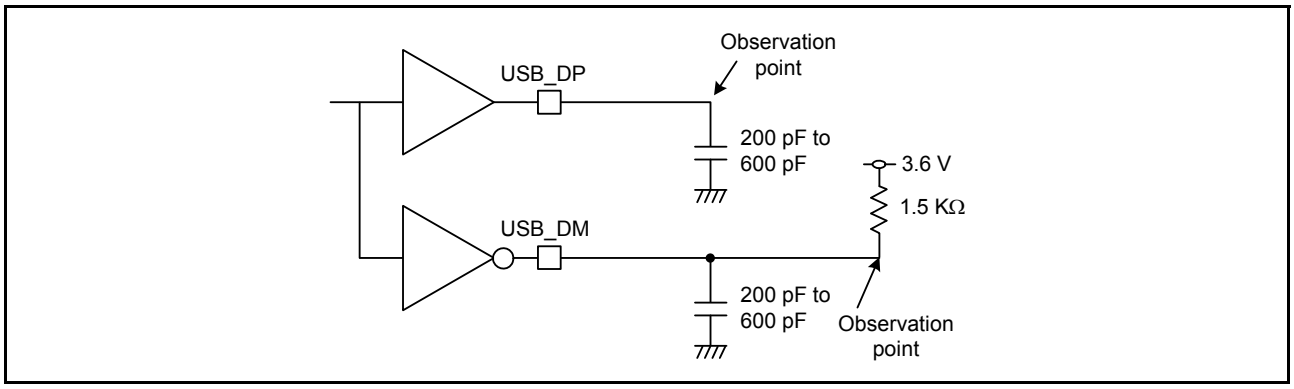


Figure 2.60 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.40 USB regulator

Parameter		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

Table 2.41 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions
Offset error	-	±2.0	±18	LSB	High-precision channel
			±24.0	LSB	Other than above
Full-scale error	-	±3.0	±18	LSB	High-precision channel
			±24.0	LSB	Other than above
Quantization error	-	±0.5	-	LSB	-
Absolute accuracy	-	±5.0	±20	LSB	High-precision channel
			±32.0	LSB	Other than above
DNL differential nonlinearity error	-	±4.0	-	LSB	-
INL integral nonlinearity error	-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Table 2.42 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	48	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.94	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.50	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.06	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h

Table 2.46 A/D conversion characteristics (6) in low-power A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions
Offset error	-	±4.0	±30.0	LSB	High-precision channel
			±40.0	LSB	Other than above
Full-scale error	-	±6.0	±30.0	LSB	High-precision channel
			±40.0	LSB	Other than above
Quantization error	-	±0.5	-	LSB	-
Absolute accuracy	-	±12.0	±32.0	LSB	High-precision channel
			±48.0	LSB	Other than above
DNL differential nonlinearity error	-	±4.0	-	LSB	-
INL integral nonlinearity error	-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Table 2.47 A/D conversion characteristics (7) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V, VSS = AVSS0 = VREFL0 = 0
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	4	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	13.5	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		20.25	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	15.0	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		21.75	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h

Table 2.54 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset enable time	$t_{W\ (POR)}$	1	-	-	ms	Figure 2.65, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)	$T_{d\ (E-A)}$	-	-	300	µs	Figure 2.67, Figure 2.68
Hysteresis width (POR)	V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0
Note 2. When OFS1.LVDAS = 1
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

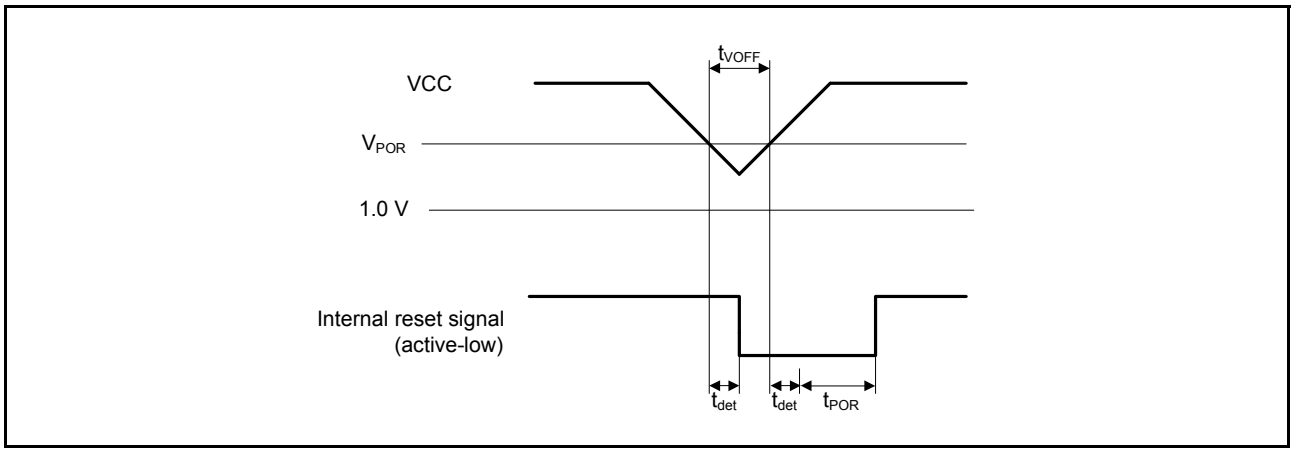
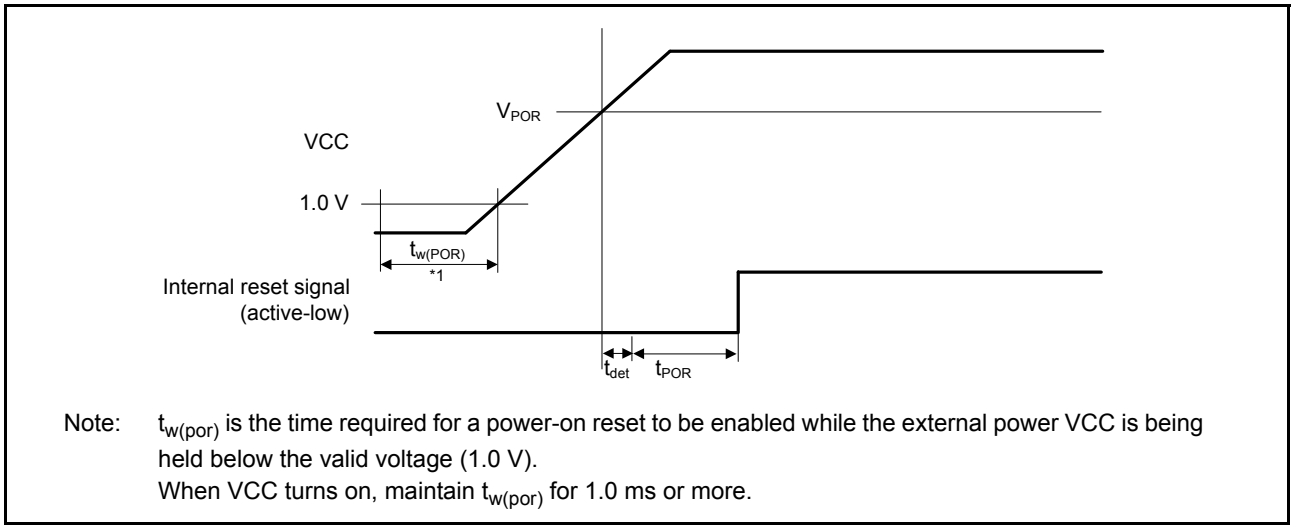


Figure 2.64 Voltage detection reset timing



Note: $t_{w(por)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(por)}$ for 1.0 ms or more.

Figure 2.65 Power-on reset timing

Table 2.58 OPAMP characteristics (2 of 2)
Conditions: 1.8 V ≤ AVCC0 = VCC ≤ 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Open gain	A_V	-		80	120	-	dB
Gain-bandwidth (GB) product	GBW1	Low-power mode		-	0.012	-	MHz
	GBW2	High-speed mode		-	1.7	-	
Phase margin	PM	CL = 20 pF		50	-	-	deg
Gain margin	GM	CL = 20 pF		10	-	-	dB
Equivalent input noise	V_{noise1}	f = 10 Hz	Low-power mode	-	700	-	nV/√Hz
	V_{noise2}	f = 1 kHz		-	400	-	
	V_{noise3}	f = 1 kHz	High-speed mode	-	90	-	
	V_{noise4}	f = 100 kHz		-	50	-	
Power supply reduction ratio	PSRR	-		-	90	-	dB
Common mode signal reduction ratio	CMRR	-		-	90	-	dB
Stabilization wait time	T_{std1}	CL = 20 pF Only operational amplifier is activated.*1	Low-power mode VCC < 3.6V	1800	-	-	µs
			Low-power mode VCC < 5.5V	2500	-	-	
	T_{std2}		High-speed mode	13	-	-	
	T_{std3}	CL = 20 pF Operational amplifier and reference current circuit are activated simultaneously.	Low-power mode VCC < 3.6V	1800	-	-	
			Low-power mode VCC < 5.5V	2500	-	-	
	T_{std4}		High-speed mode	13	-	-	
Settling time	T_{set1}	CL = 20 pF	Low-power mode VCC < 3.6V	-	-	1400	µs
			Low-power mode VCC < 5.5V	-	-	2000	µs
	T_{set2}		High-speed mode	-	-	13	µs
Slew rate	T_{slew1}	CL = 20 pF	Low-power mode	-	0.005	-	V/µs
	T_{slew2}		High-speed mode	-	1.1	-	V/µs
Load current	I_{load1}	Low-power mode		–100	-	100	µA
	I_{load2}	High-speed mode		–100	-	100	
Load capacitance	CL	-		-	-	20	pF

Note 1. When the operational amplifier and the reference current circuit have already been activated.

2.13 Flash Memory Characteristics

2.13.1 Code Flash Memory Characteristics

Table 2.59 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2, *3	-	-	Year	T_a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.60 Code flash characteristics (2)

High-speed operating mode
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4 bytes	t_{P4}	-	116	998	-	54	506	µs
Erasure time	1 KB	t_{E1K}	-	9.03	287	-	5.67	222	ms
Blank check time	4 bytes	t_{BC4}	-	-	56.8	-	-	16.6	µs
	1 KB	t_{BC1K}	-	-	1899	-	-	140	µs
Erase suspended time		t_{SED}	-	-	22.5	-	-	10.7	µs
Startup area switching setting time		t_{SAS}	-	21.9	585	-	12.1	447	ms
Access window time		t_{AWS}	-	21.9	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	21.9	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	5	-	-	5	-	-	µs

Note 1. Does not include the time until each operation of the flash memory is started after instructions are executed by the software.

Note 2. The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 3. The frequency accuracy of ICLK must be ±3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

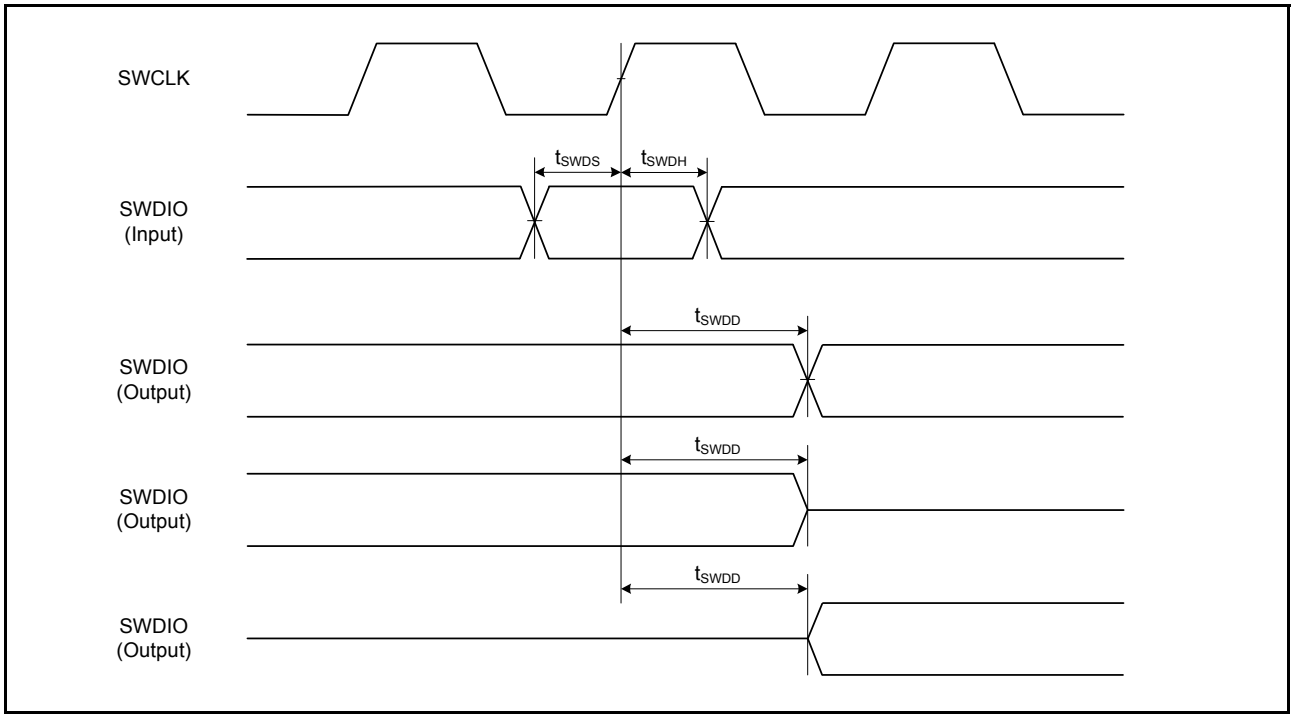
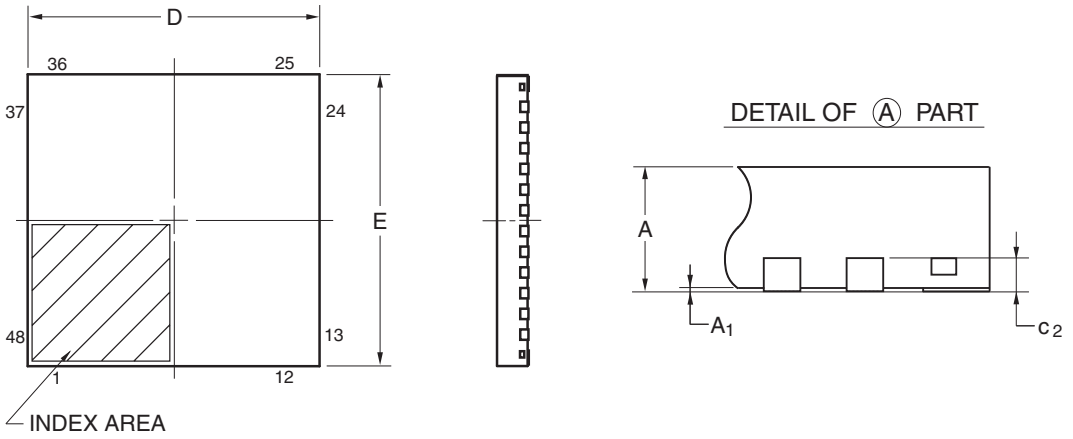
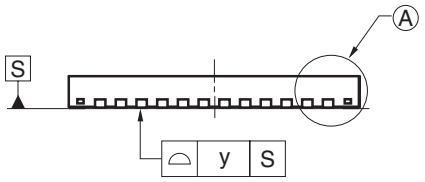
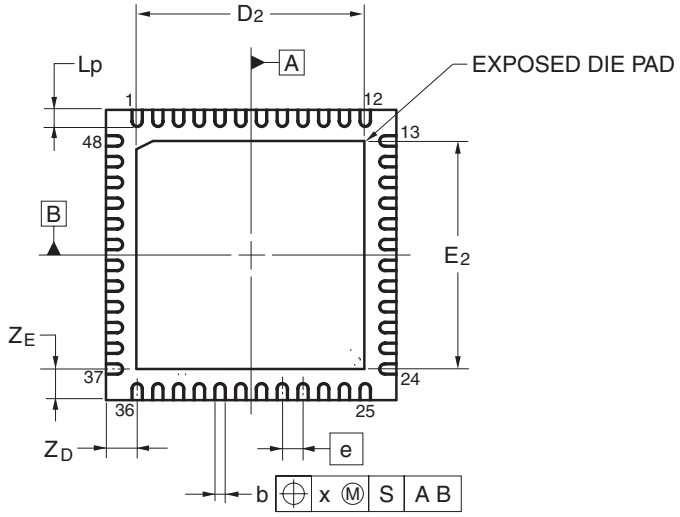


Figure 2.70 SWD input/output timing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13







Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

Figure 1.5 QFN 48-pin

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