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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, DALI, I²C, SCI, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 21x14b; D/A 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs128783a01cfm-aa0

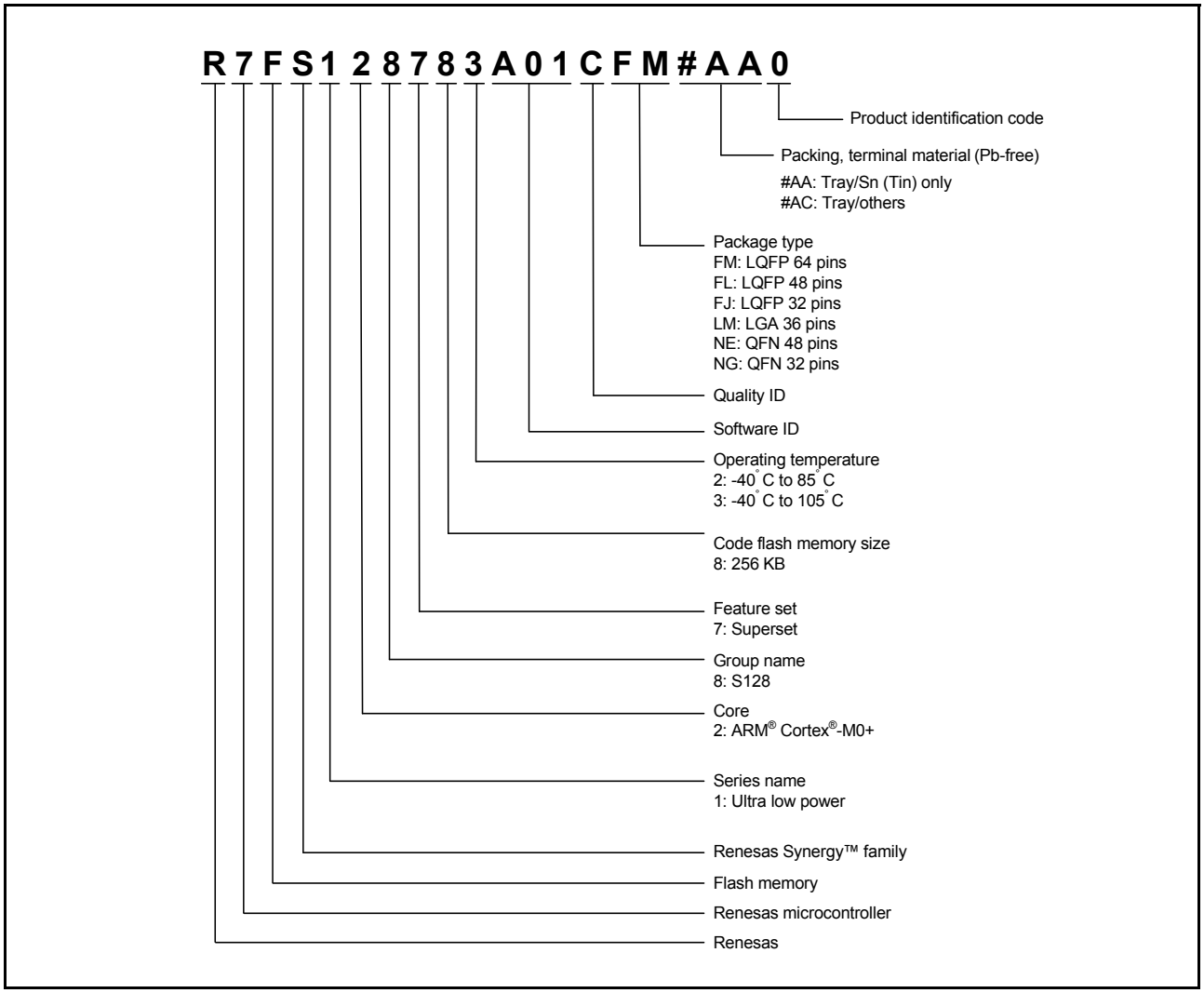


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FS128783A01CFM	R7FS128783A01CFM#AA0	PLQP0064KB-C	256 KB	4 KB	24 KB	–40 to +105°C
R7FS128783A01CFL	R7FS128783A01CFL#AA0	PLQP0048KB-B				–40 to +105°C
R7FS128783A01CNE	R7FS128783A01CNE#AC0	PWQN0048KB-A				–40 to +105°C
R7FS128782A01CLM	R7FS128782A01CLM#AC0	PWLG0036KA-A				–40 to +85°C
R7FS128783A01CFJ	R7FS128783A01CFJ#AA0	PLQP0032GB-A				–40 to +105°C
R7FS128783A01CNG	R7FS128783A01CNG#AC0	PWQN0032KB-A				–40 to +105°C

1.4 Function Comparison

Table 1.13 Function comparison (1 of 2)

Parts number	R7FS128783A01CFM	R7FS128783A01CFL R7FS128783A01CNE	R7FS128782A01CLM	R7FS128783A01CFJ R7FS128783A01CNG
Pin count	64	48	36	32
Package	LQFP	LQFP/QFN	LGA	LQFP/QFN
Code flash memory	256 KB			

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low
DALI	DRX0	Input	Input pin for DALI received data
	DTX0	Output	Output pin for DALI transmitted data
IIC	SCL0, SCL1	I/O	Input/output pins for clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D– I/O pin of the USB on-chip transceiver. This pin should be connected to the D– pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin

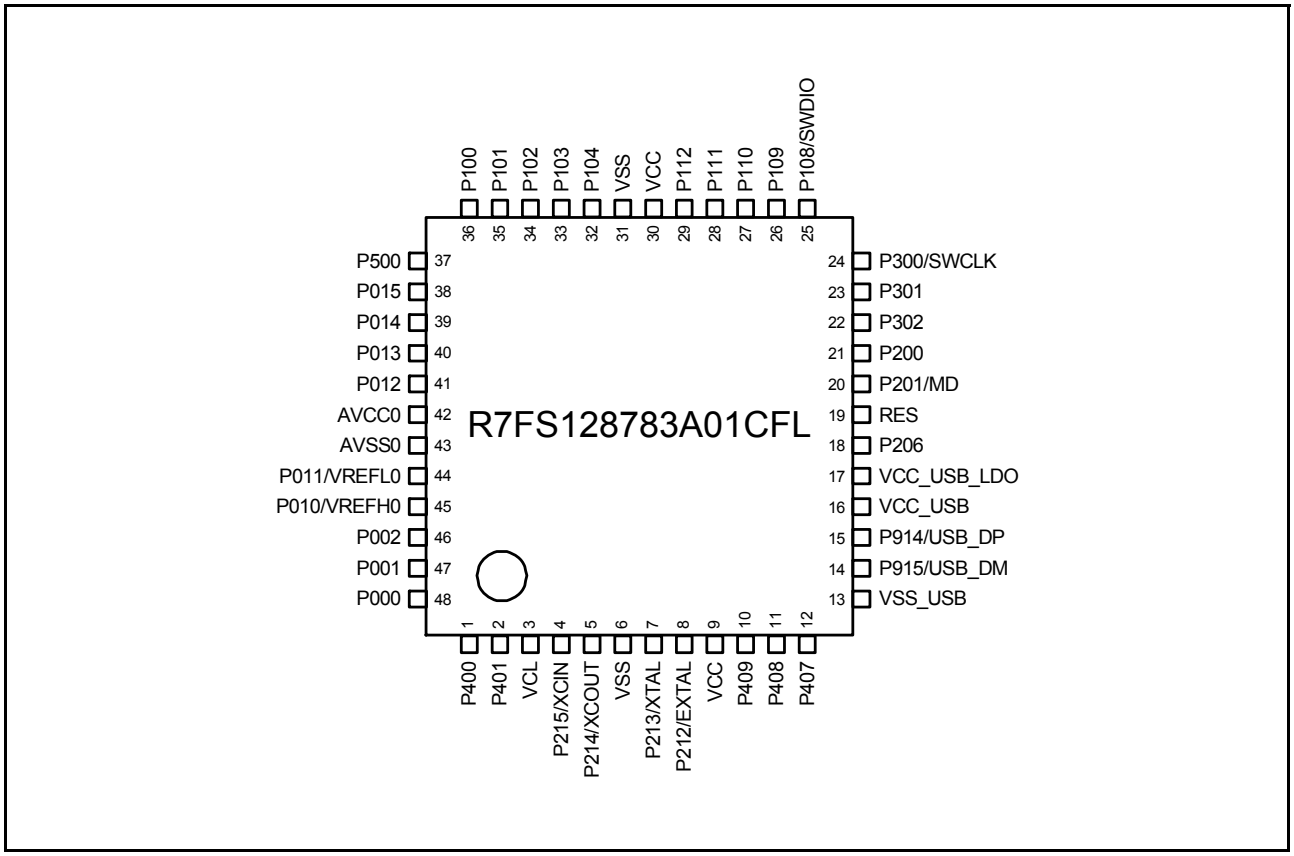


Figure 1.4 Pin assignment for LQFP 48-pin

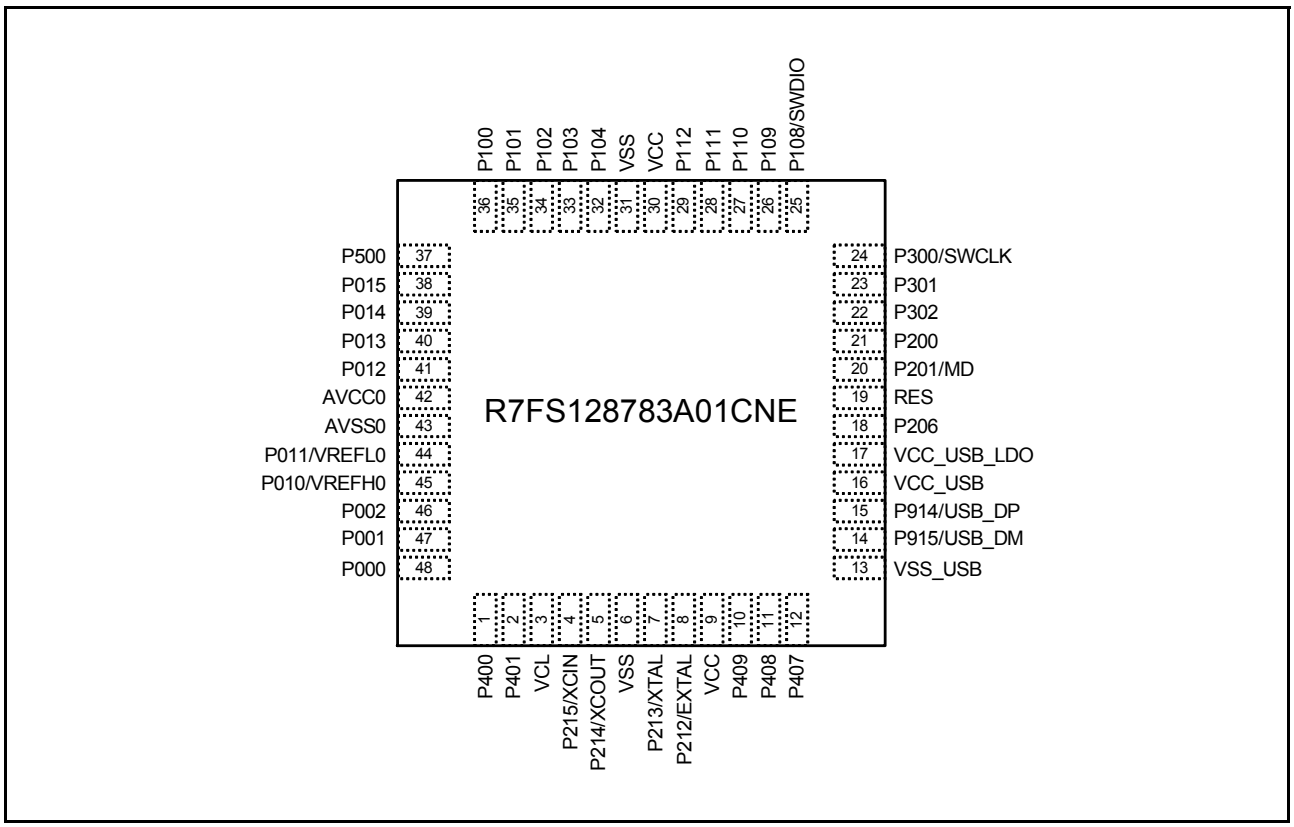


Figure 1.5 Pin assignment for QFN 48-pin

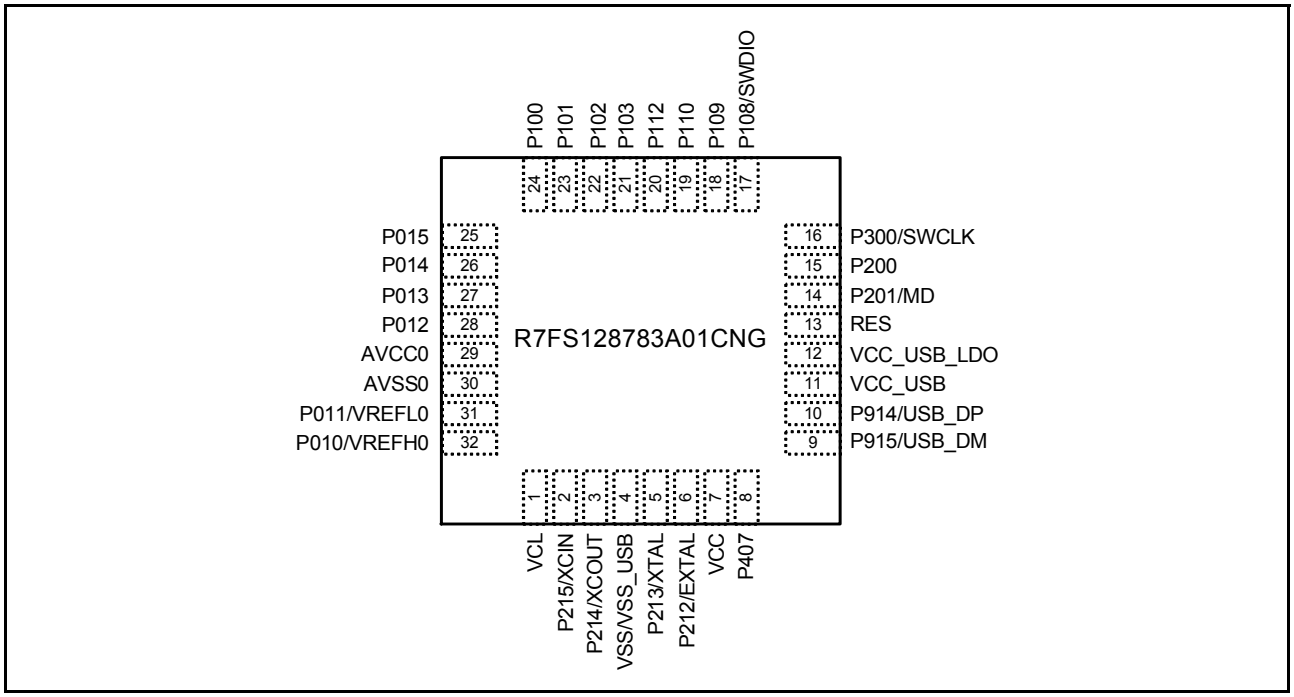


Figure 1.8 Pin assignment for QFN 32-pin

1.7 Pin Lists

Pin number								Timers				Communication Interfaces				Analogs				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32	Power, System, Clock, Debug, CAC	I/O ports	AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
1	1	1	-	-	-	CACREF_C	P400	AGTIO1_D		GTIOC6A_A			SCK0_B/SCK1_B	SCL0_A						TS20	IRQ0
2	2	2	-	-	-		P401		GTETRGA_B	GTIOC6B_A		CTX0_B	CTS0_RTS0_B/SS0_B/TXD1_B/MOSI1_B/SDA1_B	SDA0_A						TS19	IRQ5
3	-	-	-	-	-		P402			GTIOC3B_B		CRX0_B	RXD1_B/MISO1_B/SCL1_B							TS18	IRQ4
4	-	-	-	-	-		P403			GTIOC3A_B			CTS1_RTS1_B/SS1_B							TS17	
5	3	3	A1	1	1	VCL															
6	4	4	B1	2	2	XCIN	P215														
7	5	5	C1	3	3	XCOUT	P214														
8	6	6	D1	4	4	VSS															
9	7	7	D3	5	5	XTAL	P213		GTETRGA_D	GTIOC0A_D			TXD1_A/MOSI1_A/SDA1_A								IRQ2
10	8	8	D2	6	6	EXTAL	P212	AGTEE1	GTETRGB_D	GTIOC0B_D			RXD1_A/MISO1_A/SCL1_A								IRQ3
11	9	9	E1	7	7	VCC															
12	-	-	-	-	-		P411	AGTOA1	GTOVUP_B	GTIOC6A_B			TXD0_B/MOSI0_B/SDA0_B		MOSIA_B					TS07	IRQ4
13	-	-	-	-	-		P410	AGTOB1	GTOVLO_B	GTIOC6B_B			RXD0_B/MISO0_B/SCL0_B		MISOA_B					TS06	IRQ5
14	10	10	-	-	-		P409		GTOWUP_B	GTIOC5A_B			TXD0_E/MOSI0_E/SDA0_E/TXD9_A/MOSI9_A/SDA9_A							TS05	IRQ6
15	11	11	-	-	-		P408		GTOWLO_B	GTIOC5B_B			RXD9_A/MISO9_A/SCL9_A	SCL0_C						TS04	IRQ7
16	12	12	E2	8	8		P407	AGTIO0_C		GTIOC0A_E	RTCOUT	USB_VBUS	CTS0_RTS0_D/SS0_D	SDA0_B	SSLB3_A	ADTRG0_B				TS03	
17	13	13	D1	4	4	VSS_USB															

Pin number						Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs				HMI	
LQFP64	LQFP48	QFN48	LGA36	LQFP32	QFN32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN, DALI	SCI	IIC	SPI	ADC14	DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
18	14	14	F2	9	9		P915					USB_DM									
19	15	15	F3	10	10		P914					USB_DP									
20	16	16	F4	11	11	VCC_USB															
21	17	17	F5	12	12	VCC_USB_LDO															
22	18	18	-	-	-		P206		GTIU_A				RXD0_D/ MISO0_D/ SCL0_D	SDA1_A	SSLB1_A					TS01	IRQ0
23	-	-	-	-	-	CLKOUT_A	P205	AGTO1	GTIV_A	GTIOC4A_B			TXD0_D/ MOSI0_D/ SDA0_D/ CTS9_RTS9_A/SS9_A	SCL1_A	SSLB0_A					TSCAP_A	IRQ1
24	-	-	-	-	-	CACREF_A	P204	AGTIO1_A	GTIW_A	GTIOC4B_B			SCK0_D/ SCK9_A	SCL0_B	RSPCKB_A					TS00	
25	19	19	E3	13	13	RES															
26	20	20	E4	14	14	MD	P201														
27	21	21	E5	15	15		P200														NMI
28	-	-	-	-	-		P304			GTIOC1A_B											
29	-	-	-	-	-		P303			GTIOC1B_B										TS02	
30	22	22	-	-	-		P302		GTOUUP_A	GTIOC4A_A					SSLB3_B					TS08	IRQ5
31	23	23	-	-	-		P301	AGTIO0_D	GTOULO_A	GTIOC4B_A			CTS9_RTS9_D/ SS9_D		SSLB2_B					TS09	IRQ6
32	24	24	F6	16	16	SWCLK	P300		GTOUUP_C	GTIOC0A_A					SSLB1_B						
33	25	25	E6	17	17	SWDIO	P108		GTOULO_C	GTIOC0B_A			CTS9_RTS9_B/SS9_B		SSLB0_B						
34	26	26	D4	18	18	CLKOUT_B	P109		GTOVUP_A	GTIOC1A_A		CTX0_A	SCK1_E/ TXD9_B/ MOSI9_B/ SDA9_B		MOSIB_B					TS10	
35	27	27	D5	19	19		P110		GTOVLO_A	GTIOC1B_A		CRX0_A	CTS0_RTS0_C/ SS0_C/ RXD9_B/ MISO9_B/ SCL9_B		MISOB_B			VCOUT		TS11	IRQ3
36	28	28	D6	-	-		P111	AGTOA0		GTIOC3A_A			SCK0_C/ SCK9_B		RSPCKB_B					TS12	IRQ4
37	29	29	C6	20	20		P112	AGTOB0		GTIOC3B_A			TXD0_C/ MOSI0_C/ SDA0_C/ SCK1_D		SSLB0_C					TSCAP_C	
38	-	-	-	-	-		P113			GTIOC2A_C											
39	30	30	-	-	-	VCC															
40	31	31	-	-	-	VSS															
41	-	-	-	-	-		P107			GTIOC0A_B											KR07
42	-	-	-	-	-		P106			GTIOC0B_B					SSLA3_A	AN016					KR06
43	-	-	-	-	-		P105		GTETRGA_C	GTIOC1A_C					SSLA2_A	AN017					KR05/ IRQ0
44	32	32	-	-	-		P104		GTETRGB_B	GTIOC1B_C			RXD0_C/ MISO0_C/ SCL0_C		SSLA1_A	AN018				TS13	KR04/ IRQ1
45	33	33	C3	21	21		P103		GTOWUP_A	GTIOC2A_A		CTX0_C	CTS0_RTS0_A/SS0_A		SSLA0_A	AN019		CMPREF1		TS14	KR03
46	34	34	C4	22	22		P102	AGTO0	GTOWLO_A	GTIOC2B_A		CRX0_C	SCK0_A		RSPCKA_A	AN020/ ADTRG0_A		CMPIN1		TS15	KR02
47	35	35	C5	23	23		P101	AGTEE0	GTETRGB_A	GTIOC5A_A		DTX0	TXD0_A/ MOSI0_A/ SDA0_A/ CTS1_RTS1_A/SS1_A	SDA1_B	MOSIA_A	AN021		CMPREF0		TS16	KR01/ IRQ1
48	36	36	B6	24	24		P100	AGTIO0_A	GTETRGA_A	GTIOC5B_A		DRX0	RXD0_A/ MISO0_A/ SCL0_A/ SCK1_A	SCL1_B	MISOA_A	AN022		CMPIN0		TS26	KR00/ IRQ2
49	37	37	-	-	-		P500									AN013	DA1_B			TS27	
50	-	-	-	-	-		P501									AN012			AMP3+		
51	-	-	-	-	-		P502									AN011			AMP3-		
52	38	38	A6	25	25		P015									AN010	DA1_A	IVCMP1	AMP2+	TS28	IRQ7
53	39	39	A5	26	26		P014									AN009	DA0	IVREF1	AMP2-	TS29	
54	40	40	B5	27	27		P013									AN008		IVCMP0	AMP1+		
55	41	41	B4	28	28		P012									AN007		IVREF0	AMP1-		

Table 2.5 I/O V_{IH}, V_{IL} (2)
Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	VCC × 0.8	-	-3	V	-
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.01	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	VCC × 0.8	-	5.8		
		V_{IL}	-	-	VCC × 0.2		
	P000 to P004 P010 to P015 P500 to P502	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	EXTAL Input ports pins except for P000 to P004, P010 to P015, P500 to P502, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		

Note 1. P205, P206, P400, P401, P407 (total 5pins)

2.2.6 Output Characteristics for I/O Pins (Middle Drive Capacity)

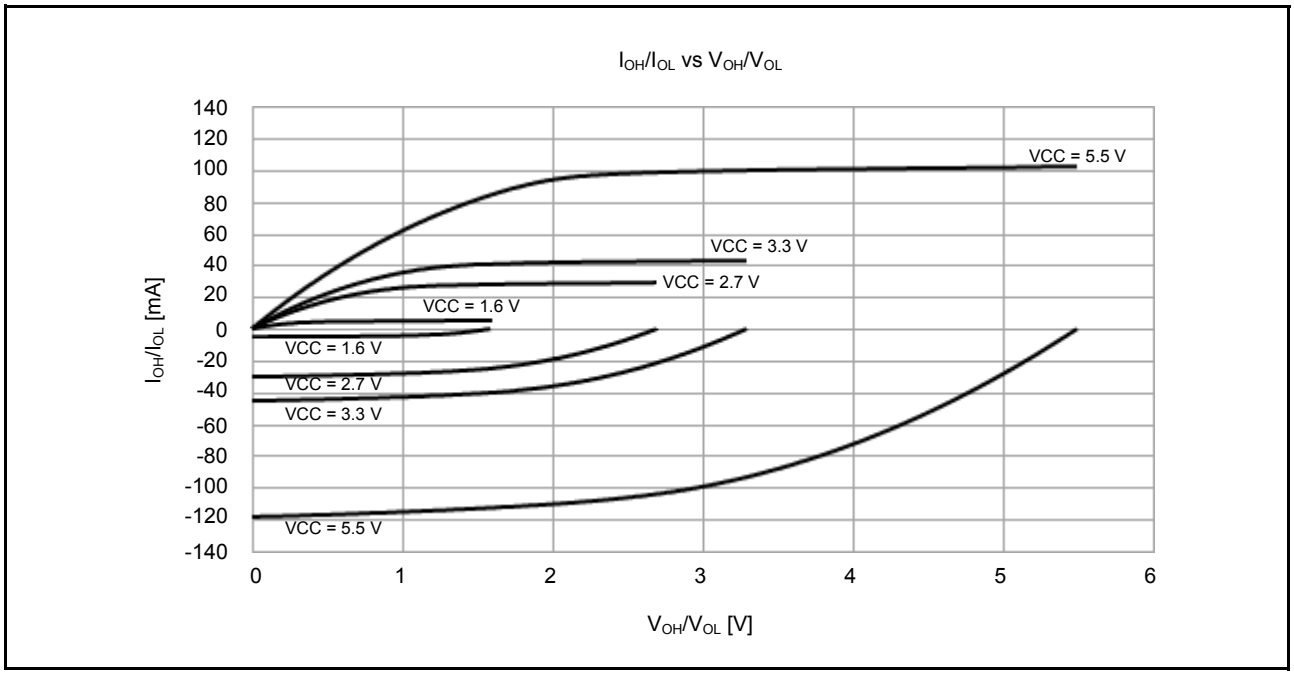


Figure 2.7 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data, except for P914 and P915)**

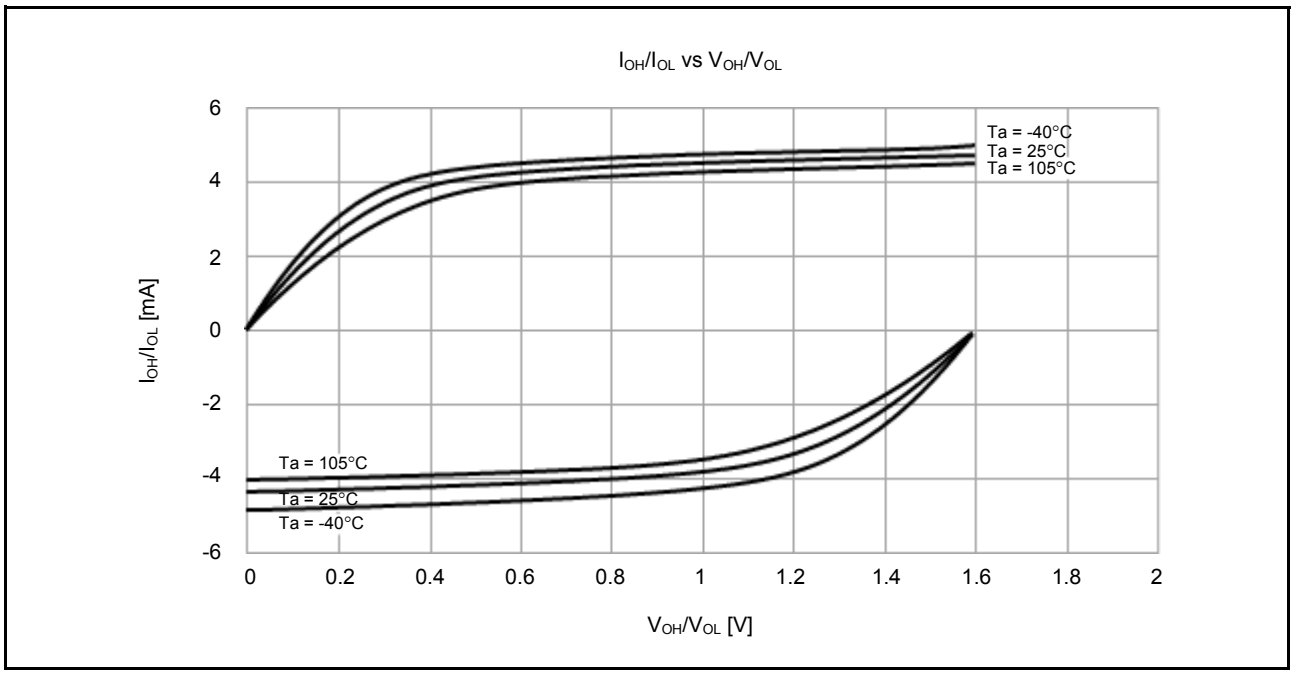


Figure 2.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when middle drive output is selected (reference data, except for P914 and P915)**

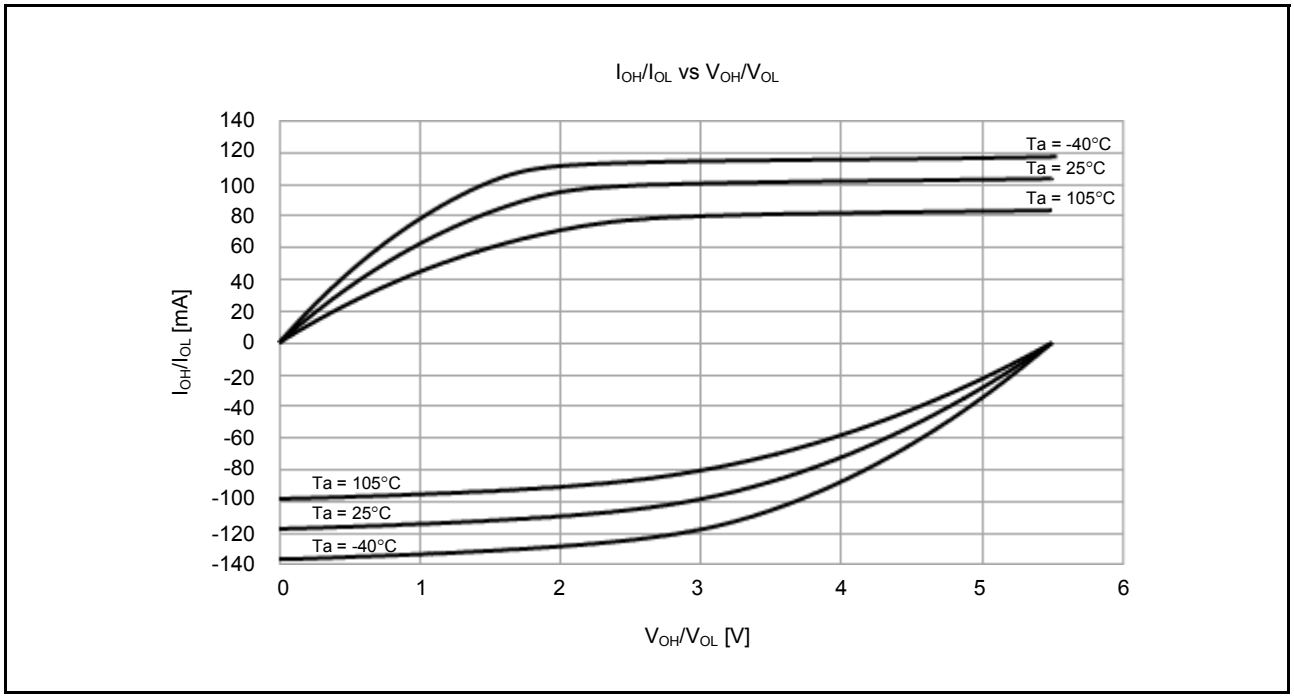


Figure 2.11 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data, except for P914 and P915)**

2.2.7 Output Characteristics for P408 and P409 I/O Pins (Middle Drive Capacity)

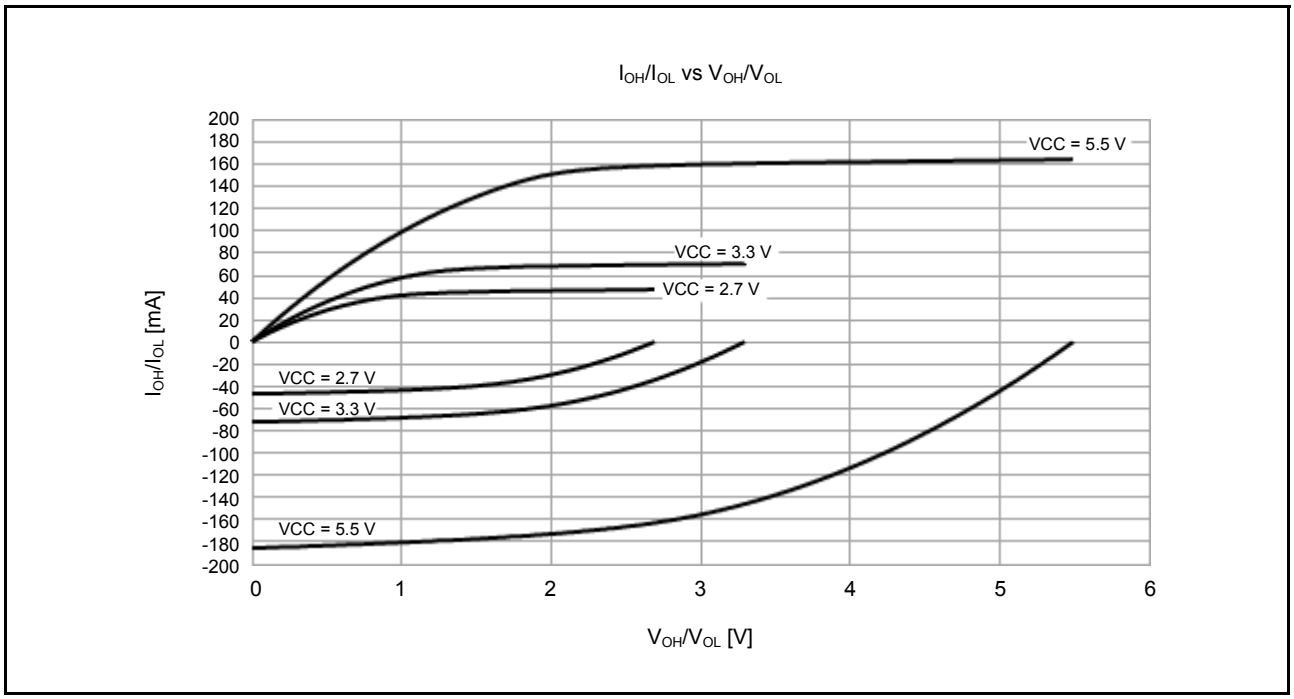


Figure 2.12 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

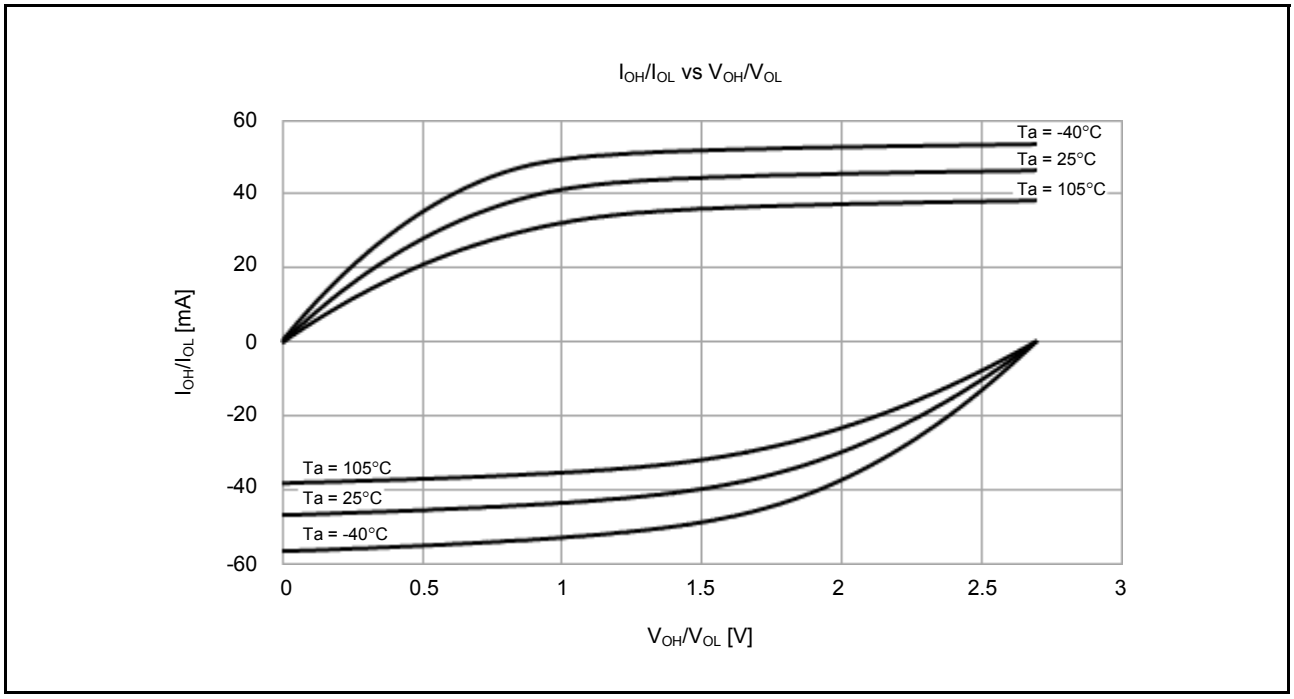


Figure 2.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)

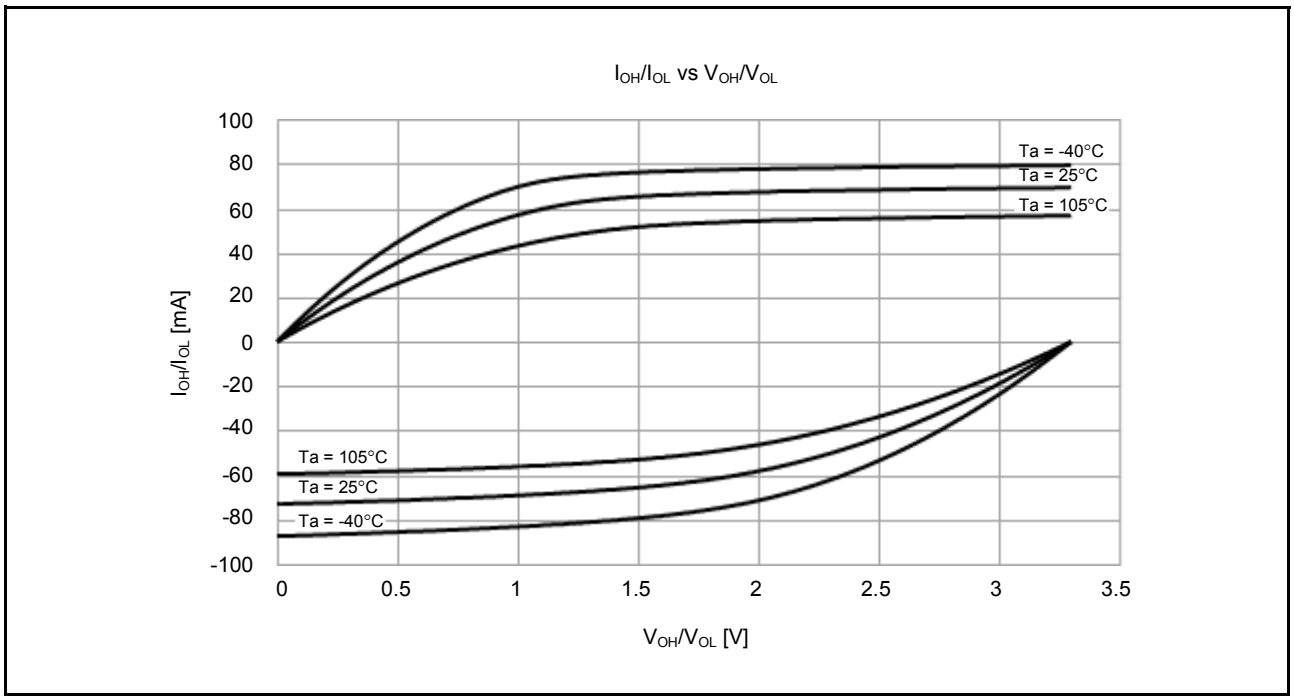
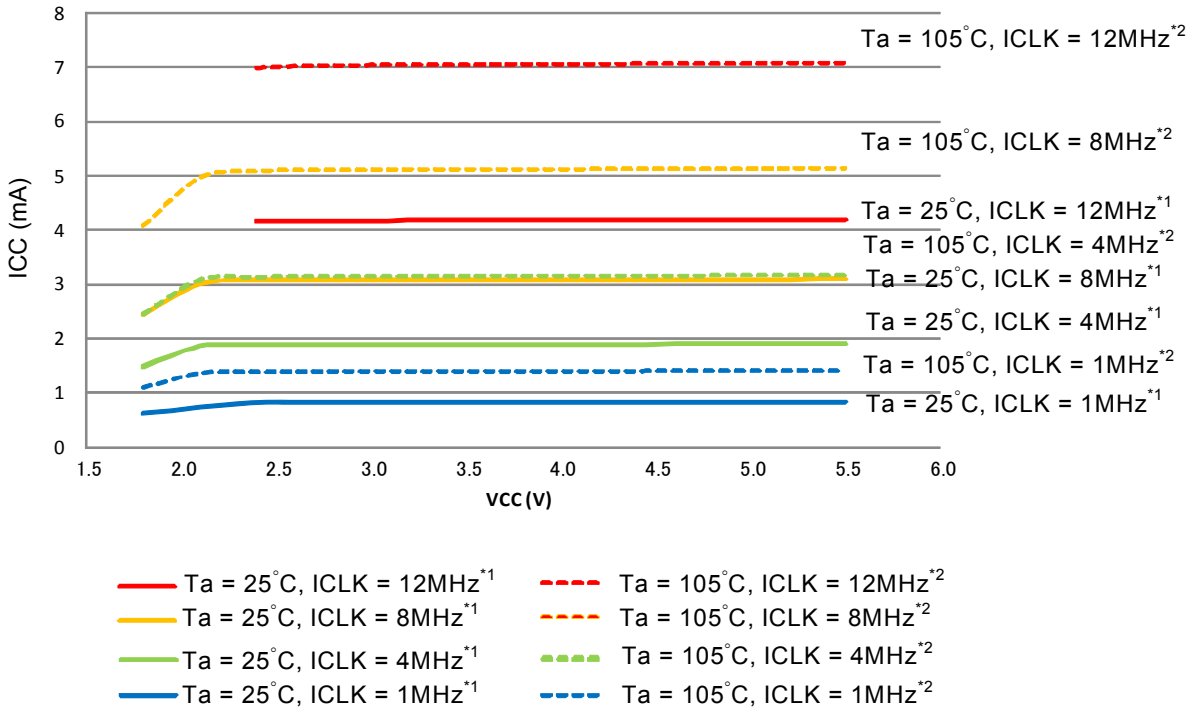


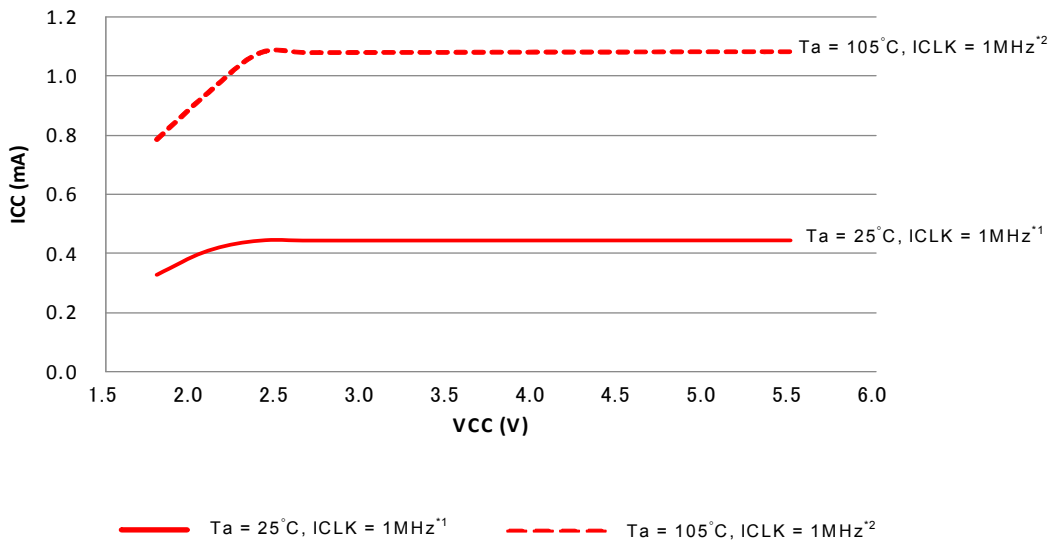
Figure 2.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.18 Voltage dependency in middle-speed mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper-limit samples during product evaluation.

Figure 2.19 Voltage dependency in low-speed mode (reference data)

2.3.2 Clock Timing

Table 2.21 Clock timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	-	-	ns	Figure 2.25
EXTAL external clock input high pulse width		t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width		t_{XL}	20	-	-	ns	
EXTAL external clock rising time		t_{Xr}	-	-	5	ns	
EXTAL external clock falling time		t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	0.3	-	-	μs	-
EXTAL external clock input frequency		f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			-	-	8		1.8 ≤ VCC < 2.4
			-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency		f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			1	-	8		1.8 ≤ VCC < 2.4
			1	-	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time		t_{LOCO}	-	-	100	μs	Figure 2.26
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time		t_{MOCO}	-	-	1	μs	-
HOCO clock oscillation frequency		f_{HOCO24}	23.64	24	24.36	MHz	Ta = –40 to –20°C 1.8 ≤ VCC ≤ 5.5
			22.68	24	25.32		Ta = –40 to –85°C 1.6 ≤ VCC < 1.8
			23.76	24	24.24		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 5.5
			23.52	24	24.48		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO32}	31.52	32	32.48		Ta = –40 to –20°C 1.8 ≤ VCC ≤ 5.5
			30.24	32	33.76		Ta = –40 to 85°C 1.6 ≤ VCC < 1.8
			31.68	32	32.32		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 5.5
			31.36	32	32.64		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO48}*3	47.28	48	48.72		Ta = –40 to –20°C 1.8 ≤ VCC ≤ 5.5
			47.52	48	48.48		Ta = –20 to 85°C 1.8 ≤ VCC ≤ 5.5
			47.04	48	48.96		Ta = –40 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO64}*4	63.04	64	64.96		Ta = –40 to –20°C 2.4 ≤ VCC ≤ 5.5
			63.36	64	64.64		Ta = –20 to 85°C 2.4 ≤ VCC ≤ 5.5
			62.72	64	65.28		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*5, *6	Except low-voltage mode	t_{HOCO24} t_{HOCO32}	-	-	37.1	μs	Figure 2.27
		t_{HOCO48}	-	-	43.3		
		t_{HOCO64}	-	-	80.6		
	Low-voltage mode	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	-	-	100.9		
Sub-clock oscillator oscillation frequency		f_{SUB}	-	32.768	-	kHz	-

2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

Table 2.30 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.35
	Input/output data cycle (P002, P003, P010, P011)		t_{POcyc}	10	-	μs	-
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 2.36
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.37
		Dual edge		2.5	-		
AGT	AGTIO, AGTEE input cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	-	ns	Figure 2.38
		2.4 V ≤ VCC < 2.7 V		500	-	ns	
		1.8 V ≤ VCC < 2.4 V		1000	-	ns	
		1.6 V ≤ VCC < 1.8 V		2000	-	ns	
	AGTIO, AGTEE input high level width, low-level width	2.7 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		2.4 V ≤ VCC < 2.7 V		200	-	ns	
		1.8 V ≤ VCC < 2.4 V		400	-	ns	
		1.6 V ≤ VCC < 1.8 V		800	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output frequency	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	-	ns	Figure 2.38
		2.4 V ≤ VCC < 2.7 V		125	-	ns	
		1.8 V ≤ VCC < 2.4 V		250	-	ns	
		1.6 V ≤ VCC < 1.8 V		500	-	ns	
ADC14	14-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.39
KINT	Key interrupt input low-level width		t_{KR}	250	-	ns	Figure 2.40

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

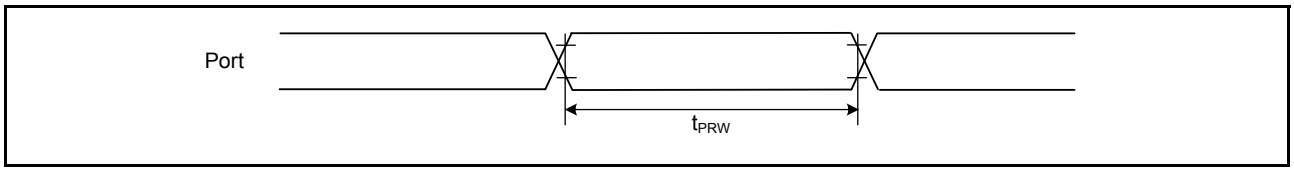


Figure 2.35 I/O ports input timing

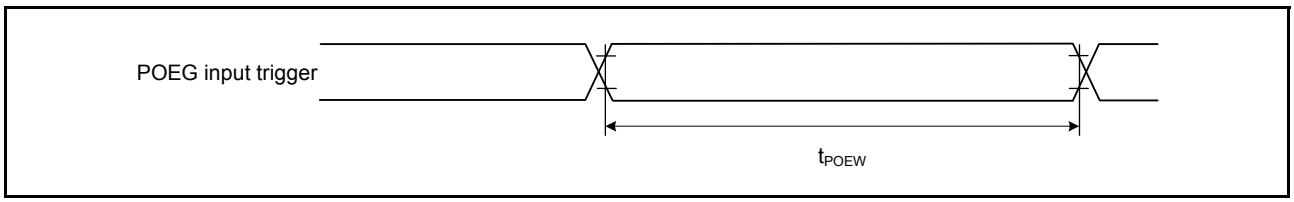


Figure 2.36 POEG input trigger timing

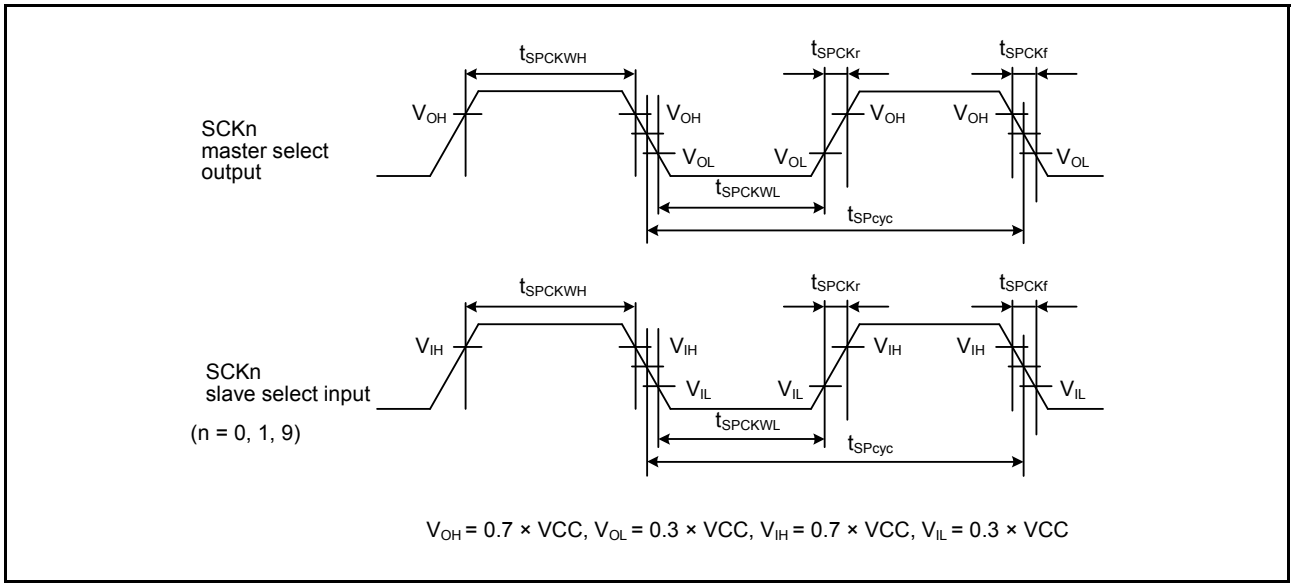


Figure 2.43 SCI simple SPI mode clock timing

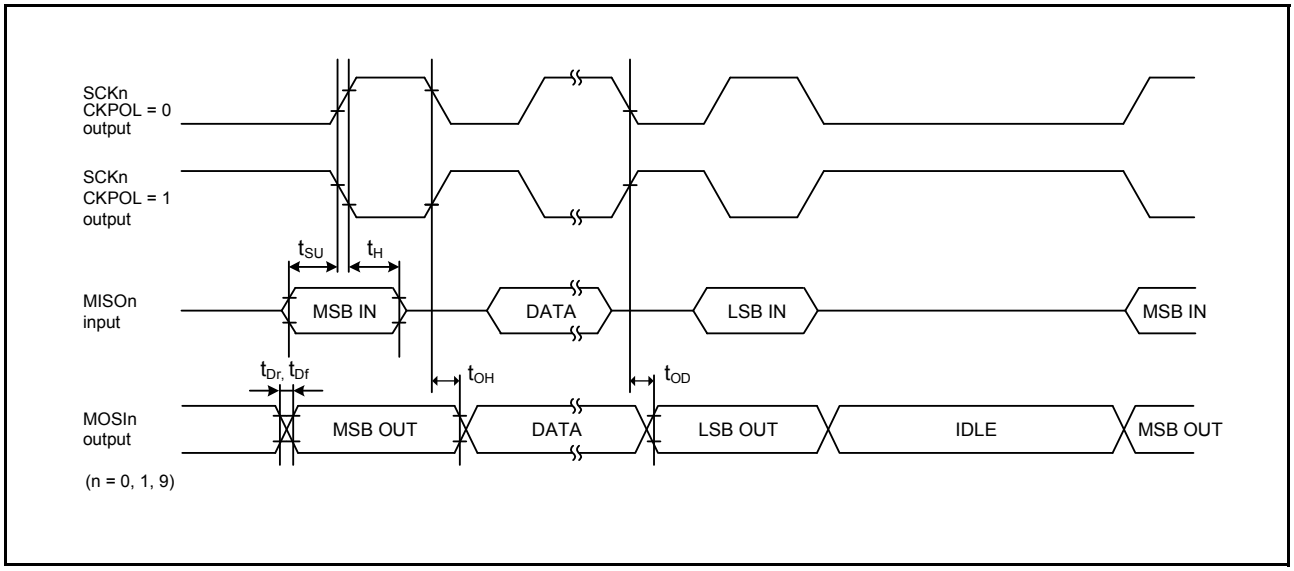


Figure 2.44 SCI simple SPI mode timing (master, CKPH = 1)

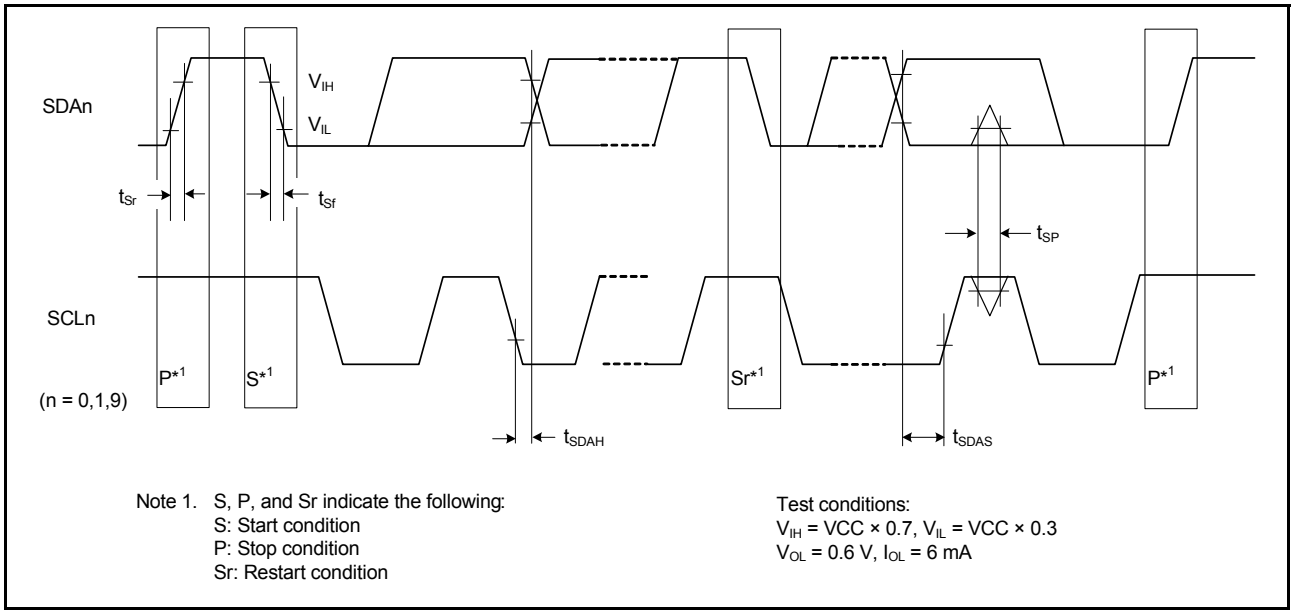


Figure 2.48 SCI simple IIC mode timing

2.3.10 SPI Timing

Table 2.36 SPI timing (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.49 C = 30pF
		Slave			6	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Output	2.7V or above	t_{SPCKr}, t_{SPCKf}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	µs	

Table 2.36 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	Data input setup time	Master		t_{SU}	10	-	ns	Figure 2.50 to Figure 2.55 C = 30pF
		Slave	2.4V or above		10	-		
			1.8V or above		15	-		
			1.6V or above		20	-		
	Data input hold time	Master (RSPCK is PCLKB/2)		t_{HF}	0	-	ns	
		Master (RSPCK is not PCLKB/2)		t_{H}	t_{Pcyc}	-		
		Slave		t_{H}	20	-		
	SSL setup time	Master		t_{LEAD}	– 30 + N x t_{Spcyc}*2	-	ns	
		Slave			6 x t_{Pcyc}	-	ns	
	SSL hold time	Master		t_{LAG}	– 30 + N x t_{Spcyc}*3	-	ns	
		Slave			6 x t_{Pcyc}	-	ns	
	Data output delay	Master	2.7V or above	t_{OD}	-	14	ns	Figure 2.50 to Figure 2.55 C = 30pF
			2.4V or above		-	20		
			1.8V or above		-	25		
			1.6V or above		-	30		
		Slave	2.7V or above		-	50		
			2.4V or above		-	60		
			1.8V or above		-	85		
			1.6V or above		-	110		
	Data output hold time	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	Successive transmission delay	Master		t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave			6 × t_{Pcyc}	-		
	MOSI and MISO rise and fall time	Output	2.7V or above	t_{Dr}, t_{Df}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	µs	
	SSL rise and fall time	Output	2.7V or above	t_{SSLr}, t_{SSLf}	-	10	ns	
			2.4V or above		-	15		
			1.8V or above		-	20		
			1.6V or above		-	30		
		Input			-	1	µs	
	Slave access time		2.4V or above	t_{SA}	-	2 × t_{Pcyc} +100	ns	Figure 2.54 and Figure 2.55 C = 30pF
			1.8V or above		-	2 × t_{Pcyc} +140		
			1.6V or above		-	2 × t_{Pcyc} +180		
	Slave output release time		2.4V or above	t_{REL}	-	2 × t_{Pcyc} +100	ns	
			1.8V or above		-	2 × t_{Pcyc} +140		
			1.6V or above		-	2 × t_{Pcyc} +180		

2.3.11 IIC Timing

Table 2.37 IIC timing
Conditions: VCC = AVCC0 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1(5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

Table 2.43 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)
Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test Conditions
Offset error	-	±2.0	±18	LSB	High-precision channel
			±24.0	LSB	Other than above
Full-scale error	-	±3.0	±18	LSB	High-precision channel
			±24.0	LSB	Other than above
Quantization error	-	±0.5	-	LSB	-
Absolute accuracy	-	±5.0	±20	LSB	High-precision channel
			±32.0	LSB	Other than above
DNL differential nonlinearity error	-	±4.0	-	LSB	-
INL integral nonlinearity error	-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Table 2.44 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V, VSS = AVSS0 = VREFL0 = 0V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test Conditions
Frequency		1	-	24	MHz	-
Analog input capacitance	Cs	-	-	15	pF	High-precision channel
		-	-	30	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5	kΩ	-
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.25	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h

2.11 Comparator Characteristics

Table 2.56 ACMPHS characteristics
Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IOCMP}	-	±5	±40	mV	-
Input voltage range	V_{ICPM}	0	-	AVCC0	V	-
Output delay time	T_d	-	50	100	ns	Input amplitude ±100 mV
Stabilization wait time during input channel switching*1	T_{WAIT}	300	-	-	ns	Input amplitude ±100 mV
Operation stabilization wait time*2	T_{cmp}	1	-	-	µs	3.3 V ≤ AVCC0 ≤ 5.5 V
		3	-	-	µs	2.7 V ≤ AVCC0 < 3.3 V

Note 1. Period from when the comparator input channel is switched until the switched result reflects in its output.
Note 2. Period from when comparator operation is enabled (CPMCTL.HCMPON = 1) until the comparator satisfies the DC/AC characteristics.

Table 2.57 ACMPLP characteristics
Conditions: VCC = AVCC0 = 1.8 to 5.5 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range	IVREF0	V_{REF}	0	-	VCC – 1.4*1	V	-
	IVREF1 (Standard mode)		0	-	VCC – 1.4	V	
	IVREF1 (Window mode)		1.4*1	-	VCC	V	
	IVCMP0, IVCMP1	V_I	0	-	VCC	V	
Internal reference voltage		-	1.36	1.44	1.50	V	-
Output delay	Comparator high-speed mode (Standard mode)	T_d	-	-	1.2	µs	VCC = 3.0 Slew rate of input signal > 50 mV/µs
	Comparator high-speed mode (Window mode)				2.0	µs	
	Comparator low-speed mode (Standard mode)				5.0	µs	
Offset voltage	Comparator high-speed mode (Standard mode)	-	-	-	50	mV	-
	Comparator high-speed mode (Window mode)				60	mV	
	Comparator low-speed mode (Standard mode)				40	mV	
Operation stabilization wait time		T_{cmp}	100	-	-	µs	-

Note 1. In window mode, be sure to satisfy the following condition: Vref1 - Vref0 ≥ 0.2 V.

2.12 OPAMP Characteristics

Table 2.58 OPAMP characteristics (1 of 2)
Conditions: 1.8 V ≤ AVCC0 = VCC ≤ 5.5 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common mode input range	V_{icm1}	Low-power mode	0.1	-	AVCC0 – 0.5	V
	V_{icm2}	High-speed mode	0.2	-	AVCC0 – 0.6	
Output voltage range	V_{o1}	Low-power mode	0.1	-	AVCC0 – 0.1	V
	V_{o2}	High-speed mode	0.1	-	AVCC0 – 0.1	
Input offset voltage	V_{ioff1}	Low-power mode	–7	-	7	mV
	V_{ioff2}	High-speed mode	–5	-	5	

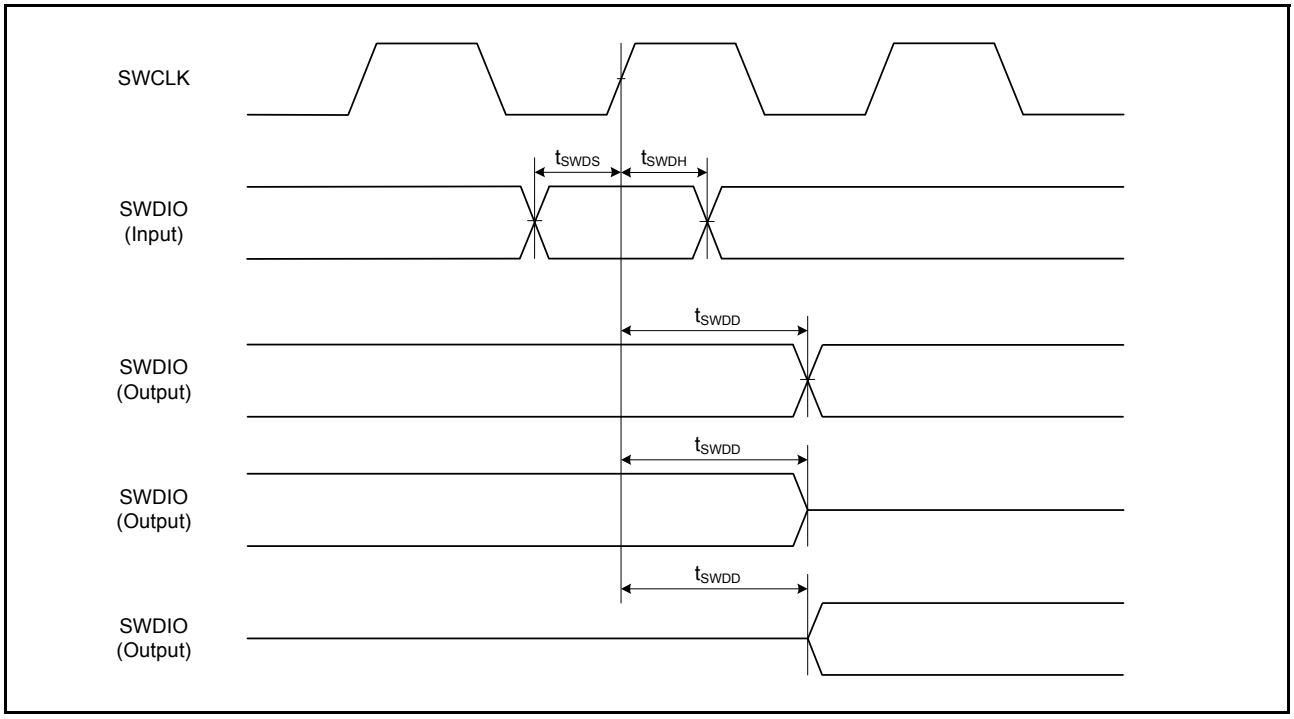


Figure 2.70 SWD input/output timing