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**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 516096 |
| Number of I/O | 620 |
| Number of Gates | 3000000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 896-BGA |
| Supplier Device Package | 896-FBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3pe3000l-1fg896i |

# Low Power Modes Overview

Table 2-2 summarizes the low power modes that achieve power consumption reduction when the FPGA or system is idle.

***Table 2-2 •*** Power Modes Summary

| Mode | | VCCI | VCC | Core | Clocks | ULSICC Macro | To Enter Mode | To Resume Operation | Trigger |
|---|---|---|---|---|---|---|---|---|---|
| Active | | On | On | On | On | N/A | Initiate clock | None | – |
| Static | Idle | On | On | On | Off | N/A | Stop clock | Initiate clock | External |
| | Flash*Freeze type 1 | On | On | On | On* | N/A | Assert FF pin | Deassert FF pin | External |
| | Flash*Freeze type 2 | On | On | On | On* | Used to enter Flash*Freeze mode | Assert FF pin and assert LSICC | Deassert FF pin | External |
| Sleep | | On | Off | Off | Off | N/A | Shut down VCC | Turn on VCC supply | External |
| Shutdown | | Off | Off | Off | Off | N/A | Shut down VCC and VCCI supplies | Turn on VCC and VCCI supplies | External |

\* External clocks can be left toggling while the device is in Flash*Freeze mode. Clocks generated by the embedded PLL will be turned off automatically.

# Static (Idle) Mode

In Static (Idle) mode, none of the clock inputs is switching, and static power is the only power consumed by the device. This mode can be achieved by switching off the incoming clocks to the FPGA, thus benefitting from reduced power consumption. In addition, I/Os draw only minimal leakage current. In this mode, embedded SRAM, I/Os, and registers retain their values so the device can enter and exit this mode just by switching the clocks on or off.

If the device-embedded PLL is used as the clock source, Static (Idle) mode can easily be entered by pulling the PLL POWERDOWN pin LOW (active Low), which will turn off the PLL.

***Table 3-3 •*** Quadrant Global Pin Name

| I/O Type | Beginning of I/O Name | Notes |
|---|---|---|
| Single-Ended | GAAO/IOuxwByVz<br>GAA1/IOuxwByVz<br>GAA2/IOuxwByVz | Only one of the I/Os can be directly connected to a quadrant global at a time |
| | GABO/IOuxwByVz<br>GAB1/IOuxwByVz<br>GAB2/IOuxwByVz | Only one of the I/Os can be directly connected to a quadrant global at a time. |
| | GAC0/IOuxwByVz<br>GAC1/IOuxwByVz<br>GAC2/IOuxwByVz | Only one of the I/Os can be directly connected to a quadrant global at a time. |
| | GBAO/IOuxwByVz<br>GBA1/IOuxwByVz<br>GBA2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GBBO/IOuxwByVz<br>GBB1/IOuxwByVz<br>GBB2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GBC0/IOuxwByVz<br>GBC1/IOuxwByVz<br>GBC2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GDAO/IOuxwByVz<br>GDA1/IOuxwByVz<br>GDA2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GDBO/IOuxwByVz<br>GDB1/IOuxwByVz<br>GDB2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GDC0/IOuxwByVz<br>GDC1/IOuxwByVz<br>GDC2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GEAO/IOuxwByVz<br>GEA1/IOuxwByVz<br>GEA2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GEBO/IOuxwByVz<br>GEB1/IOuxwByVz<br>GEB2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |
| | GEC0/IOuxwByVz<br>GEC1/IOuxwByVz<br>GEC2/IOuxwByVz | Only one of the I/Os can be directly connected to a global at a time. |

Note: Only one of the I/Os can be directly connected to a quadrant at a time.

### *External I/O or Local signal as Clock Source*

External I/O refers to regular I/O pins are labeled with the I/O convention IOuxwByVz. You can allow the external I/O or internal signal to access the global. To allow the external I/O or internal signal to access the global network, you need to instantiate the CLKINT macro. Refer to Figure 3-4 on page 51 for an example illustration of the connections. Instead of using CLKINT, you can also use PDC to promote signals from external I/O or internal signal to the global network. However, it may cause layout issues because of synthesis logic replication. Refer to the "Global Promotion and Demotion Using PDC" section on page 67 for details.
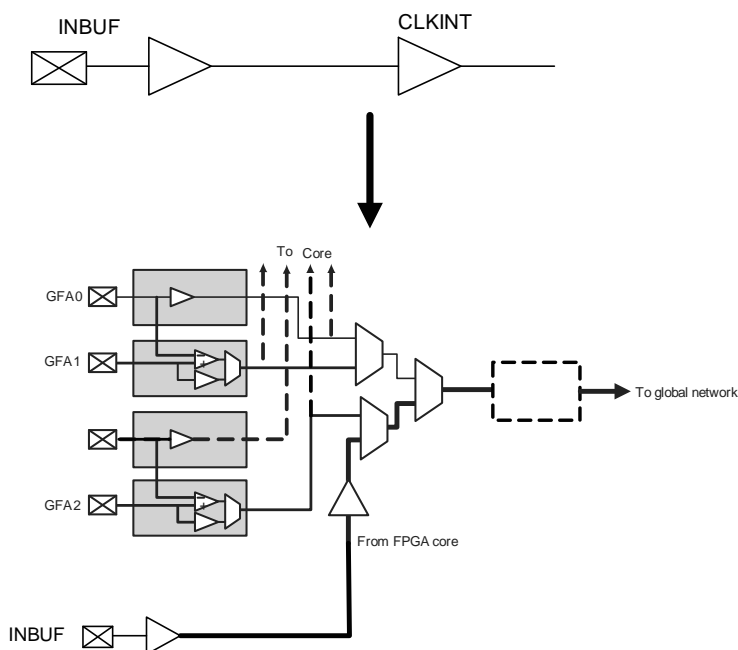


***Figure 3-14 •*** CLKINT Macro

## Using Global Macros in Synplicity

The Synplify® synthesis tool automatically inserts global buffers for nets with high fanout during synthesis. By default, Synplicity® puts six global macros (CLKBUF or CLKINT) in the netlist, including any global instantiation or PLL macro. Synplify always honors your global macro instantiation. If you have a PLL (only primary output is used) in the design, Synplify adds five more global buffers in the netlist. Synplify uses the following global counting rule to add global macros in the netlist:

1. CLKBUF: 1 global buffer
2. CLKINT: 1 global buffer
3. CLKDLY: 1 global buffer
4. PLL: 1 to 3 global buffers
   – GLA, GLB, GLC, YB, and YC are counted as 1 buffer.
   – GLB or YB is used or both are counted as 1 buffer.
   – GLC or YC is used or both are counted as 1 buffer.

## Simple Design Example

Consider a design consisting of six building blocks (shift registers) and targeted for an A3PE600-PQ208 (Figure 3-16 on page 68). The example design consists of two PLLs (PLL1 has GLA only; PLL2 has both GLA and GLB), a global reset (ACLR), an enable (EN_ALL), and three external clock domains (QCLK1, QCLK2, and QCLK3) driving the different blocks of the design. Note that the PQ208 package only has two PLLs (which access the chip global network). Because of fanout, the global reset and enable signals need to be assigned to the chip global resources. There is only one free chip global for the remaining global (QCLK1, QCLK2, QCLK3). Place two of these signals on the quadrant global resource. The design example demonstrates manually assignment of QCLK1 and QCLK2 to the quadrant global using the PDC command.
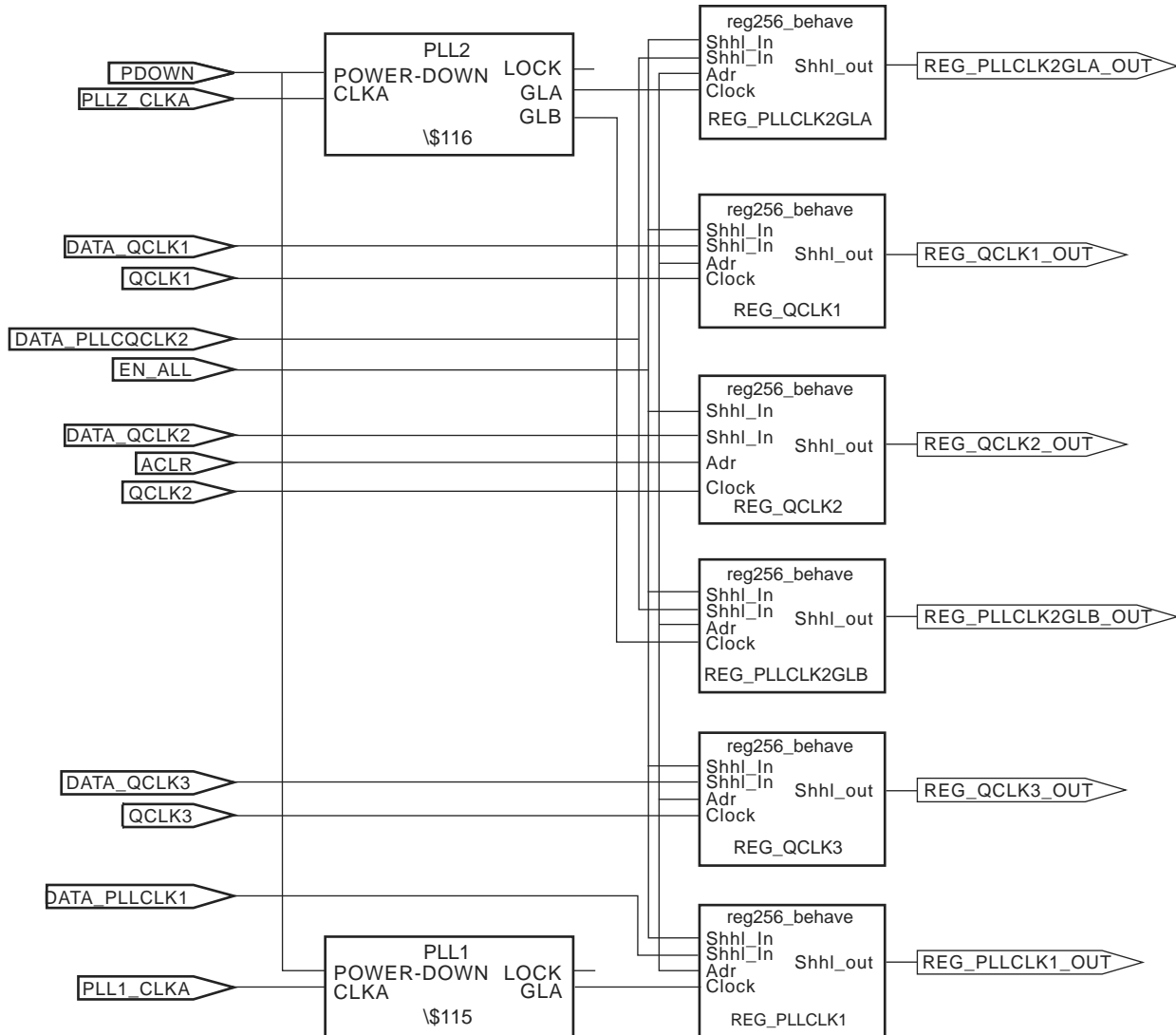


***Figure 3-19 •*** Block Diagram of the Global    Management Example Design

## CLKDLY Macro Usage

When a CLKDLY macro is used in a CCC location, the programmable delay element is used to allow the clock delays to go to the global network. In addition, the user can bypass the PLL in a CCC location integrated with a PLL, but use the programmable delay that is associated with the global network by instantiating the CLKDLY macro. The same is true when using programmable delay elements in a CCC location with no PLLs (the user needs to instantiate the CLKDLY macro). There is no difference between the programmable delay elements used for the PLL and the CLKDLY macro. The CCC will be configured to use the programmable delay elements in accordance with the macro instantiated by the user.

As an example, if the PLL is not used in a particular CCC location, the designer is free to specify up to three CLKDLY macros in the CCC, each of which can have its own input frequency and delay adjustment options. If the PLL core is used, assuming output to only one global clock network, the other two global clock networks are free to be used by either connecting directly from the global inputs or connecting from one or two CLKDLY macros for programmable delay.

The programmable delay elements are shown in the block diagram of the PLL block shown in Figure 4-6 on page 87. Note that any CCC locations with no PLL present contain only the programmable delay blocks going to the global networks (labeled "Programmable Delay Type 2"). Refer to the "Clock Delay Adjustment" section on page 102 for a description of the programmable delay types used for the PLL. Also refer to Table 4-14 on page 110 for Programmable Delay Type 1 step delay values, and Table 4-15 on page 110 for Programmable Delay Type 2 step delay values. CCC locations with a PLL present can be configured to utilize only the programmable delay blocks (Programmable Delay Type 2) going to the global networks A, B, and C.

Global network A can be configured to use only the programmable delay element (bypassing the PLL) if the PLL is not used in the design. Figure 4-6 on page 87 shows a block diagram of the PLL, where the programmable delay elements are used for the global networks (Programmable Delay Type 2).

## *Core Logic Clock Source*

Core logic refers to internal routed nets. Internal routed signals access the CCC via the FPGA Core Fabric. Similar to the External I/O option, whenever the clock source comes internally from the core itself, the routed signal is instantiated with a PLLINT macro before connecting to the CCC clock input (see Figure 4-12 for an example illustration of the connections, shown in red).



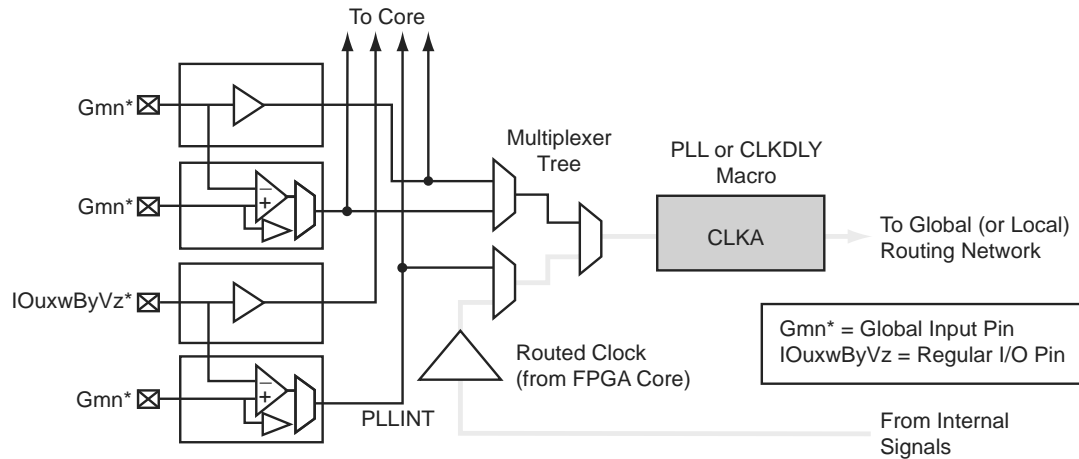*Figure 4-12 •* Illustration of Core Logic Usage

For Fusion devices, the input reference clock can also be from the embedded RC oscillator and crystal oscillator. In this case, the CCC configuration is the same as the hardwired I/O clock source, and users are required to instantiate the RC oscillator or crystal oscillator macro and connect its output to the input reference clock of the CCC block.

# PLL Core Specifications

PLL core specifications can be found in the DC and Switching Characteristics chapter of the appropriate family datasheet.

## Loop Bandwidth

Common design practice for systems with a low-noise input clock is to have PLLs with small loop bandwidths to reduce the effects of noise sources at the output. Table 4-6 shows the PLL loop bandwidth, providing a measure of the PLL's ability to track the input clock and jitter.

*Table 4-6 •* –3 dB Frequency of the PLL

|  | Minimum<br>($T_a$ = +125°C, VCCA = 1.4 V) | Typical<br>($T_a$ = +25°C, VCCA = 1.5 V) | Maximum<br>($T_a$ = −55°C, VCCA = 1.6 V) |
|---|---|---|---|
| −3 dB Frequency | 15 kHz | 25 kHz | 45 kHz |

## PLL Core Operating Principles

This section briefly describes the basic principles of PLL operation. The PLL core is composed of a phase detector (PD), a low-pass filter (LPF), and a four-phase voltage-controlled oscillator (VCO). Figure 4-19 illustrates a basic single-phase PLL core with a divider and delay in the feedback path.
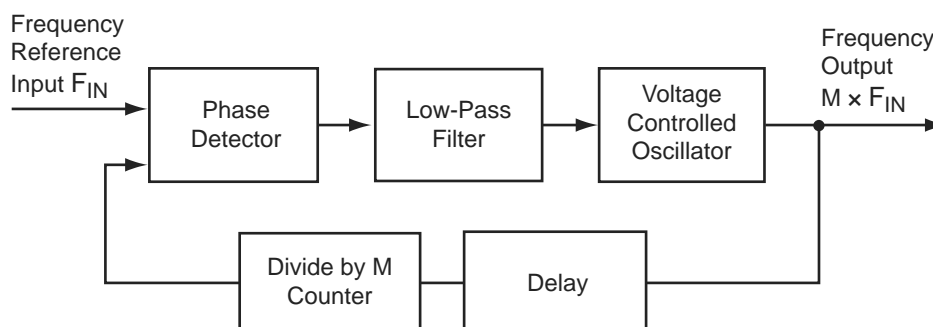


*Figure 4-19 •* Simplified PLL Core with Feedback Divider and Delay

The PLL is an electronic servo loop that phase-aligns the PD feedback signal with the reference input. To achieve this, the PLL dynamically adjusts the VCO output signal according to the average phase difference between the input and feedback signals.

The first element is the PD, which produces a voltage proportional to the phase difference between its inputs. A simple example of a digital phase detector is an Exclusive-OR gate. The second element, the LPF, extracts the average voltage from the phase detector and applies it to the VCO. This applied voltage alters the resonant frequency of the VCO, thus adjusting its output frequency.

Consider Figure 4-19 with the feedback path bypassing the divider and delay elements. If the LPF steadily applies a voltage to the VCO such that the output frequency is identical to the input frequency, this steady-state condition is known as lock. Note that the input and output phases are also identical. The PLL core sets a LOCK output signal HIGH to indicate this condition.

Should the input frequency increase slightly, the PD detects the frequency/phase difference between its reference and feedback input signals. Since the PD output is proportional to the phase difference, the change causes the output from the LPF to increase. This voltage change increases the resonant frequency of the VCO and increases the feedback frequency as a result. The PLL dynamically adjusts in this manner until the PD senses two phase-identical signals and steady-state lock is achieved. The opposite (decreasing PD output signal) occurs when the input frequency decreases.

Now suppose the feedback divider is inserted in the feedback path. As the division factor M (shown in Figure 4-20 on page 101) is increased, the average phase difference increases. The average phase

### External Feedback Configuration

For certain applications, such as those requiring generation of PCB clocks that must be matched with existing board delays, it is useful to implement an external feedback, EXTFB. The Phase Detector of the PLL core will receive CLKA and EXTFB as inputs. EXTFB may be processed by the fixed System Delay element as well as the M divider element. The EXTFB option is currently not supported.

After setting all the required parameters, users can generate one or more PLL configurations with HDL or EDIF descriptions by clicking the Generate button. SmartGen gives the option of saving session results and messages in a log file:

```
****************
Macro Parameters
****************

Name                          : test_pll
Family                        : ProASIC3E
Output Format                 : VHDL
Type                          : Static PLL
Input Freq(MHz)               : 10.000
CLKA Source                   : Hardwired I/O
Feedback Delay Value Index    : 1
Feedback Mux Select           : 2
XDLY Mux Select               : No
Primary Freq(MHz)             : 33.000
Primary PhaseShift            : 0
Primary Delay Value Index     : 1
Primary Mux Select            : 4
Secondary1 Freq(MHz)          : 66.000
Use GLB                       : YES
Use YB                        : YES
GLB Delay Value Index         : 1
YB Delay Value Index          : 1
Secondary1 PhaseShift         : 0
Secondary1 Mux Select         : 4
Secondary2 Freq(MHz)          : 101.000
Use GLC                       : YES
Use YC                        : NO
GLC Delay Value Index         : 1
YC Delay Value Index          : 1
Secondary2 PhaseShift         : 0
Secondary2 Mux Select         : 4

…
…
…

Primary Clock frequency 33.333
Primary Clock Phase Shift 0.000
Primary Clock Output Delay from CLKA 0.180

Secondary1 Clock frequency 66.667
Secondary1 Clock Phase Shift 0.000
Secondary1 Clock Global Output Delay from CLKA 0.180
Secondary1 Clock Core Output Delay from CLKA 0.625

Secondary2 Clock frequency 100.000
Secondary2 Clock Phase Shift 0.000
Secondary2 Clock Global Output Delay from CLKA 0.180
```

Below is an example Verilog HDL description of a legal PLL core configuration generated by SmartGen:

```
module test_pll(POWERDOWN,CLKA,LOCK,GLA);
input POWERDOWN, CLKA;
output  LOCK, GLA;
```

# FlashROM Security

Low power flash devices have an on-chip Advanced Encryption Standard (AES) decryption core, combined with an enhanced version of the Microsemi flash-based lock technology (FlashLock®). Together, they provide unmatched levels of security in a programmable logic device. This security applies to both the FPGA core and FlashROM content. These devices use the 128-bit AES (Rijndael) algorithm to encrypt programming files for secure transmission to the on-chip AES decryption core. The same algorithm is then used to decrypt the programming file. This key size provides approximately $3.4 \times 10^{38}$ possible 128-bit keys. A computing system that could find a DES key in a second would take approximately 149 trillion years to crack a 128-bit AES key. The 128-bit FlashLock feature in low power flash devices works via a FlashLock security Pass Key mechanism, where the user locks or unlocks the device with a user-defined key. Refer to the "Security in Low Power Flash Devices" section on page 301.

If the device is locked with certain security settings, functions such as device read, write, and erase are disabled. This unique feature helps to protect against invasive and noninvasive attacks. Without the correct Pass Key, access to the FPGA is denied. To gain access to the FPGA, the device first must be unlocked using the correct Pass Key. During programming of the FlashROM or the FPGA core, you can generate the security header programming file, which is used to program the AES key and/or FlashLock Pass Key. The security header programming file can also be generated independently of the FlashROM and FPGA core content. The FlashLock Pass Key is not stored in the FlashROM.

Low power flash devices with AES-based security allow for secure remote field updates over public networks such as the Internet, and ensure that valuable intellectual property (IP) remains out of the hands of IP thieves. Figure 5-5 shows this flow diagram.
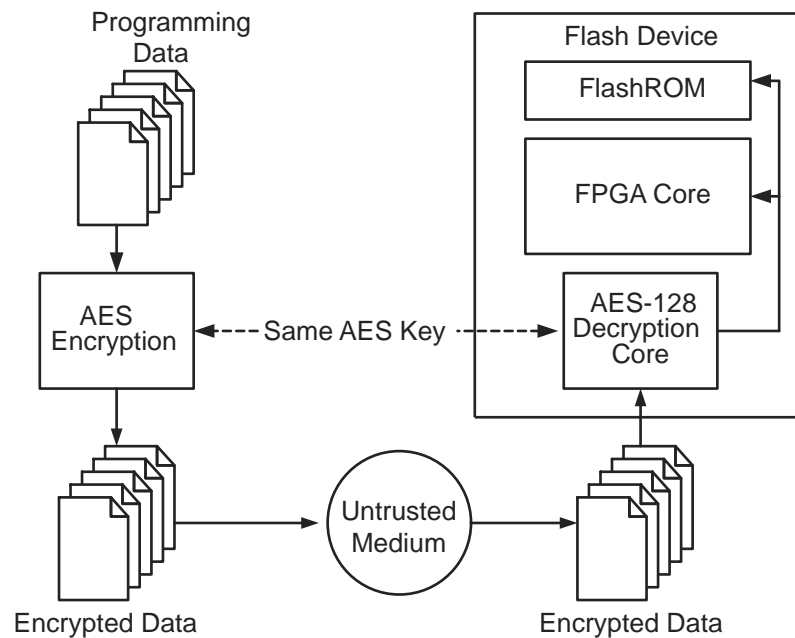


***Figure 5-5 •*** Programming FlashROM Using AES

- In Active and Static modes:
    - Input buffers with pull-up, driven Low
    - Input buffers with pull-down, driven High
    - Bidirectional buffers with pull-up, driven Low
    - Bidirectional buffers with pull-down, driven High
    - Output buffers with pull-up, driven Low
    - Output buffers with pull-down, driven High
    - Tristate buffers with pull-up, driven Low
    - Tristate buffers with pull-down, driven High
- In Flash*Freeze mode:
    - Input buffers with pull-up, driven Low
    - Input buffers with pull-down, driven High
    - Bidirectional buffers with pull-up, driven Low
    - Bidirectional buffers with pull-down, driven High

## Electrostatic Discharge Protection

Low power flash devices are tested per JEDEC Standard JESD22-A114-B.

These devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

All IGLOO and ProASIC3 devices are tested to the Human Body Model (HBM) and the Charged Device Model (CDM).

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to VCCI. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the off state, except when transient voltage is significantly above VCCI or below GND levels.

In 30K gate devices, the first diode is always off. In other devices, the clamp diode is always on and cannot be switched off.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 7-12 on page 193 for more information about the I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

***Table 7-13 •*** Comparison Table for 5 V–Compliant Receiver Solutions

| Solution | Board Components | Speed | Current Limitations |
|---|---|---|---|
| 1 | Two resistors | Low to High[1] | Limited by transmitter's drive strength |
| 2 | Resistor and Zener 3.3 V | Medium | Limited by transmitter's drive strength |
| 3 | Bus switch | High | N/A |
| 4 | Minimum resistor value[2,3,4,5]<br>R = 47 : at $T_J$ = 70°C<br>R = 150 : at $T_J$ = 85°C<br>R = 420 : at $T_J$ = 100°C | Medium | Maximum diode current at 100% duty cycle, signal constantly at 1<br>52.7 mA at $T_J$ = 70°C / 10-year lifetime<br>16.5 mA at $T_J$ = 85°C / 10-year lifetime<br>5.9 mA at $T_J$ = 100°C / 10-year lifetime<br>For duty cycles other than 100%, the currents can be increased by a factor of 1 / (duty cycle).<br>Example: 20% duty cycle at 70°C<br>Maximum current = (1 / 0.2) × 52.7 mA = 5 × 52.7 mA = 263.5 mA |

Notes:

1. Speed and current consumption increase as the board resistance values decrease.

2. Resistor values ensure I/O diode long-term reliability.

3. At 70°C, customers could still use 420 : on every I/O.

4. At 85°C, a 5 V solution on every other I/O is permitted, since the resistance is lower (150 :) and the current is higher. Also, the designer can still use 420 : and use the solution on every I/O.

5. At 100°C, the 5 V solution on every I/O is permitted, since 420 : are used to limit the current to 5.9 mA.

### 5 V Output Tolerance

IGLOO and ProASIC3 I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, the I/Os can directly drive signals into 5 V TTL receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceeds the VIL = 0.8 V and VIH = 2 V level requirements of 5 V TTL receivers. Therefore, level 1 and level 0 will be recognized correctly by 5 V TTL receivers.

## Schmitt Trigger

A Schmitt trigger is a buffer used to convert a slow or noisy input signal into a clean one before passing it to the FPGA. Using Schmitt trigger buffers guarantees a fast, noise-free input signal to the FPGA.

The Schmitt trigger is available for the LVTTL, LVCMOS, and 3.3 V PCI I/O standards.

This feature can be implemented by using a Physical Design Constraints (PDC) command (Table 7-5 on page 179) or by selecting a check box in the I/O Attribute Editor in Designer. The check box is cleared by default.

# Board-Level Considerations

Low power flash devices have robust I/O features that can help in reducing board-level components. The devices offer single-chip solutions, which makes the board layout simpler and more immune to signal integrity issues. Although, in many cases, these devices resolve board-level issues, special attention should always be given to overall signal integrity. This section covers important board-level considerations to facilitate optimum device performance.

## Termination

Proper termination of all signals is essential for good signal quality. Nonterminated signals, especially clock signals, can cause malfunctioning of the device.

For general termination guidelines, refer to the Board-Level Considerations application note for Microsemi FPGAs. Also refer to the "Pin Descriptions" chapter of the appropriate datasheet for termination requirements for specific pins.

Low power flash I/Os are equipped with on-chip pull-up/-down resistors. The user can enable these resistors by instantiating them either in the top level of the design (refer to the IGLOO, Fusion, and ProASIC3 Macro Library Guide for the available I/O macros with pull-up/-down) or in the I/O Attribute Editor in Designer if generic input or output buffers are instantiated in the top level. Unused I/O pins are configured as inputs with pull-up resistors.

As mentioned earlier, low power flash devices have multiple programmable drive strengths, and the user can eliminate unwanted overshoot and undershoot by adjusting the drive strengths.

## Power-Up Behavior

Low power flash devices are power-up/-down friendly; i.e., no particular sequencing is required for power-up and power-down. This eliminates extra board components for power-up sequencing, such as a power-up sequencer.

During power-up, all I/Os are tristated, irrespective of I/O macro type (input buffers, output buffers, I/O buffers with weak pull-ups or weak pull-downs, etc.). Once I/Os become activated, they are set to the user-selected I/O macros. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" section on page 373 for details.

## Drive Strength

Low power flash devices have up to seven programmable output drive strengths. The user can select the drive strength of a particular output in the I/O Attribute Editor or can instantiate a specialized I/O macro, such as OUTBUF_S_12 (slew = low, out_drive = 12 mA).

The maximum available drive strength is 24 mA per I/O. Though no I/O should be forced to source or sink more than 24 mA indefinitely, I/Os may handle a higher amount of current (refer to the device IBIS model for maximum source/sink current) during signal transition (AC current). Every device package has its own power dissipation limit; hence, power calculation must be performed accurately to determine how much current can be tolerated per I/O within that limit.

## I/O Interfacing

Low power flash devices are 5 V–input– and 5 V–output–tolerant if certain I/O standards are selected (refer to the "5 V Input and Output Tolerance" section on page 194). Along with other low-voltage I/O macros, this 5 V tolerance makes these devices suitable for many types of board component interfacing.

| Date | Change | Page |
|------|--------|------|
| June 2011 (continued) | The following sentence was removed from the "LVCMOS (Low-Voltage CMOS)" section (SAR 22634): "All these versions use a 3.3 V–tolerant CMOS input buffer and a push-pull output buffer." | 184 |
| | Hot-insertion was changed to "No" for other IGLOO and all ProASIC3 devices in Table 7-12 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in IGLOO and ProASIC3 Devices (SAR 24526). | 193 |
| | The "Electrostatic Discharge Protection" section was revised to remove references to tolerances (refer to the Reliability Report for tolerances). The Machine Model (MM) is not supported and was deleted from this section (SAR 24385). | 192 |
| | The "I/O Interfacing" section was revised to state that low power flash devices are 5 V–input– and 5 V–output–tolerant if certain I/O standards are selected, removing "without adding any extra circuitry," which was incorrect (SAR 21404). | 208 |
| July 2010 | This chapter is no longer published separately with its own part number and version but is now part of several FPGA fabric user's guides. | N/A |
| v1.4 (December 2008) | The terminology in the "Low Power Flash Device I/O Support" section was revised. | 176 |
| v1.3 (October 2008) | The "Low Power Flash Device I/O Support" section was revised to include new families and make the information more concise. | 176 |
| v1.2 (June 2008) | The following changes were made to the family descriptions in Table 7-1 • Flash-Based FPGAs:<br>• ProASIC3L was updated to include 1.5 V.<br>• The number of PLLs for ProASIC3E was changed from five to six. | 176 |
| v1.1 (March 2008) | Originally, this document contained information on all IGLOO and ProASIC3 families. With the addition of new families and to highlight the differences between the features, the document has been separated into 3 documents:<br>This document contains information specific to IGLOO, ProASIC3, and ProASIC3L.<br>"I/O Structures in IGLOOe and ProASIC3E Devices" in the ProASIC3E FPGA Fabric User's Guide contains information specific to IGLOOe, ProASIC3E, and ProASIC3EL I/O features.<br>"I/O Structures in IGLOO PLUS Devices" in the IGLOO PLUS FPGA Fabric User's Guide contains information specific to IGLOO PLUS I/O features. | N/A |

*Table 8-9* • Hot-Swap Level 1

| Description | Cold-swap |
|---|---|
| Power Applied to Device | No |
| Bus State | – |
| Card Ground Connection | – |
| Device Circuitry Connected to Bus Pins | – |
| Example Application | System and card with Microsemi FPGA chip are powered down, and the card is plugged into the system. Then the power supplies are turned on for the system but not for the FPGA on the card. |
| Compliance of IGLOO and ProASIC3 Devices | 30 k gate devices: Compliant<br>Other IGLOO/ProASIC3 devices: Compliant if bus switch used to isolate FPGA I/Os from rest of system<br>IGLOOe/ProASIC3E devices: Compliant I/Os can, but do not have to be set to hot-insertion mode. |

*Table 8-10* • Hot-Swap Level 2

| Description | Hot-swap while reset |
|---|---|
| Power Applied to Device | Yes |
| Bus State | Held in reset state |
| Card Ground Connection | Reset must be maintained for 1 ms before, during, and after insertion/removal. |
| Device Circuitry Connected to Bus Pins | – |
| Example Application | In the PCI hot-plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable. |
| Compliance of IGLOO and ProASIC3 Devices | 30 k gate devices, all IGLOOe/ProASIC3E devices: Compliant I/Os can but do not have to be set to hot-insertion mode.<br>Other IGLOO/ProASIC3 devices: Compliant |

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed the voltage overshoot/undershoot limits provided in the datasheet. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 8-12. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.
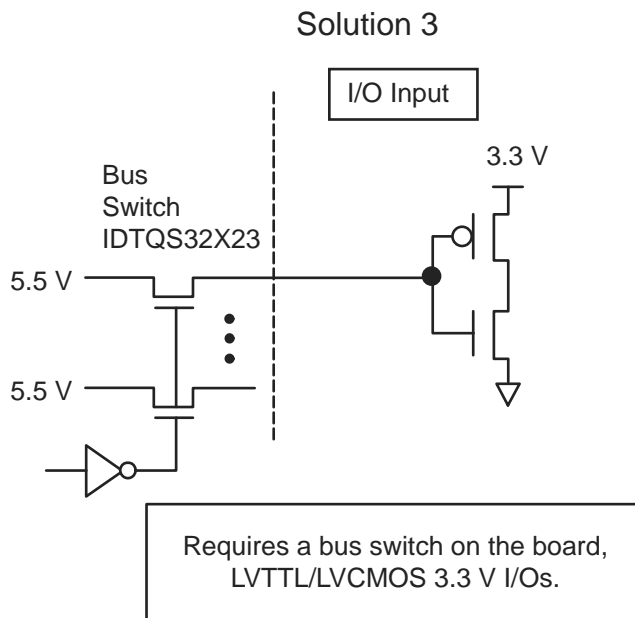


*Figure 8-12* • Solution 3

# Programming Voltage (VPUMP) and VJTAG

Low-power flash devices support on-chip charge pumps, and therefore require only a single 3.3 V programming voltage for the VPUMP pin during programming. When the device is not being programmed, the VPUMP pin can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V[2]. During programming, the target board or the FlashPro4/3/3X programmer can provide VPUMP. FlashPro4/3/3X is capable of supplying VPUMP to a single device. If more than one device is to be programmed using FlashPro4/3/3X on a given board, FlashPro4/3/3X should not be relied on to supply the VPUMP voltage. A FlashPro4/3/3X programmer is not capable of providing reliable VJTAG voltage. The board must supply VJTAG voltage to the device and the VJTAG pin of the programmer header must be connected to the device VJTAG pin. Microsemi recommends that VPUMP[3] and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail. Refer to the "Board-Level Considerations" section on page 337 for capacitor requirements.

Low power flash device I/Os support a bank-based, voltage-supply architecture that simultaneously supports multiple I/O voltage standards (Table 13-2). By isolating the JTAG power supply in a separate bank from the user I/Os, low power flash devices provide greater flexibility with supply selection and simplify power supply and printed circuit board (PCB) design. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Microsemi recommends that TCK be tied to GND through a 200 ohm to 1 Kohm resistor. This prevents a possible totempole current on the input buffer stage. For TDI, TMS, and TRST pins, the devices provide an internal nominal 10 Kohm pull-up resistor. During programming, all I/O pins, except for JTAG interface pins, are tristated and weakly pulled up to VCCI. This isolates the part and prevents the signals from floating. The JTAG interface pins are driven by the FlashPro4/3/3X during programming, including the TRST pin, which is driven HIGH.

*Table 13-2 •* Power Supplies

| Power Supply | Programming Mode | Current during Programming |
|---|---|---|
| VCC | 1.2 V / 1.5 V | < 70 mA |
| VCCI | 1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V (bank-selectable) | I/Os are weakly pulled up. |
| VJTAG | 1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V | < 20 mA |
| VPUMP | 3.15 V to 3.45 V | < 80 mA |

Note: All supply voltages should be at 1.5 V or higher, regardless of the setting during normal operation, except for IGLOO nano, where 1.2 V VCC and VJTAG programming is allowed.

# Nonvolatile Memory (NVM) Programming Voltage

SmartFusion and Fusion devices need stable VCCNVM/VCCENVM[3] (1.5 V power supply to the embedded nonvolatile memory blocks) and VCCOSC/VCCROSC[4] (3.3 V power supply to the integrated RC oscillator). The tolerance of VCCNVM/VCCENVM is ± 5% and VCCOSC/VCCROSC is ± 5%.

Unstable supply voltage on these pins can cause an NVM programming failure due to NVM page corruption. The NVM page can also be corrupted if the NVM reset pin has noise. This signal must be tied off properly.

Microsemi recommends installing the following capacitors[5] on the VCCNVM/VCCENVM and VCCOSC/VCCROSC pins:

- Add one bypass capacitor of 10 µF for each power supply plane followed by an array of decoupling capacitors of 0.1 µF.
- Add one 0.1 µF capacitor near each pin.

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2.  During sleep mode in IGLOO devices connect VPUMP to GND.
3.  VPUMP has to be quiet for successful programming. Therefore VPUMP must be separate and required capacitors must be installed close to the FPGA VPUMP pin.
4.  VCCROSC is for SmartFusion.
5.  The capacitors cannot guarantee reliable operation of the device if the board layout is not done properly.

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*Table 13-4* • Programming Header Pin Numbers and Description

| Pin | Signal | Source | Description |
|---|---|---|---|
| 1 | TCK | Programmer | JTAG Clock |
| 2 | GND[1] | – | Signal Reference |
| 3 | TDO | Target Board | Test Data Output |
| 4 | NC | – | No Connect (FlashPro3/3X); Prog_Mode (FlashPro4). See note associated with Figure 13-5 on page 335 regarding Prog_Mode on FlashPro4. |
| 5 | TMS | Programmer | Test Mode Select |
| 6 | VJTAG | Target Board | JTAG Supply Voltage |
| 7 | VPUMP[2] | Programmer/Target Board | Programming Supply Voltage |
| 8 | nTRST | Programmer | JTAG Test Reset (Hi-Z with 10 k : pull-down, HIGH, LOW, or toggling) |
| 9 | TDI | Programmer | Test Data Input |
| 10 | GND[1] | – | Signal Reference |

Notes:

1. Both GND pins must be connected.
2. FlashPro4/3/3X can provide VPUMP if there is only one device on the target board.

# List of Changes

The following table lists critical changes that were made in each revision of the chapter.

| Date | Changes | Page |
|---|---|---|
| August 2012 | This chapter will now be published standalone as an application note in addition to being part of the IGLOO/ProASIC3/Fusion FPGA fabric user's guides (SAR 38769). | N/A |
| | The "ISP Programming Header Information" section was revised to update the description of FP3-10PIN-ADAPTER-KIT in Table 13-3 • Programming Header Ordering Codes, clarifying that it is the adapter kit used for ProASIC^PLUS based boards, and also for ProASIC3 based boards where a compact programming header is being used (SAR 36779). | 335 |
| June 2011 | The VPUMP programming mode voltage was corrected in Table 13-2 • Power Supplies. The correct value is 3.15 V to 3.45 V (SAR 30668). | 329 |
| | The notes associated with Figure 13-5 • Programming Header (top view) and Figure 13-6 • Board Layout and Programming Header Top View were revised to make clear the fact that IGLOO nano V2 devices can be programmed at 1.2 V (SAR 30787). | 335, 337 |
| | Figure 13-6 • Board Layout and Programming Header Top View was revised to include resistors tying TCK and TRST to GND. Microsemi recommends tying off TCK and TRST to GND if JTAG is not used (SAR 22921). RT ProASIC3 was added to the list of device families. | 337 |
| | In the "ISP Programming Header Information" section, the kit for adapting ProASIC^PLUS devices was changed from FP3-10PIN-ADAPTER-KIT to FP3-26PIN-ADAPTER-KIT (SAR 20878). | 335 |
| July 2010 | This chapter is no longer published separately with its own part number and version but is now part of several FPGA fabric user's guides. | N/A |
| | References to FlashPro4 and FlashPro3X were added to this chapter, giving distinctions between them. References to SmartGen were deleted and replaced with Libero IDE Catalog. | N/A |
| | The "ISP Architecture" section was revised to indicate that V2 devices can be programmed at 1.2 V VCC with FlashPro4. | 327 |
| | SmartFusion was added to Table 13-1 • Flash-Based FPGAs Supporting ISP. | 328 |
| | The "Programming Voltage (VPUMP) and VJTAG" section was revised and 1.2 V was added to Table 13-2 • Power Supplies. | 329 |
| | The "Nonvolatile Memory (NVM) Programming Voltage" section is new. | 329 |
| | Cortex-M3 was added to the "Cortex-M1 and Cortex-M3 Device Security" section. | 331 |
| | In the "ISP Programming Header Information" section, the additional header adapter ordering number was changed from FP3-26PIN-ADAPTER to FP3-10PIN-ADAPTER-KIT, which contains 26-pin migration capability. | 335 |
| | The description of NC was updated in Figure 13-5 • Programming Header (top view), Table 13-4 • Programming Header Pin Numbers and Description and Figure 13-6 • Board Layout and Programming Header Top View. | 335, 336 |
| | The "Symptoms of a Signal Integrity Problem" section was revised to add that customers are expected to troubleshoot board-level signal integrity issues by measuring voltages and taking scope plots. "FlashPro4/3/3X allows TCK to be lowered from 6 MHz down to 1 MHz to allow you to address some signal integrity problems" formerly read, "from 24 MHz down to 1 MHz." "The Scan Chain command expects to see 0x2" was changed to 0x1. | 337 |

# 15 – Microprocessor Programming of Microsemi's Low Power Flash Devices

## Introduction

The Fusion, IGLOO, and ProASIC3 families of flash FPGAs support in-system programming (ISP) with the use of a microprocessor. Flash-based FPGAs store their configuration information in the actual cells within the FPGA fabric. SRAM-based devices need an external configuration memory, and hybrid nonvolatile devices store the configuration in a flash memory inside the same package as the SRAM FPGA. Since the programming of a true flash FPGA is simpler, requiring only one stage, it makes sense that programming with a microprocessor in-system should be simpler than with other SRAM FPGAs. This reduces bill-of-materials costs and printed circuit board (PCB) area, and increases system reliability.

Nonvolatile flash technology also gives the low power flash devices the advantage of a secure, low power, live-at-power-up, and single-chip solution. Low power flash devices are reprogrammable and offer time-to-market benefits at an ASIC-level unit cost. These features enable engineers to create high-density systems using existing ASIC or FPGA design flows and tools.

This document is an introduction to microprocessor programming only. To explain the difference between the options available, user's guides for DirectC and STAPL provide more detail on implementing each style.
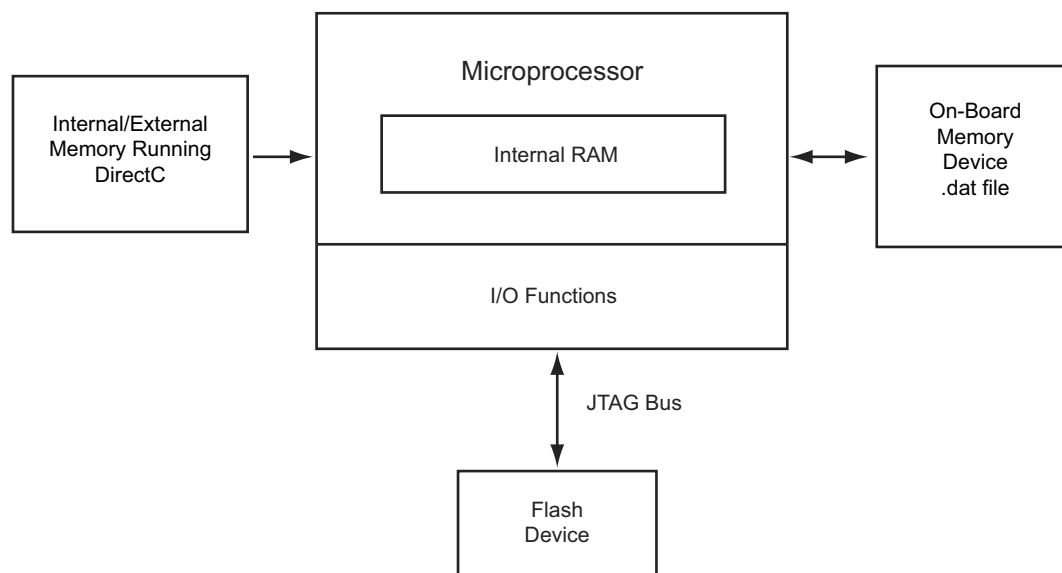


***Figure 15-1 •*** ISP Using Microprocessor