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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	516096
Number of I/O	147
Number of Gates	3000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3pe3000l-1pq208i

The INBUF_FF must be driven by a top-level input port of the design.

The INBUF_FF AND the ULSICC macro must be used to enable type 2 Flash*Freeze mode.

For type 2 Flash*Freeze mode, the INBUF_FF MUST drive some logic in the design.

For type 1 Flash*Freeze mode, the INBUF_FF may drive some logic in the design, but it may also be left floating.

Only one INBUF_FF may be instantiated in a device.

The FF pin threshold voltages are defined by VCCI and the supported single-ended I/O standard in the corresponding I/O bank.

The FF pin Schmitt trigger option may be configured in the I/O attribute editor in Microsemi's Designer software. The Schmitt trigger option is only available for IGLOOe, IGLOO nano, IGLOO PLUS, ProASIC3EL, and RT ProASIC3 devices.

A 2 ns glitch filter resides in the Flash*Freeze Technology block to filter unwanted glitches on the FF pin.

ULSICC

The User Low Static ICC (ULSICC) macro allows the FPGA core to access the Flash*Freeze Technology block so that entering and exiting Flash*Freeze mode can be controlled by the user's design. The ULSICC macro enables a hard block with an available LSICC input port, as shown in Figure 2-3 on page 27 and Figure 2-10 on page 37. Design rules for the ULSICC macro are as follows:

The ULSICC macro by itself cannot enable Flash*Freeze mode. The INBUF_FF AND the ULSICC macro must both be used to enable type 2 Flash*Freeze mode.

The ULSICC controls entering the Flash*Freeze mode by asserting the LSICC input (logic '1') of the ULSICC macro. The FF pin must also be asserted (logic '0') to enter Flash*Freeze mode.

When the LSICC signal is '0', the device cannot enter Flash*Freeze mode; and if already in Flash*Freeze mode, it will exit.

When the ULSICC macro is not instantiated in the user's design, the LSICC port will be tied High.

Flash*Freeze Management IP

The Flash*Freeze management IP can be configured with the Libero (or SmartGen) core generator in a simple, intuitive interface. With the core configuration tool, users can select the number of clocks to be gated, and select whether or not to implement housekeeping. All port names on the Flash*Freeze management IP block can be renamed by the user.

The clock gating (filter) blocks include CLKINT buffers for each gated clock output (version 8.3).

When housekeeping is NOT used, the WAIT_HOUSEKEEPING signal will be automatically fed back into DONE_HOUSEKEEPING inside the core, and the ports will not be available at the IP core interface.

The INBUF_FF macro is automatically instantiated within the IP core.

The INBUF_FF port (default name is "Flash_Freeze_N") must be connected to a top-level input port of the design.

The ULSICC macro is automatically instantiated within the IP core, and the LSICC signal is driven by the FSM.

Timing analysis can be performed on the clock domain of the source clock (i.e., input to the clock gating filters). For example, if CLKin becomes CLKin_gated, the timing can be performed on the CLKin domain in SmartTime.

The gated clocks can be added to the clock list if the user wishes to analyze these clocks specifically. The user can locate the gated clocks by looking for instance names such as those below:

Top/ff1/ff_1_wrapper_inst/user_ff_1_wrapper/Primary_Filter_Instance/
Latch_For_Clock_Gating:Q

Top/ff1/ff_1_wrapper_inst/user_ff_1_wrapper/genblk1.genblk2.secondary_filter[0].
seconday_filter_instance/Latch_For_Clock_Gating:Q

Top/ff1/ff_1_wrapper_inst/user_ff_1_wrapper/genblk1.genblk2.secondary_filter[1].
seconday_filter_instance/Latch_For_Clock_Gating:Q

During Layout, Designer will assign two of the signals to quadrant global locations.

Step 3 (optional)

You can also assign the QCLK1_c and QCLK2_c nets to quadrant regions using the following PDC commands:

```
assign_local_clock  net QCLK1_c   type quadrant UL
assign_local_clock  net QCLK2_c   type quadrant LL
```

Step 4

Import this PDC with the netlist and run Compile again. You will see the following in the Compile report:

```
The following nets have been assigned to a global resource:
Fanout  Type         Name
---------------------------
1536    INT_NET      Net   : EN_ALL_c
                             Driver: EN_ALL_pad_CLKINT
                             Source: AUTO PROMOTED
1536    SET/RESET_NET Net  : ACLR_c
                             Driver: ACLR_pad_CLKINT
                             Source: AUTO PROMOTED
256     CLK_NET      Net   : QCLK3_c
                             Driver: QCLK3_pad_CLKINT
                             Source: AUTO PROMOTED
256     CLK_NET      Net   : $1N14
                             Driver: $1I5/Core
                             Source: ESSENTIAL
256     CLK_NET      Net   : $1N12
                             Driver: $1I6/Core
                             Source: ESSENTIAL
256     CLK_NET      Net   : $1N10
                             Driver: $1I6/Core
                             Source: ESSENTIAL
The following nets have been assigned to a quadrant clock resource using PDC:
Fanout  Type         Name
---------------------------
256     CLK_NET      Net   : QCLK1_c
                             Driver: QCLK1_pad_CLKINT
                             Region: quadrant_UL
256     CLK_NET      Net   : QCLK2_c
                             Driver: QCLK2_pad_CLKINT
                             Region: quadrant_LL
```

Step 5

Run Layout.

Global Management in PLL Design

This section describes the legal global network connections to PLLs in the low power flash devices. For detailed information on using PLLs, refer to "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" section on page 77. Microsemi recommends that you use the dedicated global pins to directly drive the reference clock input of the associated PLL for reduced propagation delays and clock distortion. However, low power flash devices offer the flexibility to connect other signals to reference clock inputs. Each PLL is associated with three global networks (Figure 3-5 on page 52). There are some limitations, such as when trying to use the global and PLL at the same time:

- If you use a PLL with only primary output, you can still use the remaining two free global networks.
- If you use three globals associated with a PLL location, you cannot use the PLL on that location.
- If the YB or YC output is used standalone, it will occupy one global, even though this signal does not go to the global network.

5 V Output Tolerance

IGLOO and ProASIC3 I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, the I/Os can directly drive signals into 5 V TTL receivers. In fact, VOL = 0.4 V and VOH = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceeds the VIL = 0.8 V and VIH = 2 V level requirements of 5 V TTL receivers. Therefore, level 1 and level 0 will be recognized correctly by 5 V TTL receivers.

Schmitt Trigger

A Schmitt trigger is a buffer used to convert a slow or noisy input signal into a clean one before passing it to the FPGA. Using Schmitt trigger buffers guarantees a fast, noise-free input signal to the FPGA.

ProASIC3E devices have Schmitt triggers built into their I/O circuitry. The Schmitt trigger is available for the LVTTL, LVCMOS, and 3.3 V PCI I/O standards.

This feature can be implemented by using a Physical Design Constraints (PDC) command (Table 8-6 on page 218) or by selecting a check box in the I/O Attribute Editor in Designer. The check box is cleared by default.

Selectable Skew between Output Buffer Enable and Disable Times

Low power flash devices have a configurable skew block in the output buffer circuitry that can be enabled to delay output buffer assertion without affecting deassertion time. Since this skew block is only available for the OE signal, the feature can be used in tristate and bidirectional buffers. A typical 1.2 ns delay is added to the OE signal to prevent potential bus contention. Refer to the appropriate family datasheet for detailed timing diagrams and descriptions.

The Skew feature is available for all I/O standards.

This feature can be implemented by using a PDC command (Table 8-6 on page 218) or by selecting a check box in the I/O Attribute Editor in Designer. The check box is cleared by default.

The configurable skew block is used to delay output buffer assertion (enable) without affecting deassertion (disable) time.

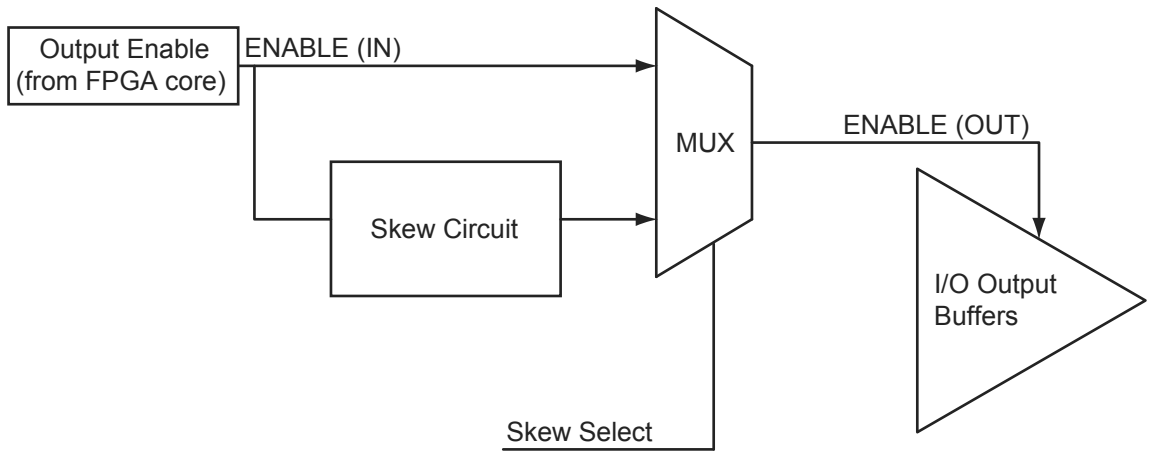

***Figure 8-14* • Block Diagram of Output Enable Path**