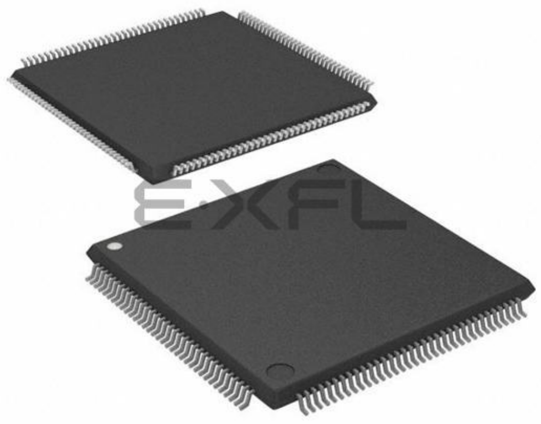

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	110
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.75V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3a3128-alut

1. Description

The AT32UC3A3/A4 is a complete System-On-Chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 84MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems. Higher computation capabilities are achievable using a rich set of DSP instructions.

The AT32UC3A3/A4 incorporates on-chip Flash and SRAM memories for secure and fast access. 64 KBytes of SRAM are directly coupled to the AVR32 UC for performances optimization. Two blocks of 32 Kbytes SRAM are independently attached to the High Speed Bus Matrix, allowing real ping-pong management.

The Peripheral Direct Memory Access Controller (PDCA) enables data transfers between peripherals and memories without processor involvement. The PDCA drastically reduces processing overhead when transferring continuous and large data streams.

The Power Manager improves design flexibility and security: the on-chip Brown-Out Detector monitors the power supply, the CPU runs from the on-chip RC oscillator or from one of external oscillator sources, a Real-Time Clock and its associated timer keeps track of the time.

The device includes two sets of three identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation. 16-bit channels are combined to operate as 32-bit channels.

The AT32UC3A3/A4 also features many communication interfaces for communication intensive applications like UART, SPI or TWI. The USART supports different communication modes, like SPI Mode and LIN Mode. Additionally, a flexible Synchronous Serial Controller (SSC) is available. The SSC provides easy access to serial communication protocols and audio standards like I2S.

The AT32UC3A3/A4 includes a powerfull External Bus Interface to interface all standard memory device like SRAM, SDRAM, NAND Flash or parallel interfaces like LCD Module.

The peripheral set includes a High Speed MCI for SDIO/SD/MMC and a hardware encryption module based on AES algorithm.

The device embeds a 10-bit ADC and a Digital Audio bistream DAC.

The Direct Memory Access controller (DMACA) allows high bandwidth data flows between high speed peripherals (USB, External Memories, MMC, SDIO, ...) and through high speed internal features (AES, internal memories).

The High-Speed (480MBit/s) USB 2.0 Device and Host interface supports several USB Classes at the same time thanks to the rich Endpoint configuration. The Embedded Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor. This periphal has its own dedicated DMA and is perfect for Mass Storage application.

AT32UC3A3/A4 integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

Figure 3-2. LQFP144 Pinout

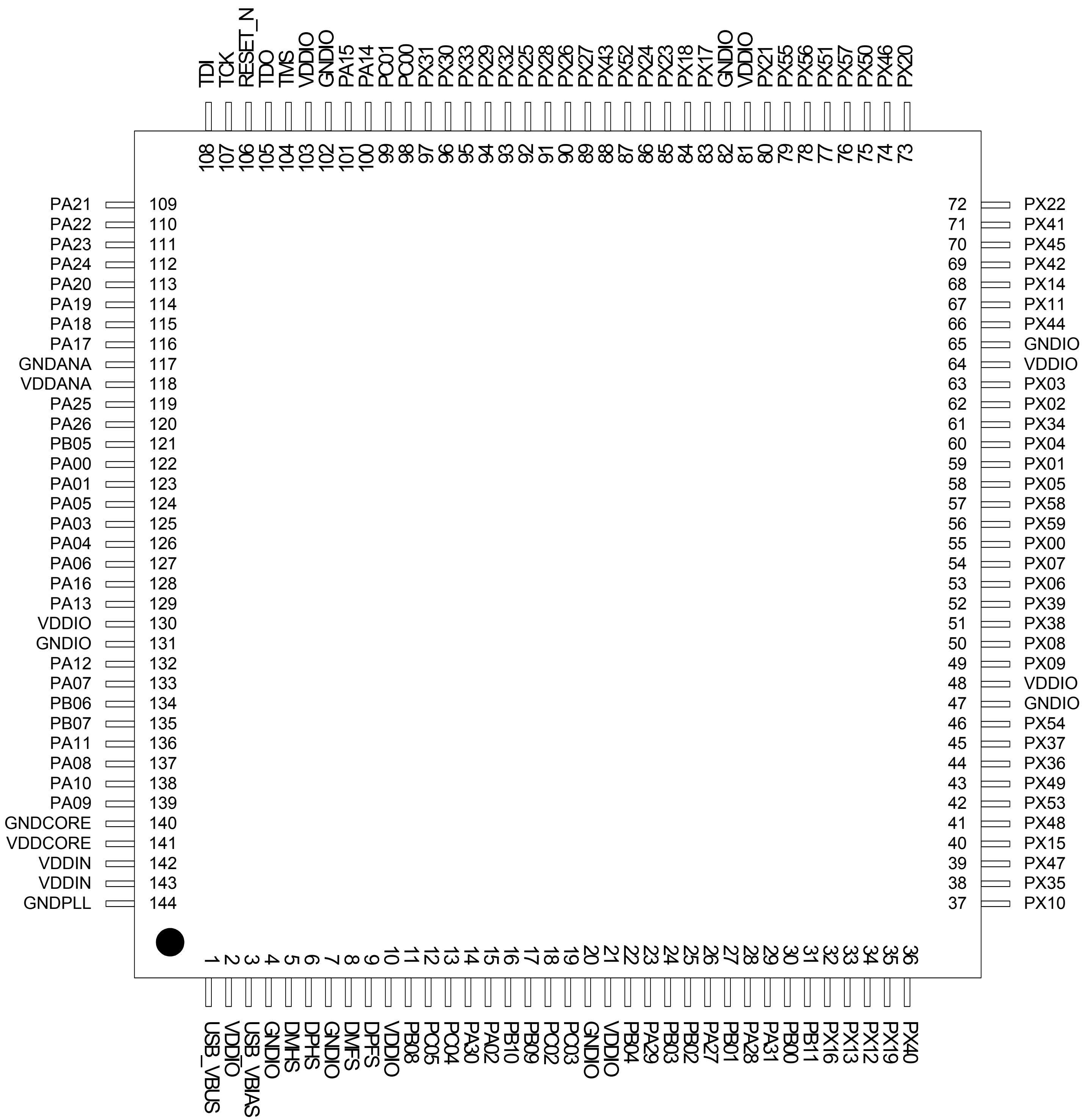


Figure 3-3. VFBGA100 Pinout (top view)

	1	2	3	4	5	6	7	8	9	10
A	PA28	PA27	PB04	PA30	PC02	PC03	PC05	DPHS	DMHS	USB_VBUS
B	PB00	PB01	PB02	PA29	VDDIO	VDDIO	PC04	DPFS	DMFS	GNDPLL
C	PB11	PA31	GNDIO	PB03	PB09	PB08	USB_VBIAS	GNDIO	PA11	PA10
D	PX12	PX10	PX13	PX16/ PX53[1]	PB10	PB07	PB06	PA09	VDDIN	VDDIN
E	PA02/ PX47[1]	GNDIO	PX08	PX09	VDDIO	GNDIO	PA16	PA06/ PA13[1]	PA04	VDDCORE
F	PX19/ PX59[1]	VDDIO	PX06	PX07	GNDIO	VDDIO	PA26/ PB05[1]	PA08	PA03	GNDCORE
G	PX05	PX01	PX02	PX00	PX30	PA23/ PX46[1]	PA12/ PA25[1]	PA00/ PA18[1]	PA05	PA01/ PA17[1]
H	PX04	PX21	GNDIO	PX25	PX31	PA22/ PX20[1]	TMS	GNDANA	PA20/ PX18[1]	PA07/ PA19[1]
J	PX03	PX24	PX26	PX29	VDDIO	VDDANA	PA15/ PX45[1]	TDO	RESET_N	PA24/ PX17[1]
K	PX23	PX27	PX28	PX15/ PX32[1]	PC00/ PX14[1]	PC01	PA14/ PX11[1]	TDI	TCK	PA21/ PX22[1]

Note: 1. Those balls are physically connected to 2 GPIOs. Software must managed carrefully the GPIO configuration to avoid electrical conflict

Table 3-1. GPIO Controller Function Multiplexing

BGA 144	QFP 144	BGA 100	PIN	GPIO	Supply	PIN Type (2)	GPIO function A	B	C	D
L6	84	H9(1)	PX18	69	VDDIO	x2	EBI - ADDR[16]	DMACA - DMAACK[1]	TC0 - A2	
D5	35	F1(1)	PX19	70	VDDIO	x2	EBI - ADDR[15]	EIC - SCAN[0]	TC0 - B2	
L4	73	H6(1)	PX20	71	VDDIO	x2	EBI - ADDR[14]	EIC - SCAN[1]	TC0 - CLK0	
M5	80	H2	PX21	72	VDDIO	x2	EBI - ADDR[13]	EIC - SCAN[2]	TC0 - CLK1	
M1	72	K10(1)	PX22	73	VDDIO	x2	EBI - ADDR[12]	EIC - SCAN[3]	TC0 - CLK2	
M6	85	K1	PX23	74	VDDIO	x2	EBI - ADDR[11]	EIC - SCAN[4]	SSC - TX_CLOCK	
M7	86	J2	PX24	75	VDDIO	x2	EBI - ADDR[10]	EIC - SCAN[5]	SSC - TX_DATA	
M8	92	H4	PX25	76	VDDIO	x2	EBI - ADDR[9]	EIC - SCAN[6]	SSC - RX_DATA	
L9	90	J3	PX26	77	VDDIO	x2	EBI - ADDR[8]	EIC - SCAN[7]	SSC - RX_FRAME_SYNC	
K9	89	K2	PX27	78	VDDIO	x2	EBI - ADDR[7]	SPI0 - MISO	SSC - TX_FRAME_SYNC	
L10	91	K3	PX28	79	VDDIO	x2	EBI - ADDR[6]	SPI0 - MOSI	SSC - RX_CLOCK	
K11	94	J4	PX29	80	VDDIO	x2	EBI - ADDR[5]	SPI0 - SPCK		
M11	96	G5	PX30	81	VDDIO	x2	EBI - ADDR[4]	SPI0 - NPCS[0]		
M10	97	H5	PX31	82	VDDIO	x2	EBI - ADDR[3]	SPI0 - NPCS[1]		
M9	93	K4(1)	PX32	83	VDDIO	x2	EBI - ADDR[2]	SPI0 - NPCS[2]		
M12	95		PX33	84	VDDIO	x2	EBI - ADDR[1]	SPI0 - NPCS[3]		
J3	61		PX34	85	VDDIO	x2	EBI - ADDR[0]	SPI1 - MISO	PM - GCLK[0]	
C2	38		PX35	86	VDDIO	x2	EBI - DATA[15]	SPI1 - MOSI	PM - GCLK[1]	
D3	44		PX36	87	VDDIO	x2	EBI - DATA[14]	SPI1 - SPCK	PM - GCLK[2]	
D2	45		PX37	88	VDDIO	x2	EBI - DATA[13]	SPI1 - NPCS[0]	PM - GCLK[3]	
E1	51		PX38	89	VDDIO	x2	EBI - DATA[12]	SPI1 - NPCS[1]	USART1 - DCD	
F1	52		PX39	90	VDDIO	x2	EBI - DATA[11]	SPI1 - NPCS[2]	USART1 - DSR	
A1	36		PX40	91	VDDIO	x2		MCI - CLK		
M2	71		PX41	92	VDDIO	x2	EBI - CAS			
M3	69		PX42	93	VDDIO	x2	EBI - RAS			
L7	88		PX43	94	VDDIO	x2	EBI - SDA10	USART1 - RI		
K2	66		PX44	95	VDDIO	x2	EBI - SDWE	USART1 - DTR		
L3	70	J7(1)	PX45	96	VDDIO	x3	EBI - SDCK			
K4	74	G6(1)	PX46	97	VDDIO	x2	EBI - SDCKE			
D4	39	E1(1)	PX47	98	VDDIO	x2	EBI - NANDOE	ADC - TRIGGER	MCI - DATA[11]	
F5	41		PX48	99	VDDIO	x2	EBI - ADDR[23]	USB - VBOF	MCI - DATA[10]	
F4	43		PX49	100	VDDIO	x2	EBI - CFRNW	USB - ID	MCI - DATA[9]	
G4	75		PX50	101	VDDIO	x2	EBI - CFCE2	TC1 - B2	MCI - DATA[8]	
G5	77		PX51	102	VDDIO	x2	EBI - CFCE1	DMACA - DMAACK[0]	MCI - DATA[15]	
K7	87		PX52	103	VDDIO	x2	EBI - NCS[3]	DMACA - DMARQ[0]	MCI - DATA[14]	
E4	42	D4(1)	PX53	104	VDDIO	x2	EBI - NCS[2]		MCI - DATA[13]	
E3	46		PX54	105	VDDIO	x2	EBI - NWAIT	USART3 - TXD	MCI - DATA[12]	
J5	79		PX55	106	VDDIO	x2	EBI - ADDR[22]	EIC - SCAN[3]	USART2 - RXD	

Table 3-6. Signal Description List

Signal Name	Function	Type	Active Level	Comments
RESET_N	Reset Pin	Input	Low	
DMA Controller - DMACA (optional)				
DMAACK[1:0]	DMA Acknowledge	Output		
DMARQ[1:0]	DMA Requests	Input		
External Interrupt Controller - EIC				
EXTINT[7:0]	External Interrupt Pins	Input		
SCAN[7:0]	Keypad Scan Pins	Output		
NMI	Non-Maskable Interrupt Pin	Input	Low	
General Purpose Input/Output pin - GPIOA, GPIOB, GPIOC, GPIOX				
PA[31:0]	Parallel I/O Controller GPIO port A	I/O		
PB[11:0]	Parallel I/O Controller GPIO port B	I/O		
PC[5:0]	Parallel I/O Controller GPIO port C	I/O		
PX[59:0]	Parallel I/O Controller GPIO port X	I/O		
External Bus Interface - EBI				
ADDR[23:0]	Address Bus	Output		
CAS	Column Signal	Output	Low	
CFCE1	Compact Flash 1 Chip Enable	Output	Low	
CFCE2	Compact Flash 2 Chip Enable	Output	Low	
CFRNW	Compact Flash Read Not Write	Output		
DATA[15:0]	Data Bus	I/O		
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NCS[5:0]	Chip Select	Output	Low	
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
RAS	Row Signal	Output	Low	

3.4 I/O Line Considerations

3.4.1 JTAG Pins

TMS and TDI pins have pull-up resistors. TDO pin is an output, driven at up to VDDIO, and has no pull-up resistor.

3.4.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

3.4.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike filtering. When used as GPIO pins or used for other peripherals, the pins have the same characteristics as other GPIO pins.

3.4.4 GPIO Pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the I/O Controller. After reset, I/O lines default as inputs with pull-up resistors disabled, except when indicated otherwise in the column “Reset State” of the I/O Controller multiplexing tables.

Table 5-2. Peripheral Address Mapping

Address	Peripheral	Description
0xFFFF0C00	PM	Power Manager - PM
0xFFFF0D00	RTC	Real Time Counter - RTC
0xFFFF0D30	WDT	Watchdog Timer - WDT
0xFFFF0D80	EIC	External Interrupt Controller - EIC
0xFFFF1000	GPIO	General Purpose Input/Output Controller - GPIO
0xFFFF1400	USART0	Universal Synchronous/Asynchronous Receiver/Transmitter - USART0
0xFFFF1800	USART1	Universal Synchronous/Asynchronous Receiver/Transmitter - USART1
0xFFFF1C00	USART2	Universal Synchronous/Asynchronous Receiver/Transmitter - USART2
0xFFFF2000	USART3	Universal Synchronous/Asynchronous Receiver/Transmitter - USART3
0xFFFF2400	SPI0	Serial Peripheral Interface - SPI0
0xFFFF2800	SPI1	Serial Peripheral Interface - SPI1
0xFFFF2C00	TWIM0	Two-wire Master Interface - TWIM0
0xFFFF3000	TWIM1	Two-wire Master Interface - TWIM1
0xFFFF3400	SSC	Synchronous Serial Controller - SSC
0xFFFF3800	TC0	Timer/Counter - TC0
0xFFFF3C00	ADC	Analog to Digital Converter - ADC
0xFFFF4000	ABDAC	Audio Bitstream DAC - ABDAC
0xFFFF4400	TC1	Timer/Counter - TC1

Table 7-2. Normal I/O Pin Characteristics

Symbol	Parameter	Conditions	drive x2	drive x2	drive x3	Unit
f_{MAX}	Output frequency	10pf	40	66	100	MHz
		30pf	18.2	35.7	61.6	MHz
		60pf	7.5	18.5	36.3	MHz
t_{RISE}	Rise time	10pf	2.7	1.4	0.9	ns
		30pf	6.9	3.5	1.9	ns
		60pf	13.4	6.7	3.5	ns
t_{FALL}	Fall time	10pf	3.2	1.7	0.9	ns
		30pf	8.6	4.3	2.26	ns
		60pf	16.5	8.3	4.3	ns

7.4 Regulator characteristics

Table 7-3. Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{VDDIN}	Supply voltage (input)		3.0	3.3	3.6	V
$V_{VDDCORE}$	Supply voltage (output)		1.75	1.85	1.95	V
I_{OUT}	Maximum DC output current	V_{VDDIN} = 3.3V			100	mA

Table 7-4. Decoupling Requirements

Symbol	Parameter	Conditions	Typ.	Technology	Unit
C_{IN1}	Input Regulator Capacitor 1		1	NPO	nF
C_{IN2}	Input Regulator Capacitor 2		4.7	X7R	µF
C_{OUT1}	Output Regulator Capacitor 1		470	NPO	pF
C_{OUT2}	Output Regulator Capacitor 2		2.2	X7R	µF

Table 7-13. Typical Cuurent Consumption by Peripheral

Peripheral	Typ.	Unit
ADC	7	µA/MHz
AES	80	
ABDAC	10	
DMACA	70	
EBI	23	
EIC	0.5	
GPIO	37	
INTC	3	
MCI	40	
MSI	10	
PDCA	20	
SDRAM	5	
SMC	9	
SPI	6	
SSC	10	
RTC	5	
TC	8	
TWIM	2	
TWIS	2	
USART	10	
USBB	90	
WDT	2	

7.7 System Clock Characteristics

These parameters are given in the following conditions:

- V_{DDCORE} = 1.8V

7.7.1 CPU/HSB Clock Characteristics

Table 7-14. Core Clock Waveform Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPCPU})$	CPU Clock Frequency	-40°C < Ambient Temperature < 70°C			84	MHz
$1/(t_{CPCPU})$	CPU Clock Frequency	-40°C < Ambient Temperature < 85°C			66	MHz

7.7.2 PBA Clock Characteristics

Table 7-15. PBA Clock Waveform Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPPBA})$	PBA Clock Frequency	-40°C < Ambient Temperature < 70°C			84	MHz
$1/(t_{CPPBA})$	PBA Clock Frequency	-40°C < Ambient Temperature < 85°C			66	MHz

7.7.3 PBB Clock Characteristics

Table 7-16. PBB Clock Waveform Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPPBB})$	PBB Clock Frequency	-40°C < Ambient Temperature < 70°C			84	MHz
$1/(t_{CPPBB})$	PBB Clock Frequency	-40°C < Ambient Temperature < 85°C			66	MHz

7.8.3 Main Oscillators

Table 7-19. Main Oscillators Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$1/(t_{CPMAIN})$	Oscillator Frequency	External clock on XIN			50	MHz
		Crystal	0.4		20	MHz
C_{L1}, C_{L2}	Internal Load Capacitance ($C_{L1} = C_{L2}$)			7		pF
ESR	Crystal Equivalent Series Resistance				75	Ω
	Duty Cycle		40	50	60	%
t_{ST}	Startup Time	f = 400 KHz f = 8 MHz f = 16 MHz f = 20 MHz		25 4 1.4 1		ms
t_{CH}	XIN Clock High Half-period		0.4 t_{CP}		0.6 t_{CP}	
t_{CL}	XIN Clock Low Half-period		0.4 t_{CP}		0.6 t_{CP}	
C_{IN}	XIN Input Capacitance			7		pF
I_{OSC}	Current Consumption	Active mode at 400 KHz. Gain = G0 Active mode at 8 MHz. Gain = G1 Active mode at 16 MHz. Gain = G2 Active mode at 20 MHz. Gain = G3		30 45 95 205		µA

7.8.4 Phase Lock Loop (PLL0, PLL1)

Table 7-20. PLL Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{OUT}	VCO Output Frequency		80		240	MHz
F_{IN}	Input Frequency (after input divider)		4		16	MHz
I_{PLL}	Current Consumption	Active mode (Fout=80 MHz)		250		µA
		Active mode (Fout=240 MHz)		600		µA

7.8.5 USB Hi-Speed Phase Lock Loop

Table 7-21. PLL Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{OUT}	VCO Output Frequency			480		MHz
F_{IN}	Input Frequency			12		MHz
Delta F_{IN}	Input Frequency Accuracy (applicable to Clock signal on XIN or to Quartz tolerance)		-500		+500	ppm
I_{PLL}	Current Consumption	Active mode @480MHz @1.8V		2.5		mA

Table 7-29. Dynamic Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{VDDUTMI}$	HS Transceiver current consumption	HS transmission		47	60	mA
	HS Transceiver current consumption	HS reception		18	27	mA
	FS/HS Transceiver current consumption	FS transmission 0m cable [(1)]		4	6	mA
	FS/HS Transceiver current consumption	FS transmission 5m cable		26	30	mA
	FS/HS Transceiver current consumption	FS reception		3	4.5	mA

1. Including 1 mA due to Pull-up/Pull-down current consumption.

34.5.5 USB High Speed Design Guidelines

In order to facilitate hardware design, Atmel provides an application note on www.atmel.com.

Table 7-32. SMC Read Signals with no Hold Settings

Symbol	Parameter	Min.	Unit
NRD Controlled (READ_MODE = 1)			
SMC_{19}	Data Setup before NRD High	13.7	ns
SMC_{20}	Data Hold after NRD High	1	ns
NRD Controlled (READ_MODE = 0)			
SMC_{21}	Data Setup before NCS High	13.3	ns
SMC_{22}	Data Hold after NCS High	0	ns

Table 7-33. SMC Write Signals with Hold Settings

Symbol	Parameter	Min.	Unit
NRD Controlled (READ_MODE = 1)			
SMC_{23}	Data Out Valid before NWE High	(nwe pulse length - 1) * t_{CPSMC} - 0.9	ns
SMC_{24}	Data Out Valid after NWE High[(1)]	nwe hold length * t_{CPSMC} - 6	ns
SMC_{25}	NWE High to NBS0/A0 Change[(1)]	nwe hold length * t_{CPSMC} - 1.9	ns
SMC_{26}	NWE High to NBS1 Change[(1)]	nwe hold length * t_{CPSMC} - 1.9	ns
SMC_{29}	NWE High to A1 Change[(1)]	nwe hold length * t_{CPSMC} - 1.9	ns
SMC_{31}	NWE High to A2 - A23 Change[(1)]	nwe hold length * t_{CPSMC} - 1.7	ns
SMC_{32}	NWE High to NCS Inactive[(1)]	(nwe hold length - ncs wr hold length)* t_{CPSMC} - 2.9	ns
SMC_{33}	NWE Pulse Width	nwe pulse length * t_{CPSMC} - 0.9	ns
NRD Controlled (READ_MODE = 0)			
SMC_{34}	Data Out Valid before NCS High	(ncs wr pulse length - 1)* t_{CPSMC} - 4.6	ns
SMC_{35}	Data Out Valid after NCS High[(1)]	ncs wr hold length * t_{CPSMC} - 5.8	ns
SMC_{36}	NCS High to NWE Inactive[(1)]	(ncs wr hold length - nwe hold length)* t_{CPSMC} - 0.6	ns

Note: 1. hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs wr hold length” or “nwe hold length"

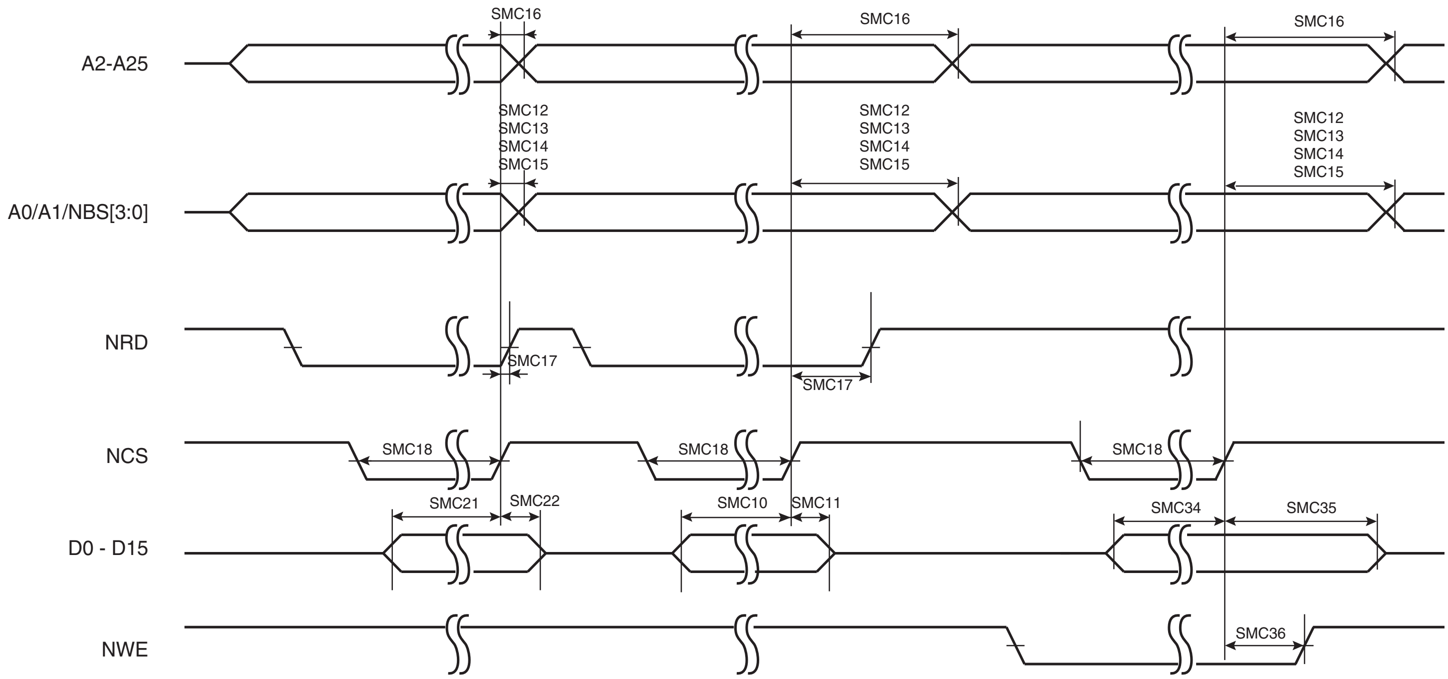
Table 7-34. SMC Write Signals with No Hold Settings (NWE Controlled only)

Symbol	Parameter	Min.	Unit
SMC_{37}	NWE Rising to A2-A25 Valid	5.4	ns
SMC_{38}	NWE Rising to NBS0/A0 Valid	5	ns
SMC_{39}	NWE Rising to NBS1 Change	5	ns
SMC_{40}	NWE Rising to A1/NBS2 Change	5	ns
SMC_{41}	NWE Rising to NBS3 Change	5	ns
SMC_{42}	NWE Rising to NCS Rising	5.1	ns

Table 7-34. SMC Write Signals with No Hold Settings (NWE Controlled only)

Symbol	Parameter	Min.	Unit
SMC_{43}	Data Out Valid before NWE Rising	(nwe pulse length - 1) * t_{CPSMC} - 1.2	ns
SMC_{44}	Data Out Valid after NWE Rising	5	ns
SMC_{45}	NWE Pulse Width	nwe pulse length * t_{CPSMC} - 0.9	ns

Figure 7-7. SMC Signals for NCS Controlled Accesses.



9. Ordering Information

Device	Ordering Code	Package	Conditioning	Temperature Operating Range
AT32UC3A3256S	AT32UC3A3256S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3256S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3256	AT32UC3A3256-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3256-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3128S	AT32UC3A3128S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3128S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3128	AT32UC3A3128-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3128-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A364S	AT32UC3A364S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A364S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A364	AT32UC3A364-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A364-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4256S	AT32UC3A4256S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4256S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4256	AT32UC3A4256-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4256-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4128S	AT32UC3A4128S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4128S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4128	AT32UC3A4128-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4128-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A464S	AT32UC3A464S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A464S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A464	AT32UC3A464-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A464-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)

For higher polling time, the software must freeze the pipe for the desired period in order to prevent any "extra" token.

10.1.5 ADC

Sleep Mode activation needs additional A to D conversion
If the ADC sleep mode is activated when the ADC is idle the ADC will not enter sleep mode before after the next AD conversion.
Fix/Workaround
Activate the sleep mode in the mode register and then perform an AD conversion.

10.1.6 USART

ISO7816 info register US_NER cannot be read
The NER register always returns zero.
Fix/Workaround
None.

The LIN ID is not transmitted in mode PDCM='0'
Fix/Workaround
Using USART in mode LIN master with the PDCM bit = '0', the LINID written at the first address of the transmit buffer is not used. The LINID must be written in the LINIR register, after the configuration and start of the PDCA transfer. Writing the LINID in the LINIR register will start the transfer whenever the PDCA transfer is ready.

The LINID interrupt is only available for the header reception and not available for the header transmission
Fix/Workaround
None.

USART LIN mode is not functional with the PDCA if PDCM bit in LINMR register is set to 1
If a PDCA transfer is initiated in USART LIN mode with PDCM bit set to 1, the transfer never starts.
Fix/Workaround
Only use PDCM=0 configuration with the PDCA transfer.

10.1.7 SPI

SPI disable does not work in SLAVE mode
SPI disable does not work in SLAVE mode.
Fix/Workaround
Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0
When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
Fix/Workaround
When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

SMBALERT bit may be set after reset
The SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.
Fix/Workaround
After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

10.2.13 TWIS

Clearing the NAK bit before the BTF bit is set locks up the TWI bus
When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.
Fix/Workaround
Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

TWIS stretch on Address match error
When the TWIS stretches TWCK due to a slave address match, it also holds TWD low for the same duration if it is to be receiving data. When TWIS releases TWCK, it releases TWD at the same time. This can cause a TWI timing violation.
Fix/Workaround
None.

10.2.14 MCI

MCI_CLK features is not available on PX12, PX13 and PX40
Fix/Workaround
MCI_CLK feature is available on PA27 only.

The busy signal of the responses R1b is not taken in account for CMD12 STOP_TRANSFER
It is not possible to know the busy status of the card during the response (R1b) for the commands CMD12.
Fix/Workaround
The card busy line should be polled through the GPIO Input Value register (IVR) for commands CMD12.

10.2.15 SSC

Frame Synchro and Frame Synchro Data are delayed by one clock cycle
The frame synchro and the frame synchro data are delayed from 1 SSC_CLOCK when:
- Clock is CKDIV
- The START is selected on either a frame synchro edge or a level
- Frame synchro data is enabled
- Transmit clock is gated on output (through CKO field)

Fix/Workaround
Transmit or receive CLOCK must not be gated (by the mean of CKO field) when START condition is performed on a generated frame synchro.

When the main clock is RCSYS, TIMER_CLOCK5 is equal to PBA clock
When the main clock is generated from RCSYS, TIMER_CLOCK5 is equal to PBA Clock and not PBA Clock / 128.
Fix/Workaround
None.

RETE instruction does not clear SREG[L] from interrupts
The RETE instruction clears SREG[L] as expected from exceptions.
Fix/Workaround
When using the STCOND instruction, clear SREG[L] in the stacked value of SR before returning from interrupts with RETE.

RETS behaves incorrectly when MPU is enabled
RETS behaves incorrectly when MPU is enabled and MPU is configured so that system stack is not readable in unprivileged mode.
Fix/Workaround
Make system stack readable in unprivileged mode, or return from supervisor mode using rete instead of rets. This requires:
1. Changing the mode bits from 001 to 110 before issuing the instruction. Updating the mode bits to the desired value must be done using a single mtsr instruction so it is done atomically. Even if this step is generally described as not safe in the UC technical reference manual, it is safe in this very specific case.
2. Execute the RETE instruction.

In the PRAS and PRBS registers, the MxPR fields are only two bits
In the PRAS and PRBS registers, the MxPR fields are only two bits wide, instead of four bits. The unused bits are undefined when reading the registers.
Fix/Workaround
Mask undefined bits when reading PRAS and PRBS.

Multiply instructions do not work on RevD
All the multiply instructions do not work.
Fix/Workaround
Do not use the multiply instructions.

10.3.3 MPU

Privilege violation when using interrupts in application mode with protected system stack
If the system stack is protected by the MPU and an interrupt occurs in application mode, an MPU DTLB exception will occur.
Fix/Workaround
Make a DTLB Protection (Write) exception handler which permits the interrupt request to be handled in privileged mode.

10.3.4 USB

UPCFGn.INTFRQ is irrelevant for isochronous pipe
As a consequence, isochronous IN and OUT tokens are sent every 1ms (Full Speed), or every 125uS (High Speed).
Fix/Workaround
For higher polling time, the software must freeze the pipe for the desired period in order to prevent any "extra" token.

10.3.7 SPI

SPI disable does not work in SLAVE mode
SPI disable does not work in SLAVE mode.
Fix/Workaround
Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0
When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
Fix/Workaround
When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0
When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
Fix/Workaround
Disable mode fault detection by writing a one to MR.MODFDIS.

Disabling SPI has no effect on the SR.TDRE bit
Disabling SPI has no effect on the SR.TDRE bit whereas the write data command is filtered when SPI is disabled. Writing to TDR when SPI is disabled will not clear SR.TDRE. If SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR until its buffer is empty, and this data will be lost.
Fix/Workaround
Disable the PDCA, add two NOPs, and disable the SPI. To continue the transfer, enable the SPI and PDCA.

10.3.8 Power Manager

OSC32 not functionnal in Crystal Modes (OSC32CTRL.MODE=1 or OSC32CTRL.MODE=2)
OSC32 clock output is not active even if the oscillation signal is present on XIN32/XOUT32 pins.
OSC32RDY bit may still set even if the CLK32 is not active.
External clock mode (OSC32CTRL.MODE=0) is not affected.

Fix/Workaround
None.

Clock sources will not be stopped in STATIC sleep mode if the difference between CPU and PBx division factor is too high
If the division factor between the CPU/HSB and PBx frequencies is more than 4 when going to a sleep mode where the system RC oscillator is turned off, then high speed clock sources will not be turned off. This will result in a significantly higher power consumption during the sleep mode.
Fix/Workaround
Before going to sleep modes where the system RC oscillator is stopped, make sure that the factor between the CPU/HSB and PBx frequencies is less than or equal to 4.