What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, POR, WDT
Number of I/O	88
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.75V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at32uc3a4128s-c1ur

- – **Support for SPI and LIN**
- – **Optionnal support for IrDA, ISO7816, Hardware Handshaking, RS485 interfaces and Modem Line**
- **Two Master/Slave Serial Peripheral Interfaces (SPI) with Chip Select Signals**
- **One Synchronous Serial Protocol Controller**
  - – **Supports I2S and Generic Frame-Based Protocols**
- **Two Master/Slave Two-Wire Interface (TWI), 400 kbit/s I2C-compatible**
- **16-bit Stereo Audio Bitstream**
  - – **Sample Rate Up to 50 KHz**
- **QTouch® Library Support**
  - – **Capacitive Touch Buttons, Sliders, and Wheels**
  - – **QTouch and QMatrix Acquisition**
- **On-Chip Debug System (JTAG interface)**
  - – **Nexus Class 2+, Runtime Control, Non-Intrusive Data and Program Trace**
- **110 General Purpose Input/Output (GPIOs)**
  - – **Standard or High Speed mode**
  - – **Toggle capability: up to 84 MHz**
- **Packages**
  - – **144-ball TFBGA, 11x11 mm, pitch 0.8 mm**
  - – **144-pin LQFP, 22x22 mm, pitch 0.5 mm**
  - – **100-ball VFBGA, 7x7 mm, pitch 0.65 mm**
- **Single 3.3V Power Supply**

1. Description

The AT32UC3A3/A4 is a complete System-On-Chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 84MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern operating systems and real-time operating systems. Higher computation capabilities are achievable using a rich set of DSP instructions.

The AT32UC3A3/A4 incorporates on-chip Flash and SRAM memories for secure and fast access. 64 KBytes of SRAM are directly coupled to the AVR32 UC for performances optimization. Two blocks of 32 Kbytes SRAM are independently attached to the High Speed Bus Matrix, allowing real ping-pong management.

The Peripheral Direct Memory Access Controller (PDCA) enables data transfers between peripherals and memories without processor involvement. The PDCA drastically reduces processing overhead when transferring continuous and large data streams.

The Power Manager improves design flexibility and security: the on-chip Brown-Out Detector monitors the power supply, the CPU runs from the on-chip RC oscillator or from one of external oscillator sources, a Real-Time Clock and its associated timer keeps track of the time.

The device includes two sets of three identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation. 16-bit channels are combined to operate as 32-bit channels.

The AT32UC3A3/A4 also features many communication interfaces for communication intensive applications like UART, SPI or TWI. The USART supports different communication modes, like SPI Mode and LIN Mode. Additionally, a flexible Synchronous Serial Controller (SSC) is available. The SSC provides easy access to serial communication protocols and audio standards like I2S.

The AT32UC3A3/A4 includes a powerfull External Bus Interface to interface all standard memory device like SRAM, SDRAM, NAND Flash or parallel interfaces like LCD Module.

The peripheral set includes a High Speed MCI for SDIO/SD/MMC and a hardware encryption module based on AES algorithm.

The device embeds a 10-bit ADC and a Digital Audio bistream DAC.

The Direct Memory Access controller (DMACA) allows high bandwidth data flows between high speed peripherals (USB, External Memories, MMC, SDIO, ...) and through high speed internal features (AES, internal memories).

The High-Speed (480MBit/s) USB 2.0 Device and Host interface supports several USB Classes at the same time thanks to the rich Endpoint configuration. The Embedded Host interface allows device like a USB Flash disk or a USB printer to be directly connected to the processor. This periphal has its own dedicated DMA and is perfect for Mass Storage application.

AT32UC3A3/A4 integrates a class 2+ Nexus 2.0 On-Chip Debug (OCD) System, with non-intrusive real-time trace, full-speed read/write memory access in addition to basic runtime control.

2. Overview
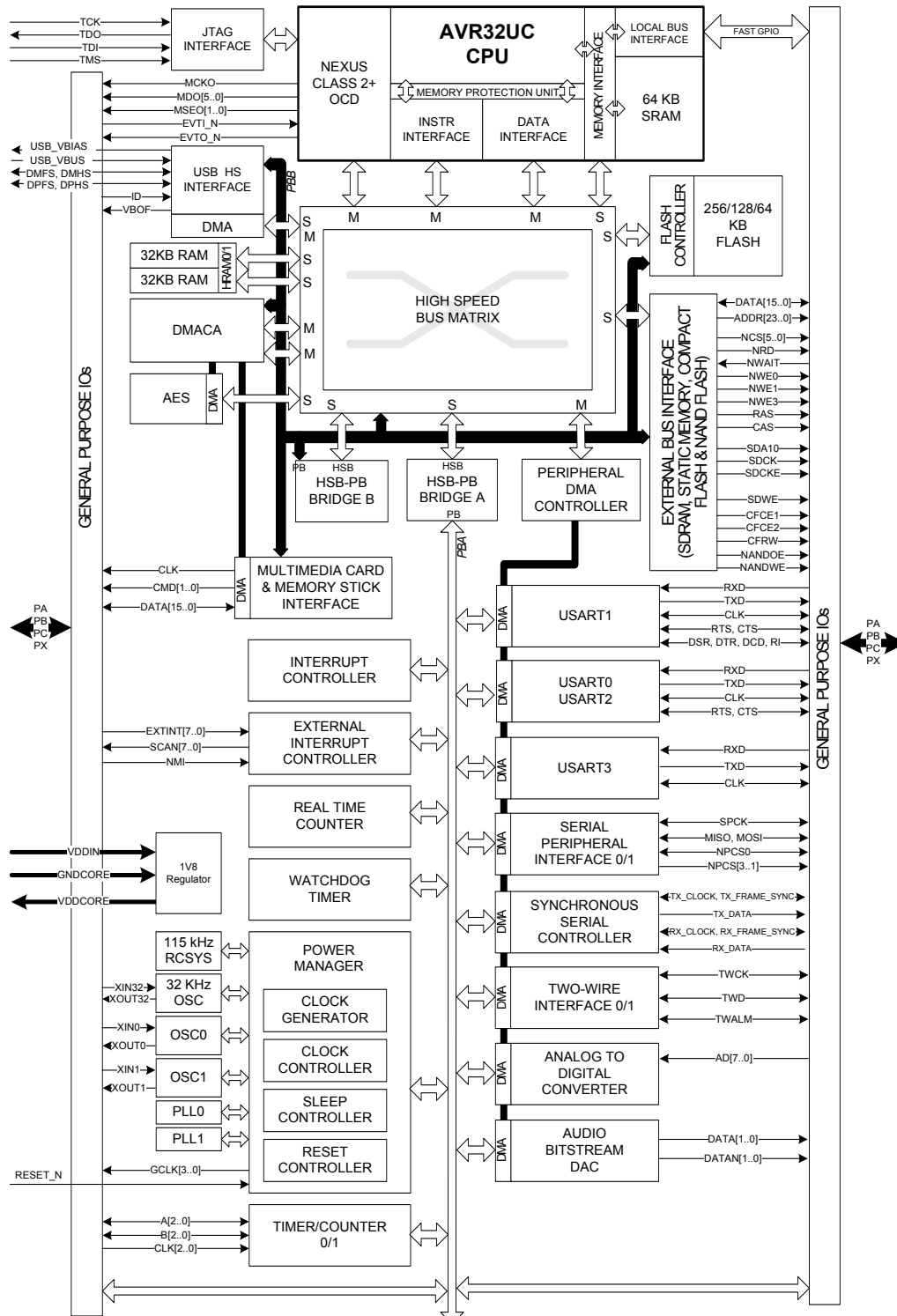
2.1 Block Diagram

Figure 2-1. Block Diagram

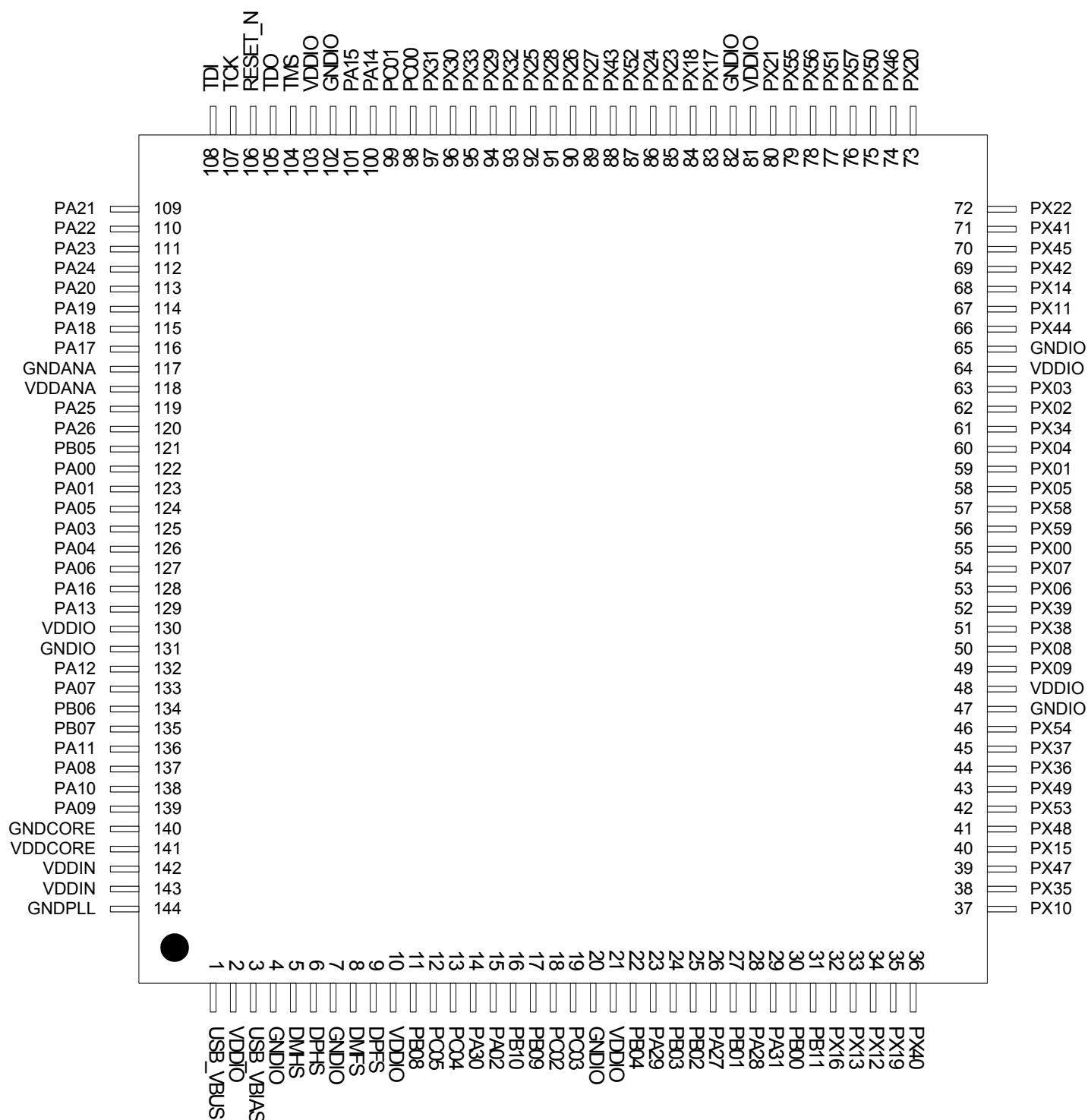**Figure 3-2.** LQFP144 Pinout

Figure 3-3. VFBGA100 Pinout (top view)

Note: 1. Those balls are physically connected to 2 GPIOs. Software must managed carrefully the GPIO configuration to avoid electrical conflict

Table 3-1. GPIO Controller Function Multiplexing

BGA 144	QFP 144	BGA 100	PIN	GPIO	Supply	PIN Type [2]	GPIO function A	B	C	D
L6	84	H9[1]	PX18	69	VDDIO	x2	EBI - ADDR[16]	DMACA - DMAACK[1]	TC0 - A2	
D5	35	F1[1]	PX19	70	VDDIO	x2	EBI - ADDR[15]	EIC - SCAN[0]	TC0 - B2	
L4	73	H6[1]	PX20	71	VDDIO	x2	EBI - ADDR[14]	EIC - SCAN[1]	TC0 - CLK0	
M5	80	H2	PX21	72	VDDIO	x2	EBI - ADDR[13]	EIC - SCAN[2]	TC0 - CLK1	
M1	72	K10[1]	PX22	73	VDDIO	x2	EBI - ADDR[12]	EIC - SCAN[3]	TC0 - CLK2	
M6	85	K1	PX23	74	VDDIO	x2	EBI - ADDR[11]	EIC - SCAN[4]	SSC - TX_CLOCK	
M7	86	J2	PX24	75	VDDIO	x2	EBI - ADDR[10]	EIC - SCAN[5]	SSC - TX_DATA	
M8	92	H4	PX25	76	VDDIO	x2	EBI - ADDR[9]	EIC - SCAN[6]	SSC - RX_DATA	
L9	90	J3	PX26	77	VDDIO	x2	EBI - ADDR[8]	EIC - SCAN[7]	SSC - RX_FRAME_SYNC	
K9	89	K2	PX27	78	VDDIO	x2	EBI - ADDR[7]	SPI0 - MISO	SSC - TX_FRAME_SYNC	
L10	91	K3	PX28	79	VDDIO	x2	EBI - ADDR[6]	SPI0 - MOSI	SSC - RX_CLOCK	
K11	94	J4	PX29	80	VDDIO	x2	EBI - ADDR[5]	SPI0 - SPCK		
M11	96	G5	PX30	81	VDDIO	x2	EBI - ADDR[4]	SPI0 - NPCS[0]		
M10	97	H5	PX31	82	VDDIO	x2	EBI - ADDR[3]	SPI0 - NPCS[1]		
M9	93	K4[1]	PX32	83	VDDIO	x2	EBI - ADDR[2]	SPI0 - NPCS[2]		
M12	95		PX33	84	VDDIO	x2	EBI - ADDR[1]	SPI0 - NPCS[3]		
J3	61		PX34	85	VDDIO	x2	EBI - ADDR[0]	SPI1 - MISO	PM - GCLK[0]	
C2	38		PX35	86	VDDIO	x2	EBI - DATA[15]	SPI1 - MOSI	PM - GCLK[1]	
D3	44		PX36	87	VDDIO	x2	EBI - DATA[14]	SPI1 - SPCK	PM - GCLK[2]	
D2	45		PX37	88	VDDIO	x2	EBI - DATA[13]	SPI1 - NPCS[0]	PM - GCLK[3]	
E1	51		PX38	89	VDDIO	x2	EBI - DATA[12]	SPI1 - NPCS[1]	USART1 - DCD	
F1	52		PX39	90	VDDIO	x2	EBI - DATA[11]	SPI1 - NPCS[2]	USART1 - DSR	
A1	36		PX40	91	VDDIO	x2		MCI - CLK		
M2	71		PX41	92	VDDIO	x2	EBI - CAS			
M3	69		PX42	93	VDDIO	x2	EBI - RAS			
L7	88		PX43	94	VDDIO	x2	EBI - SDA10	USART1 - RI		
K2	66		PX44	95	VDDIO	x2	EBI - SDWE	USART1 - DTR		
L3	70	J7[1]	PX45	96	VDDIO	x3	EBI - SDCK			
K4	74	G6[1]	PX46	97	VDDIO	x2	EBI - SDCKE			
D4	39	E1[1]	PX47	98	VDDIO	x2	EBI - NANDOE	ADC - TRIGGER	MCI - DATA[11]	
F5	41		PX48	99	VDDIO	x2	EBI - ADDR[23]	USB - VBOF	MCI - DATA[10]	
F4	43		PX49	100	VDDIO	x2	EBI - CFRNW	USB - ID	MCI - DATA[9]	
G4	75		PX50	101	VDDIO	x2	EBI - CFCE2	TC1 - B2	MCI - DATA[8]	
G5	77		PX51	102	VDDIO	x2	EBI - CFCE1	DMACA - DMAACK[0]	MCI - DATA[15]	
K7	87		PX52	103	VDDIO	x2	EBI - NCS[3]	DMACA - DMARQ[0]	MCI - DATA[14]	
E4	42	D4[1]	PX53	104	VDDIO	x2	EBI - NCS[2]		MCI - DATA[13]	
E3	46		PX54	105	VDDIO	x2	EBI - NWAIT	USART3 - TXD	MCI - DATA[12]	
J5	79		PX55	106	VDDIO	x2	EBI - ADDR[22]	EIC - SCAN[3]	USART2 - RXD	

Table 3-6. Signal Description List

Signal Name	Function	Type	Active Level	Comments
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI0, TWI1				
TWCK	Serial Clock	I/O		
TWD	Serial Data	I/O		
TWALM	SMBALERT signal	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input		
DCD	Data Carrier Detect			Only USART1
DSR	Data Set Ready			Only USART1
DTR	Data Terminal Ready			Only USART1
RI	Ring Indicator			Only USART1
RTS	Request To Send	Output		
RXD	Receive Data	Input		
TXD	Transmit Data	Output		
Analog to Digital Converter - ADC				
AD0 - AD7	Analog input pins	Analog input		
Audio Bitstream DAC (ABDAC)				
DATA0-DATA1	D/A Data out	Output		
DATAN0-DATAN1	D/A Data inverted out	Output		
Universal Serial Bus Device - USB				
DMFS	USB Full Speed Data -	Analog		
DPFS	USB Full Speed Data +	Analog		

Table 3-6. Signal Description List

Signal Name	Function	Type	Active Level	Comments
DMHS	USB High Speed Data -	Analog		
DPHS	USB High Speed Data +	Analog		
USB_VBIAS	USB VBIAS reference	Analog		Connect to the ground through a 6810 ohms (+/- 1%) resistor in parallel with a 10pf capacitor. If USB hi-speed feature is not required, leave this pin unconnected to save power
USB_VBUS	USB VBUS signal	Output		
VBOF	USB VBUS on/off bus power control port	Output		
ID	ID Pin fo the USB bus	Input		

status register. Upon entry into Debug mode, hardware sets the SR[D] bit and jumps to the Debug Exception handler. By default, Debug mode executes in the exception context, but with dedicated Return Address Register and Return Status Register. These dedicated registers remove the need for storing this data to the system stack, thereby improving debuggability. The mode bits in the status register can freely be manipulated in Debug mode, to observe registers in all contexts, while retaining full privileges.

Debug mode is exited by executing the *retd* instruction. This returns to the previous context.

4.5.5   Entry Points for Events

Several different event handler entry points exists. In AVR32UC, the reset address is 0x8000_0000. This places the reset address in the boot flash memory area.

TLB miss exceptions and *scall* have a dedicated space relative to EVBA where their event handler can be placed. This speeds up execution by removing the need for a jump instruction placed at the program address jumped to by the event hardware. All other exceptions have a dedicated event routine entry point located relative to EVBA. The handler routine address identifies the exception source directly.

AVR32UC uses the ITLB and DTLB protection exceptions to signal a MPU protection violation. ITLB and DTLB miss exceptions are used to signal that an access address did not map to any of the entries in the MPU. TLB multiple hit exception indicates that an access address did map to multiple TLB entries, signalling an error.

All external interrupt requests have entry points located at an offset relative to EVBA. This autovector offset is specified by an external Interrupt Controller. The programmer must make sure that none of the autovector offsets interfere with the placement of other code. The autovector offset has 14 address bits, giving an offset of maximum 16384 bytes.

Special considerations should be made when loading EVBA with a pointer. Due to security considerations, the event handlers should be located in non-writeable flash memory, or optionally in a privileged memory protection region if an MPU is present.

If several events occur on the same instruction, they are handled in a prioritized way. The priority ordering is presented in Table 4-4. If events occur on several instructions at different locations in the pipeline, the events on the oldest instruction are always handled before any events on any younger instruction, even if the younger instruction has events of higher priority than the oldest instruction. An instruction B is younger than an instruction A if it was sent down the pipeline later than A.

The addresses and priority of simultaneous events are shown in Table 4-4. Some of the exceptions are unused in AVR32UC since it has no MMU, coprocessor interface, or floating-point unit.

Table 5-2. Peripheral Address Mapping

Address	Peripheral	Description
0xFFFF0C00	PM	Power Manager - PM
0xFFFF0D00	RTC	Real Time Counter - RTC
0xFFFF0D30	WDT	Watchdog Timer - WDT
0xFFFF0D80	EIC	External Interrupt Controller - EIC
0xFFFF1000	GPIO	General Purpose Input/Output Controller - GPIO
0xFFFF1400	USART0	Universal Synchronous/Asynchronous Receiver/Transmitter - USART0
0xFFFF1800	USART1	Universal Synchronous/Asynchronous Receiver/Transmitter - USART1
0xFFFF1C00	USART2	Universal Synchronous/Asynchronous Receiver/Transmitter - USART2
0xFFFF2000	USART3	Universal Synchronous/Asynchronous Receiver/Transmitter - USART3
0xFFFF2400	SPI0	Serial Peripheral Interface - SPI0
0xFFFF2800	SPI1	Serial Peripheral Interface - SPI1
0xFFFF2C00	TWIM0	Two-wire Master Interface - TWIM0
0xFFFF3000	TWIM1	Two-wire Master Interface - TWIM1
0xFFFF3400	SSC	Synchronous Serial Controller - SSC
0xFFFF3800	TC0	Timer/Counter - TC0
0xFFFF3C00	ADC	Analog to Digital Converter - ADC
0xFFFF4000	ABDAC	Audio Bitstream DAC - ABDAC
0xFFFF4400	TC1	Timer/Counter - TC1

7.9 ADC Characteristics

Table 7-22. Channel Conversion Time and ADC Clock

Parameter	Conditions	Min.	Typ.	Max.	Unit
ADC Clock Frequency	10-bit resolution mode			5	MHz
	8-bit resolution mode			8	MHz
Startup Time	Return from Idle Mode			20	µs
Track and Hold Acquisition Time		600			ns
Conversion Time	ADC Clock = 5 MHz			2	µs
	ADC Clock = 8 MHz			1.25	µs
Throughput Rate	ADC Clock = 5 MHz			384 [1]	kSPS
	ADC Clock = 8 MHz			533 [2]	kSPS

1. Corresponds to 13 clock cycles: 3 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.
2. Corresponds to 15 clock cycles: 5 clock cycles for track and hold acquisition time and 10 clock cycles for conversion.

Table 7-23. ADC Power Consumption

Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Consumption on VDDANA [1]	On 13 samples with ADC clock = 5 MHz			1.25	mA

1. Including internal reference input current

Table 7-24. Analog Inputs

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range		0		VDDANA	V
Input Leakage Current				1	µA
Input Capacitance			7		pF
Input Resistance			350	850	Ohm

Table 7-25. Transfer Characteristics in 8-bit mode

Parameter	Conditions	Min.	Typ.	Max.	Unit
Resolution			8		Bit
Absolute Accuracy	ADC Clock = 5 MHz			0.8	LSB
	ADC Clock = 8 MHz			1.5	LSB
Integral Non-linearity	ADC Clock = 5 MHz		0.35	0.5	LSB
	ADC Clock = 8 MHz		0.5	1.5	LSB
Differential Non-linearity	ADC Clock = 5 MHz		0.3	0.5	LSB
	ADC Clock = 8 MHz		0.5	1.5	LSB
Offset Error	ADC Clock = 5 MHz	-1.5		1.5	LSB
Gain Error	ADC Clock = 5 MHz	-0.5		0.5	LSB

Table 7-29. Dynamic Power Consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{VDDUTMI}	HS Transceiver current consumption	HS transmission		47	60	mA
	HS Transceiver current consumption	HS reception		18	27	mA
	FS/HS Transceiver current consumption	FS transmission 0m cable [1]		4	6	mA
	FS/HS Transceiver current consumption	FS transmission 5m cable		26	30	mA
	FS/HS Transceiver current consumption	FS reception		3	4.5	mA

1.   Including 1 mA due to Pull-up/Pull-down current consumption.

34.5.5   USB High Speed Design Guidelines

In order to facilitate hardware design, Atmel provides an application note on www.atmel.com.

Figure 7-9. SDRAMC Signals relative to SDCK.
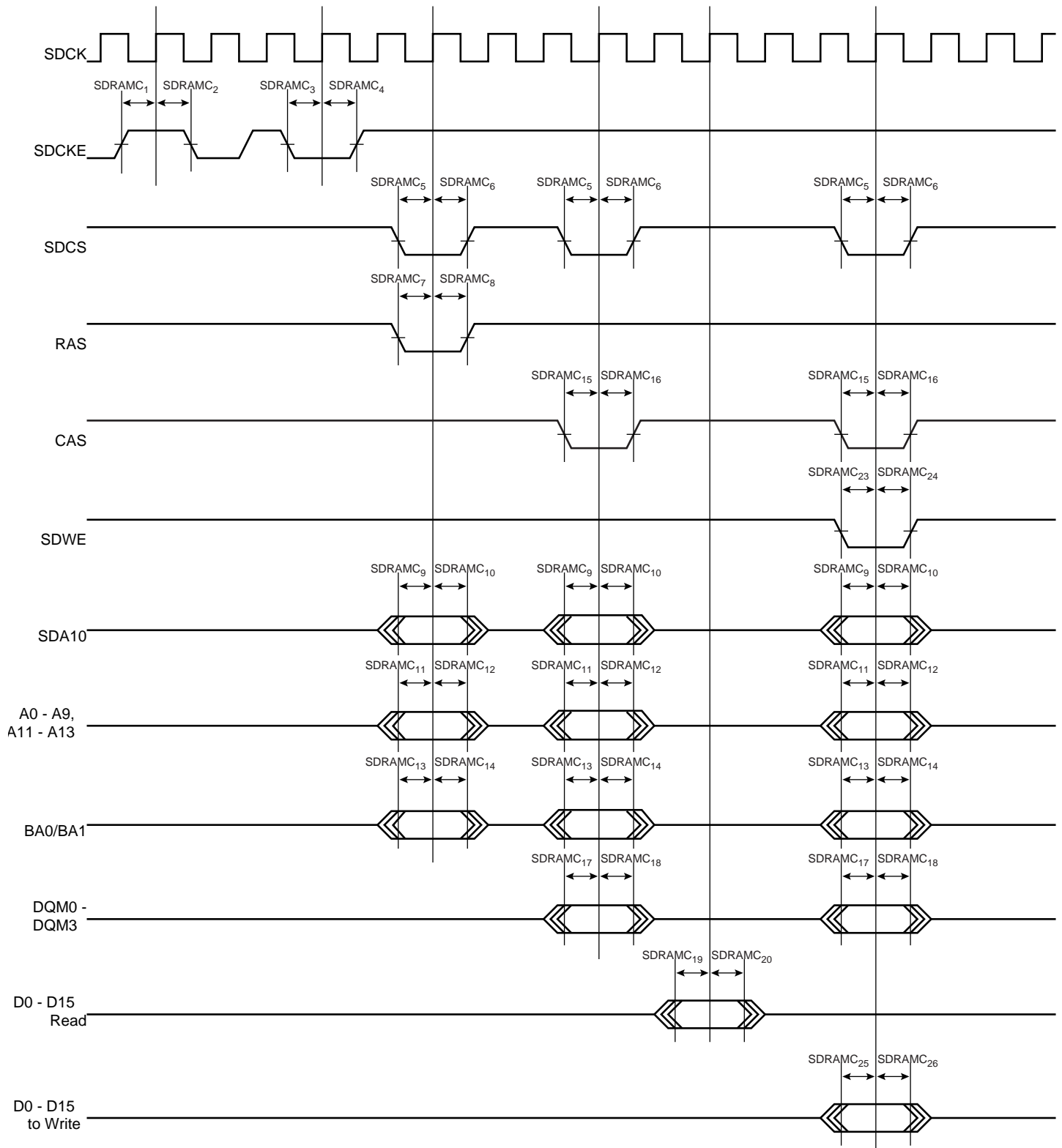
7.15   Flash Memory Characteristics

The following table gives the device maximum operating frequency depending on the field FWS of the Flash FSR register. This field defines the number of wait states required to access the Flash Memory. Flash operating frequency equals the CPU/HSB frequency.

Table 7-39.   Flash Operating Frequency

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{FOP}	Flash Operating Frequency	FWS = 0 High Speed Read Mode Disable -40°C < Ambient Temperature < 85°C			36	MHz
		FWS = 1 High Speed Read Mode Disable -40°C < Ambient Temperature < 85°C			66	MHz
		FWS = 0 High Speed Read Mode Enable -40°C < Ambient Temperature < 70°C			42	MHz
		FWS = 1 High Speed Read Mode Enable -40°C < Ambient Temperature < 70°C			84	MHz

Table 7-40.   Parts Programming Time

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{FPP}	Page Programming Time			5		ms
T_{FFP}	Fuse Programming Time			0.5		ms
T_{FCE}	Chip erase Time			8		ms

Table 7-41.   Flash Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{FARRAY}	Flash Array Write/Erase cycle				100K	cycle
N_{FFUSE}	General Purpose Fuses write cycle				1000	cycle
T_{FDR}	Flash Data Retention Time			15		year

8.2   Package Drawings

Figure 8-1.   TFBGA 144 package drawing

	MM		
	MIN	NOM	MAX
A	----	----	1.20
A1	0.27	----	0.37
A2	0.790 BSC		
e	0.80 BSC		
b	0.38	----	0.48
E/D	11.00 BSC		
I/J	1.100 REF		
ddd	copla: 0.120		
bbb	copla: 0.200		
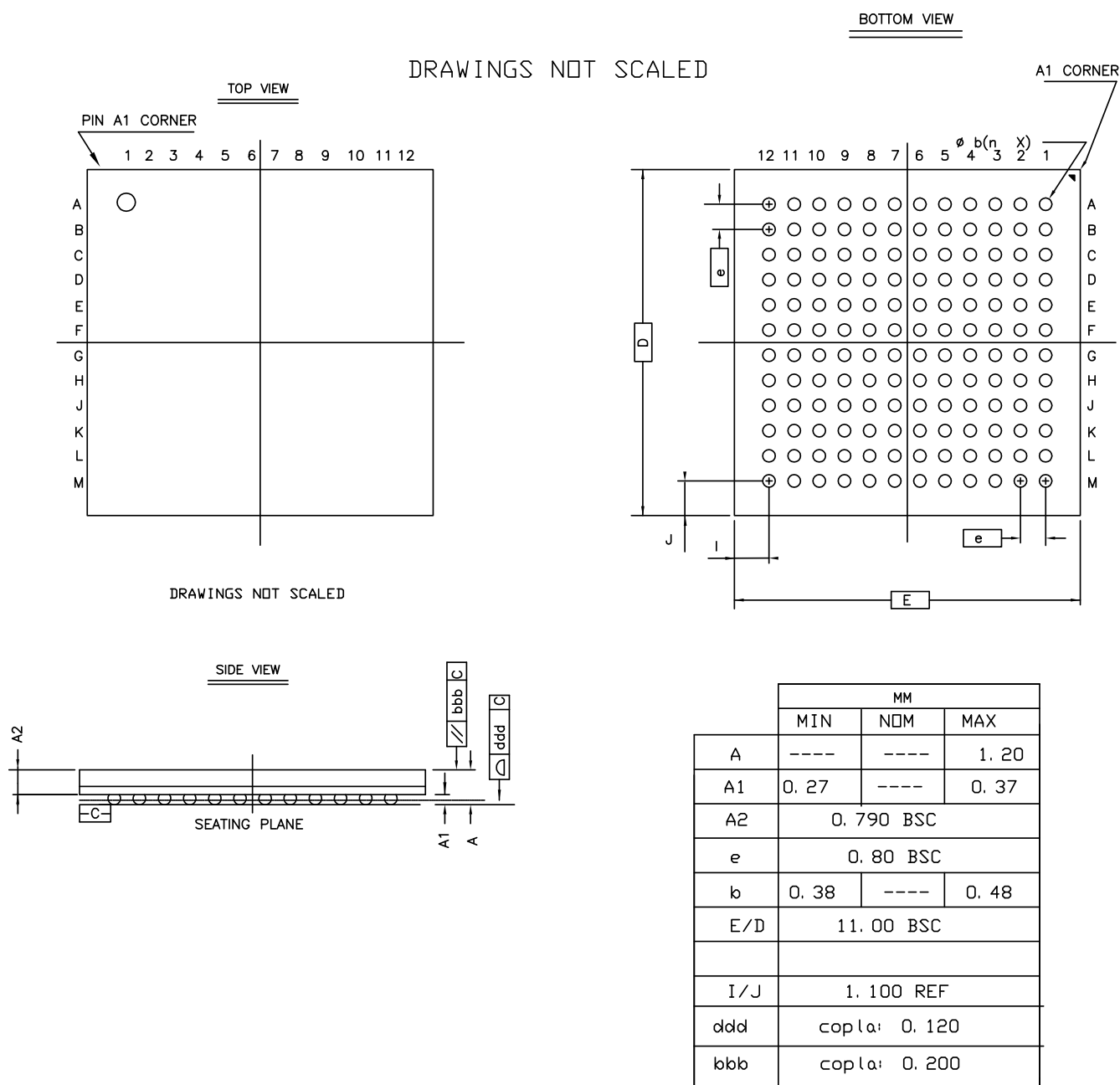
9. Ordering Information

Device	Ordering Code	Package	Conditioning	Temperature Operating Range
AT32UC3A3256S	AT32UC3A3256S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3256S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3256	AT32UC3A3256-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3256-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3256-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3128S	AT32UC3A3128S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3128S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A3128	AT32UC3A3128-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A3128-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A3128-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A364S	AT32UC3A364S-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364S-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A364S-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364S-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A364	AT32UC3A364-ALUT	144-lead LQFP	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364-ALUR	144-lead LQFP	Reels	Industrial (-40·C to 85·C)
	AT32UC3A364-CTUT	144-ball TFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A364-CTUR	144-ball TFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4256S	AT32UC3A4256S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4256S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4256	AT32UC3A4256-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4256-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4128S	AT32UC3A4128S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4128S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A4128	AT32UC3A4128-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A4128-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A464S	AT32UC3A464S-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A464S-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)
AT32UC3A464	AT32UC3A464-C1UT	100-ball VFBGA	Tray	Industrial (-40·C to 85·C)
	AT32UC3A464-C1UR	100-ball VFBGA	Reels	Industrial (-40·C to 85·C)

10.2.16 FLASHC

Corrupted read in flash may happen after fuses write or erase operations (FLASHC LP, UP, WGPB, EGPB, SSB, PGPFB, EAGPF commands)
After a flash fuse write or erase operation (FLASHC LP, UP, WGPB, EGPB, SSB, PGPFB, EAGPF commands), reading (data read or code fetch) in flash may fail. This may lead to an exception or to other errors derived from this corrupted read access.
Fix/Workaround
Before the flash fuse write or erase operation, enable the flash high speed mode (FLASHC HSEN command). The flash fuse write or erase operations (FLASHC LP, UP, WGPB, EGPB, SSB, PGPFB, EAGPF commands) must be issued from RAM or through the EBI. After these commands, read 3 times one flash page initialized to 00h. Disable the flash high speed mode (FLASHC HSDIS command). It is then possible to safely read or code fetch the flash.

10.3 Rev. D

10.3.1 General

Devices cannot operate with CPU frequency higher than 66MHz in 1WS and 36MHz in 0WS
Fix/Workaround
None

DMACA data transfer fails when CTLx.SRC_TR_WIDTH is not equal to CTLx.DST_TR_WIDTH
Fix/Workaround
For any DMACA transfer make sure CTLx.SRC_TR_WIDTH = CTLx.DST_TR_WIDTH.

3.3V supply monitor is not available
FGPFRLO[30:29] are reserved and should not be used by the application.
Fix/Workaround
None.

Service access bus (SAB) can not access DMACA registers
Fix/Workaround
None.

10.3.2 Processor and Architecture

LDM instruction with PC in the register list and without ++ increments Rp
For LDM with PC in the register list: the instruction behaves as if the ++ field is always set, ie the pointer is always updated. This happens even if the ++ field is cleared. Specifically, the increment of the pointer is done in parallel with the testing of R12.
Fix/Workaround
None.

Hardware breakpoints may corrupt MAC results
Hardware breakpoints on MAC instructions may corrupt the destination register of the MAC instruction.
Fix/Workaround
Place breakpoints on earlier or later instructions.

10.3.7 SPI

SPI disable does not work in SLAVE mode
SPI disable does not work in SLAVE mode.
Fix/Workaround
Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0
When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
Fix/Workaround
When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0
When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
Fix/Workaround
Disable mode fault detection by writing a one to MR.MODFDIS.

Disabling SPI has no effect on the SR.TDRE bit
Disabling SPI has no effect on the SR.TDRE bit whereas the write data command is filtered when SPI is disabled. Writing to TDR when SPI is disabled will not clear SR.TDRE. If SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR until its buffer is empty, and this data will be lost.
Fix/Workaround
Disable the PDCA, add two NOPs, and disable the SPI. To continue the transfer, enable the SPI and PDCA.

10.3.8 Power Manager

OSC32 not functionnal in Crystal Modes (OSC32CTRL.MODE=1 or OSC32CTRL.MODE=2)
OSC32 clock output is not active even if the oscillation signal is present on XIN32/XOUT32 pins.
OSC32RDY bit may still set even if the CLK32 is not active.
External clock mode (OSC32CTRL.MODE=0) is not affected.

Fix/Workaround
None.

Clock sources will not be stopped in STATIC sleep mode if the difference between CPU and PBx division factor is too high
If the division factor between the CPU/HSB and PBx frequencies is more than 4 when going to a sleep mode where the system RC oscillator is turned off, then high speed clock sources will not be turned off. This will result in a significantly higher power consumption during the sleep mode.
Fix/Workaround
Before going to sleep modes where the system RC oscillator is stopped, make sure that the factor between the CPU/HSB and PBx frequencies is less than or equal to 4.

10.3.9 PDCA

PCONTROL.CHxRES is non-functional
PCONTROL.CHxRES is non-functional. Counters are reset at power-on, and cannot be reset by software.
Fix/Workaround
Software needs to keep history of performance counters.

Transfer error will stall a transmit peripheral handshake interface
If a transfer error is encountered on a channel transmitting to a peripheral, the peripheral handshake of the active channel will stall and the PDCA will not do any more transfers on the affected peripheral handshake interface.
Fix/Workaround
Disable and then enable the peripheral after the transfer error.

10.3.10 AES

URAD (Unspecified Register Access Detection Status) does not detect read accesses to the write-only KEYW[5..8]R registers
Fix/Workaround
None.

10.3.11 HMATRIX

In the PRAS and PRBS registers, the MxPR fields are only two bits
In the PRAS and PRBS registers, the MxPR fields are only two bits wide, instead of four bits. The unused bits are undefined when reading the registers.
Fix/Workaround
Mask undefined bits when reading PRAS and PRBS.

10.3.12 TWIM

TWIM SR.IDLE goes high immediately when NAK is received
When a NAK is received and there is a non-zero number of bytes to be transmitted, SR.IDLE goes high immediately and does not wait for the STOP condition to be sent. This does not cause any problem just by itself, but can cause a problem if software waits for SR.IDLE to go high and then immediately disables the TWIM by writing a one to CR.MDIS. Disabling the TWIM causes the TWCK and TWD pins to go high immediately, so the STOP condition will not be transmitted correctly.
Fix/Workaround
If possible, do not disable the TWIM. If it is absolutely necessary to disable the TWIM, there must be a software delay of at least two TWCK periods between the detection of SR.IDLE==1 and the disabling of the TWIM.

TWIM TWALM polarity is wrong
The TWALM signal in the TWIM is active high instead of active low.
Fix/Workaround
Use an external inverter to invert the signal going into the TWIM. When using both TWIM and TWIS on the same pins, the TWALM cannot be used.

10.3.13 TWIS

TWIS Version Register reads zero
TWIS Version Register (VR) reads zero instead of 0x112.