Lattice Semiconductor Corporation - ICE40UL1K-CM36AI Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	156
Number of Logic Elements/Cells	1248
Total RAM Bits	57344
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40ul1k-cm36ai

- **Flexible Device Configuration**
  - SRAM is configured through:
    - — Standard SPI Interface
    - — Internal Nonvolatile Configuration Memory (NVCM)
- **Ultra-Small Form Factor**
  - As small as 1.409 mm x 1.409 mm
- **Applications**
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Industrial Devices
  - Multi Sensor Management Applications
  - IR remote, Barcode emulator
  - RGB light control

Table 1-1. iCE40 UltraLite Family Selection Guide

Part Number	iCE40UL-640	iCE40UL-1K
Logic Cells (LUT + Flip-Flop)	**640**	**1248**
EBR Memory Blocks	14	14
EBR Memory Bits	56 k	56 k
PLL Block[1]	1	1
Hardened I2C	2	2
Hardened IR TX/RX	1	1
Hardened RGB PWM IP	1	1
HF Oscillator (48 MHz)	1	1
LF Oscillator (10 kHz)	1	1
24 mA LED Sink	3	3
100 mA LED Sink	1	1
400 mA LED Sink	1	1
Packages, ball pitch, dimension	**Programmable I/O Count**	
16-ball WLCSP, 0.35 mm, 1.409 mm x 1.409 mm	10	10
36-ball ucBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26

1. Only in 36-ball ucBGA package.

Introduction

The iCE40 UltraLite devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as user configurable RGB LED and IR LED Controllers, and two Oscillators.

The iCE40 UltraLite FPGAs are available in very small form factor packages, as small as 1.409 mm x 1.409 mm. The small form factor allows the device to easily fit into a lot of mobile applications. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40 UltraLite devices offer I/O features such as programmable multiple value pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 UltraLite devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 UltraLite family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 UltraLite. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 UltraLite device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

sysCLOCK Phase Locked Loops (PLLs) *(sysCLOCK PLL is only supported in 36-ball ucBGA package)*

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraLite devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraLite global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraLite PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

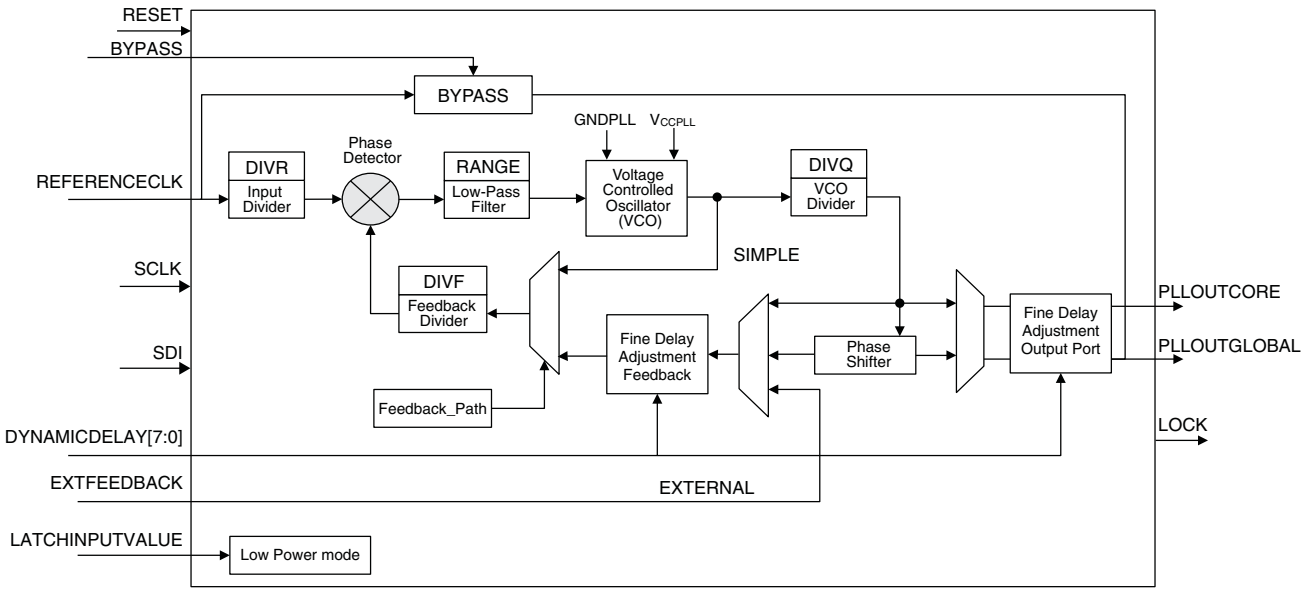


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 UltraLite device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

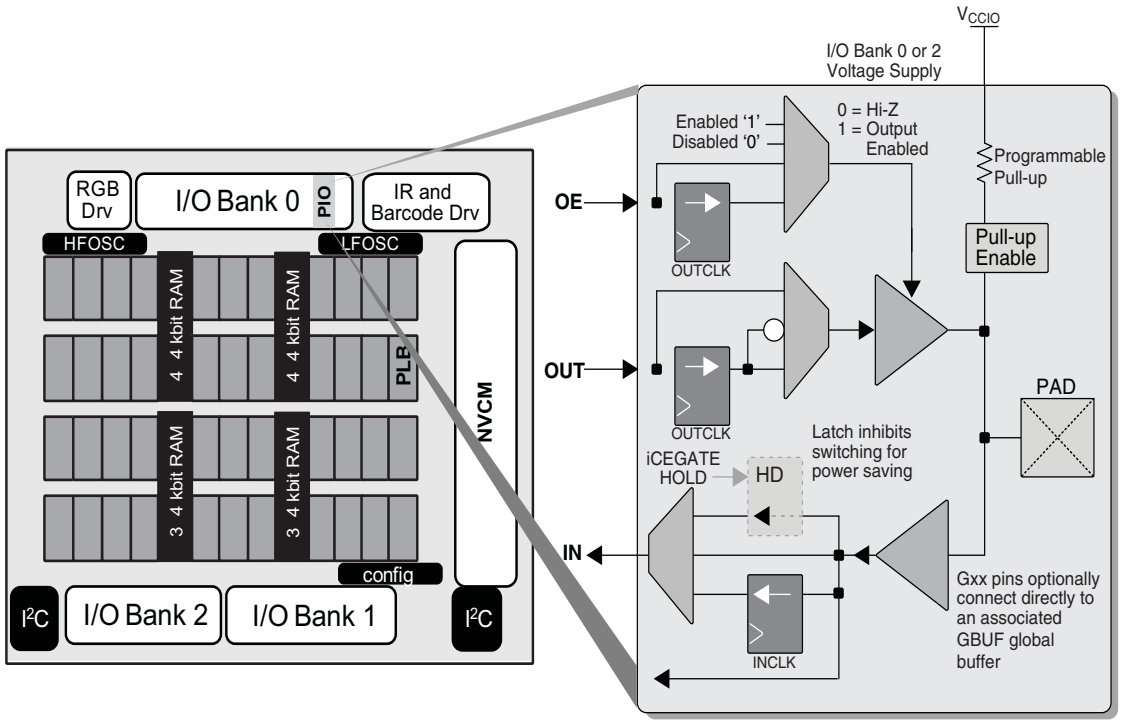
sysIO Buffer Banks

iCE40 UltraLite devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. On the 16 WLCSP package, V_{CCIO1} and V_{PP_2V5} are connected to the same pin on the package, and must meet the voltage requirement of both supplies. Please refer to the Pin Information Summary table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-5. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-6 shows the input/output register block for the PIOs.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO}, and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics chapter of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO}, and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 UltraLite sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 UltraLite devices.

Programmable Pull Up Resistors

The iCE40 UltraLite sysIO buffer can be configured with programmable pull up resistors on every I/O. The options are 3.3 kOhms, 6.8 kOhms, 10 kOhms or 100 kOhms (default). This feature is useful in supporting the I^2C interface. The user can also use it for other purposes.

Differential Comparators

The iCE40 UltraLite devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the Pin Information Summary section to locate the corresponding paired I/Os with differential comparators.

Table 2-7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes		
LVCMOS25		Yes	
LVCMOS18[1]			Yes

1. Not supported in bank 0 for 16-WLCP package.

Table 2-8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18[1]	1.8 V

1. Not supported in bank 0 for 16-WLCP package.

On-Chip Oscillator

The iCE40 UltraLite devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz, by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

User I²C IP

The iCE40 UltraLite devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components.

In optional FIFO mode, FIFOs are used for storing multiple bytes of data for transmit and / or receive in order to efficiently support the I²C sensor applications

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

High Current LED Drive I/O Pins

The iCE40 UltraLite family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 UltraLite product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA in full current mode or from 2 mA to 12 mA, in increments of 2 mA in half current mode. This output functions as General Purpose I/O with open-drain when the high current drive is not needed.

There is one output on each device that can sink up to 100 mA current. This output is open-drain, and provides sinking current to drive an external Barcode LED connecting to the positive supply. This Barcode drive current is user programmable from 16.6 mA to100 mA in increments of 16.6 mA in full current mode or 8.3 mA to 50 mA in

increments of 8.3 mA in half current mode. This output functions as General Purpose I/O with open drain when the high current drive is not needed.

There is one output on each device that can sink up to 400 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 400 mA in increments of 50 mA in full current mode or from 25mA to 200mA in increments of 25mA in half current mode. This output functions as General Purpose I/O with open-drain when the high current drive is not needed. This output pin can also bond together with the Barcode output to drive higher current for IR LED.

The 400 mA IR LED drive output and the 100 mA Barcode LED drive output can be connected together to drive up to 500 mA IR LED, if higher than 400 mA driving capability is needed.

Table 2-9 shows the different LED driving current in the different selected Current Modes. IR500 LED applies with both IR LED and Barcode LED pins connected together.

Table 2-9. Current Drive

	Full Current Mode		Half Current Mode	
	mA (V_{CCIO}= 3.3 V)	mA (V_{CCIO}=2.5 V)	mA (V_{CCIO}= 3.3 V)	mA (V_{CCIO}=2.5 V)
RGB LED	0, 4, 8, 12, 16, 20, 24	not allowed	0, 2, 4, 6, 8, 10, 12	0, 2, 4, 6, 8, 10, 12
BARCODE LED	0, 16.6, 33.3, 50, 66.6, 83.3, 100	not allowed	0, 8.3, 16.6, 25, 33.3, 41.6, 50	not allowed
IR400 LED	0, 50, 100, 150, 200, 250, 300, 350, 400	not allowed	0, 25, 50, 75, 100, 125, 150, 175, 200	0, 25, 50, 75, 100, 125, 150, 175, 200
IR500 LED	0, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500	not allowed	0, 25, 50, 75, 100, 125, 150, 175, 200, 225, 250	0,25, 50, 75, 100, 125, 150, 175, 200, 225, 250

Hardened RGB PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the PWM IP, please refer to TN1288, iCE40 LED Driver Usage Guide.

Hardened IR Transceiver IP

The IR Transceiver hard IP provides logic function to transmit and receive data through the Infrared LED data link. It takes the data residing inside the FPGA fabric to transmit with user specified frequency. In user enabled learning mode, it receives data from Infrared receiver and send the received data back to the FPGA fabric along with the measured receiving frequency.

For additional information on IR Transceiver IP, please see TN1288, iCE40 LED Driver Usage Guide.

Non-Volatile Configuration Memory

All iCE40 UltraLite devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration.

Power On Reset

iCE40 UltraLite devices have power-on reset circuitry to monitor V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} voltage levels during power-up and operation. At power-up, the POR circuitry monitors these voltage levels. It then triggers

download from either the internal NVCM or the external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

iCE40 UltraLite Programming and Configuration

This section describes the programming and configuration of the iCE40 UltraLite family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO01} power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 UltraLite, please see TN1248, iCE40 Programming and Configuration.

Power Saving Options

The iCE40 UltraLite devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 UltraLite Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

iCE40 UltraLite Family Data Sheet DC and Switching Characteristics

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Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.30 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10	30	°C

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to Power-Up Supply Sequencing section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR / Barcode LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power-up sequence must be followed. Please refer to Power-Up Supply Sequencing section.

Power-On Reset

All iCE40 UltraLite devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) V_{CC}, (2) SPI_V_{CCIO1} and (3) V_{PP_2V5}. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

Power-Up Supply Sequencing

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5V, or higher, before any subsequent power supplies in the sequence are applied.

1. **V_{CC}** and **V_{CCPLL}** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the V_{CCPLL} (Please refer to TN1252, iCE40 Hardware Checklist.)

2. **SPI_V_{CCIO1}** should be the next supply, and can be applied any time after the previous supplies (V_{CC} and V_{CCPLL}) have reached as level of 0.5 V or higher.

3. **V_{PP_2V5}** should be the next supply, and can be applied any time after previous supplies (V_{CC}, V_{CCPLL} and SPI_V_{CCIO1}) have reached a level of 0.5 V or higher.

4. **Other Supplies** (V_{CCIO0} and V_{CCIO2}) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (V_{CC} and V_{CCPLL}) have reached a level of 0.5 V or greater. *On the 16*

Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.6	1	V
		SPI_V_{CCIO1}	0.7	1.6	V
		V_{PP_2V5}	0.7	1.6	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.85	V
		SPI_V_{CCIO1}	—	1.6	V
		V_{PP_2V5}	—	1.6	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2$ V	—	—	+/–10	µA
C_1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_3	24 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
C_4	400 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	53	—	pf
C_5	100 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	–3	—	–31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	–8	—	–72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

Maximum sysIO Buffer Performance[1]

I/O Standard	Max. Speed	Units
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
LED I/O used as GPIO open drain	50	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz
LED I/O used as GPIO open drain	50[2]	MHz

1. Measured with a toggling pattern.
2. With external resistor from 180 Ohm to 250 Ohm and capacity of no more than 15 pF.

iCE40 UltraLite External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	Min	Max	Units
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	2	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	500	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[1]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All devices	—	410	ps
t_{CO}	Clock to Output - PIO Output Register	All devices	—	9.0	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All devices	–0.5	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	All devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output - PIO Output Register	All Devices	—	2.9	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	7.9	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	–0.6	—	ns

1. All the data is from the worst case condition.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	µs
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices - Low Frequency (Default)	53	ms
		All devices - Medium frequency	25	ms
		All devices - High frequency	13	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

High Current LED, IR LED and Barcode LED Drives[1]

Symbol	Parameter	VCCIO = 3.3 V			VCCIO = 2.5 V		
		Min.	Max.	Units	Min.	Max.	Units
$I_{RGB\_ACCURACY\_FULL}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.5 ~ 2.5 V	–12	+12	%	not allowed	not allowed	%
$I_{RGB\_ACCURACY\_HALF}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.35 ~ 2.5 V	–14	+14	%	–14	+14	%
I_{RGB_MATCH}	RGB LED0, LED1, LED2 Sink Current Matching among the 3 outputs @ V_{PAD} = 0.35 ~ 2.5 V	–5	+5	%	–5	+5	%
$I_{IR\_ACCURACY\_FULL}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{IR\_ACCURACY\_HALF}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	–12	+12	%
$I_{BARCODE\_ACCURACY\_FULL}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{BARCODE\_ACCURACY\_HALF}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	not allowed	not allowed	%

1. Refer to Table 2-9 for valid current settings.

RGB LED Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	$F_{PWM\_OUT\_X}$ FR_{250} = 0	Frequency of the PWM output for color LED; When FR_{250} = 0		125		Hz
2	$F_{PWM\_OUT\_X}$ FR_{250} = 1	Frequency of the PWM output for color LED; When FR_{250} = 1		250		Hz
3	T_{HIGH_X}	PWM High percentage for color LED.	0		99	%
4	$T_{HIGH\_STEP\_X}$	PWM High percentage incremental step.		1/256		%

IR Transceiver IP Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	F_{IR_OUT}	Frequency of the IR output	25		120	kHz
2	F_{IR_IN}	Frequency of the IR input	25		120	kHz
3	$T_{HIGH\ (DUTY1/3\ =\ 0)}$	Duty Cycle when DUTY1/3 = 0.		50		%
4	$T_{HIGH\ (DUTY1/3\ =\ 1)}$	Duty Cycle when DUTY1/3 = 1.		33.33		%

Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-1.

Figure 3-3. Output Test Load, LVCMOS Standards

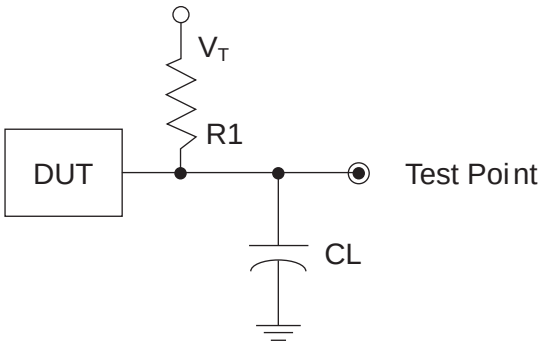

Table 3-1. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15 V	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

PIOB_15b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_17b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_22b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer.
PIOT_21a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer.
PIOB_13b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer.
PIOB_8a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer.
PIOB_7b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer.
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer.
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.

RGB2	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
IRLED	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 400 mA output to drive external LED.
BARCODE	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 100 mA output to drive external LED.
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location).
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location).

iCE40 UltraLite Family Data Sheet Revision History

November 2016 **Data Sheet DS1050**

Date	Version	Section	Change Summary
November 2016	1.4	DC and Switching Characteristics	Updated External Reset section. Added information on following supply sequence.
June 2016	1.3	Introduction	Updated General Description section. — Changed “embedded RGB PWM IP” to ”hardened RGB PWM IP”. — Changed “modulation logic” to “hardened TX/RX pulse logic”. — Updated information on the use of 500 mA IR driver.
			Updated Introduction section. — Added “RGB LED and IR LED” to configurable Controllers. — Added “LED” to RGB control functions.
		Architecture	Updated Architecture Overview section. — Changed caption to Figure 2-1, iCE40UL1K iCE40UL-1K Device, Top View. — Changed logic blocks to PLB. — Changed “LED sink” to “RGB and IR LED sinks, and a 100 mA Bar-code emulation output”. — Corrected headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. — Updated footnote in Table 2-4, sysMEM Block Configuration. — Updated sysIO Buffer Banks section. — Corrected V_{CCIO} format in Figure 2-5, I/O Bank and Programmable I/O Cell. — Updated Typical I/O Behavior During Power-up section. — Updated Supported Standards section. — Updated Programmable Pull Up Resistors section. — Changed “more than one byte” to “multiple bytes” in User I^2C IP section. — Updated High Current LED Drive I/O Pins section. Changed heading to High Current LED Drive I/O Pins. Added LED to “high current drive”. Added information on use of 500 mA IR LED. Added paragraph to reference Table 2-9. — Changed heading to Hardened RGB PWM IP. — Changed heading to Hardened IR Transceiver IP.
			Updated iCE40 UltraLite Programming and Configuration section. Changed VCCIO_1 to SPI_V_{CCIO1} in Device Programming.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Corrected V_{PP_2V5} and V_{CCPLL} format.
			Updated Recommended Operating Conditions section. — Changed heading to Hardened RGB PWM IP. — Updated footnote.
			Removed Power-up Sequence section.
			Added the following sections: — Power-On Reset — Power-Up Supply Sequencing — External Reset
			Updated DC Electrical Characteristics section. Revised footnote 4.
			Updated Supply Current section. — Changed V_{PP_2V5} format. — Updated footnote 5.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for f_{CLKHF} and DCH_{CLKHF}.
			Updated Differential Comparator Electrical Characteristics section.

Date	Version	Section	Change Summary
			Updated iCE40 UltraLite External Switching Characteristics section. Revised footnote.
			Updated sysCLOCK PLL Timing section. Revised t_{OPJIT} conditions.
			Updated sysCONFIG Port Timing Specifications section. — Added footnote to Master SPI. — Added footnote to MCLK setup time. — Revised t_{MTSU} minimum value. — Added footnotes 3 and 4.
		Supplemental Information	Updated For Further Information section. Added reference to TN1252, iCE40 Hardware Checklist.
April 2016	1.2	Introduction	Updated Features section. — Updated BGA package to ucBGA. — Corrected HF Oscillator unit in Table 1-1, iCE40 UltraLite Family Selection Guide.
		Architecture	Updated sysCLOCK Phase Locked Loops (PLLs) (sysCLOCK PLL is only supported in 36-ball ucBGA package) section. Updated BGA package to ucBGA in heading.
		DC and Switching Characteristics	Updated Recommended Operating Conditions section. Added footnote 4 regarding V_{PP_2V5}.
		Pinout Information	Updated Signal Descriptions and Pin Information Summary sections. — Updated BGA package to ucBGA. — Changed SPI_CSN to SPI_SS_B. — Corrected minor typo errors.
		Ordering Information	Updated iCE40 UltraLite Part Number Description section. — Added shipment types. — Updated BGA package to ucBGA.
			Added Tape and Reel Quantity section.
			Updated Ordering Part Numbers section. — Added part numbers. — Updated BGA package to ucBGA.
March 2015	1.1	All	Document status changed from Preliminary to Final.
		Introduction	Updated General Description and Features sections. Changed the LFOSC frequency value from 9.7 kHz to 10 kHz.
		Architecture	Updated On-Chip Oscillator section. Changed the LFOSC frequency value from 9.7 kHz to 10 kHz.
		DC and Switching Characteristics	Updated Power-up Sequence section. Revised power-up sequence description for 16-ball WLCSP. Added Power-up Sequence table.
			Updated User I2C Specifications section. Added footnote 2.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added and revised values. Removed footnote.
			Updated Maximum sysIO Buffer Performance section. Revised value for LED I/O used as GPIO open drain.
			Updated High Current LED, IR LED and Barcode LED Drives[1] section. Revised values.
January 2015	1.0	All	Initial release.