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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	57344
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40ul640-cm36ai

iCE40 UltraLite Family Data Sheet Introduction

July 2016 Data Sheet DS1050

General Description

iCE40 UltraLite family is an optimum logic, smallest footprint, low I/O count ultra-low power FPGA and sensor manager with instant on capability. It is designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 UltraLite family includes integrated blocks to interface with virtually all mobile sensors and application processors. The iCE40 UltraLite family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The hardened RGB PWM IP, with the three 24 mA constant current RGB LED outputs on the iCE40 UltraLite provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 400 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the hardened TX/RX pulse logic that meets their needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. The 100 mA Barcode Emulation driver output provides a direct interface for applications such as barcode scanning. The 100 mA and 400 mA drivers can also be combined to be used as a 500 mA IR driver if higher than 400 mA current drive is required.

The iCE40 UltraLite family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 UltraLite family features two device densities of 640 or 1K Look Up Tables (LUTs) of logic with programmable I/Os that can be used as an interface port or general purpose I/O. It also has up to 56 kbits of Block RAMs to work with user logic.

Features

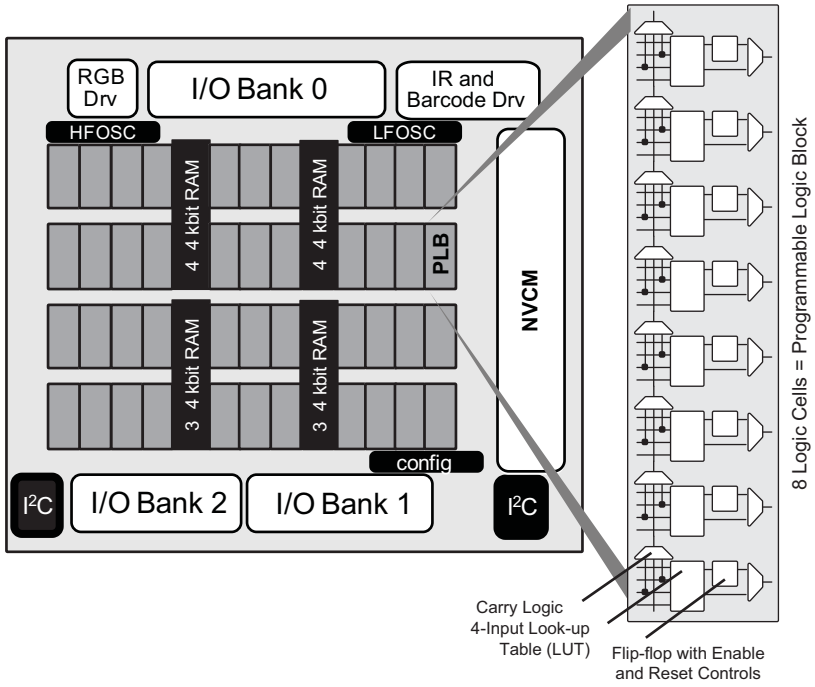
- **Flexible Logic Architecture**
  - Two devices with 640 or 1K LUTs
  - Offered in 16-ball WLCSP package
  - Offered in 36-ball ucBGA package
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - Typical 35 µA standby current which equals 42 uW standby power consumption
- **Embedded and Distributed Memory**
  - Up to 56 kbits sysMEM™ Embedded Block RAM
- **Two Hardened Interfaces**
  - Two optional FIFO mode I^2C interface up to 1 MHz
  - Either master or slave
- **Two On-Chip Oscillators**
  - Low Frequency Oscillator - 10 kHz
  - High Frequency Oscillator - 48 MHz
- **Hardened PWM circuit for RGB**
- **Hardened TX/RX Pulse Logic circuit for IR LED**
- **24 mA Current Drive RGB LED Outputs**
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- **400 or 500 mA Current Drive IR LED Output**
  - One IR drive output in each device
  - User selectable sink current up to 400 mA
  - Can be combined with 100 mA Barcode driver to form 500 mA IR driver
- **100 mA Current Drive Barcode Emulator**
  - One barcode driver output in each device
  - User selectable sink current up to 100 mA
  - Can be combined with 400 mA IR driver to use as 500 mA IR driver
- **Flexible On-Chip Clocking**
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device

iCE40 UltraLite Family Data Sheet Architecture

Architecture Overview

The iCE40 UltraLite family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE40UL-1K device.

Figure 2-1. iCE40UL-1K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

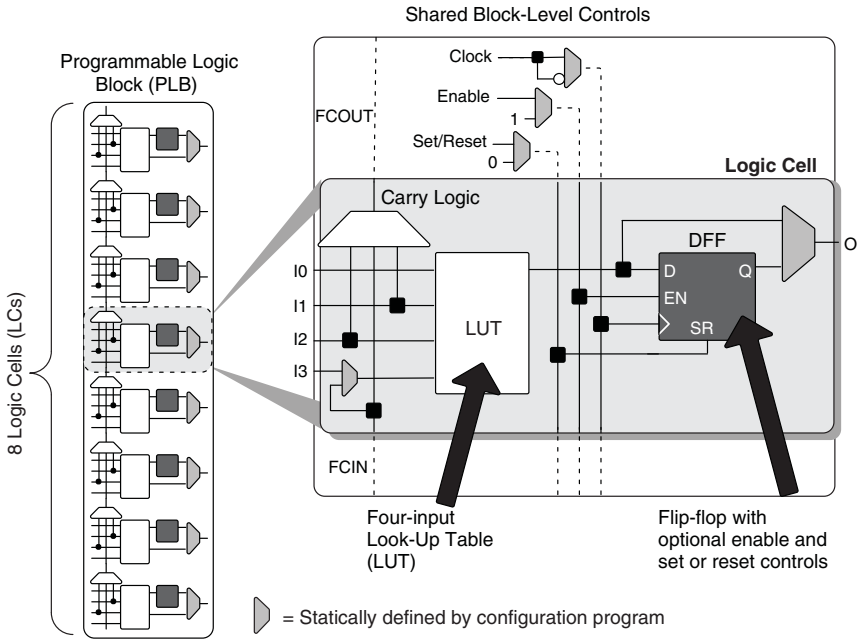
In the iCE40 UltraLite family, there are three sysIO banks, one on top and two at the bottom. User can connect all V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

The iCE40 UltraLite also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks, and a 100 mA Barcode emulation output.

PLB Blocks

The core of the iCE40 UltraLite device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

Routing

There are many resources provided in the iCE40 UltraLite devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 UltraLite device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 UltraLite External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraLite device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraLite device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysCLOCK Phase Locked Loops (PLLs) *(sysCLOCK PLL is only supported in 36-ball ucBGA package)*

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraLite devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraLite global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraLite PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

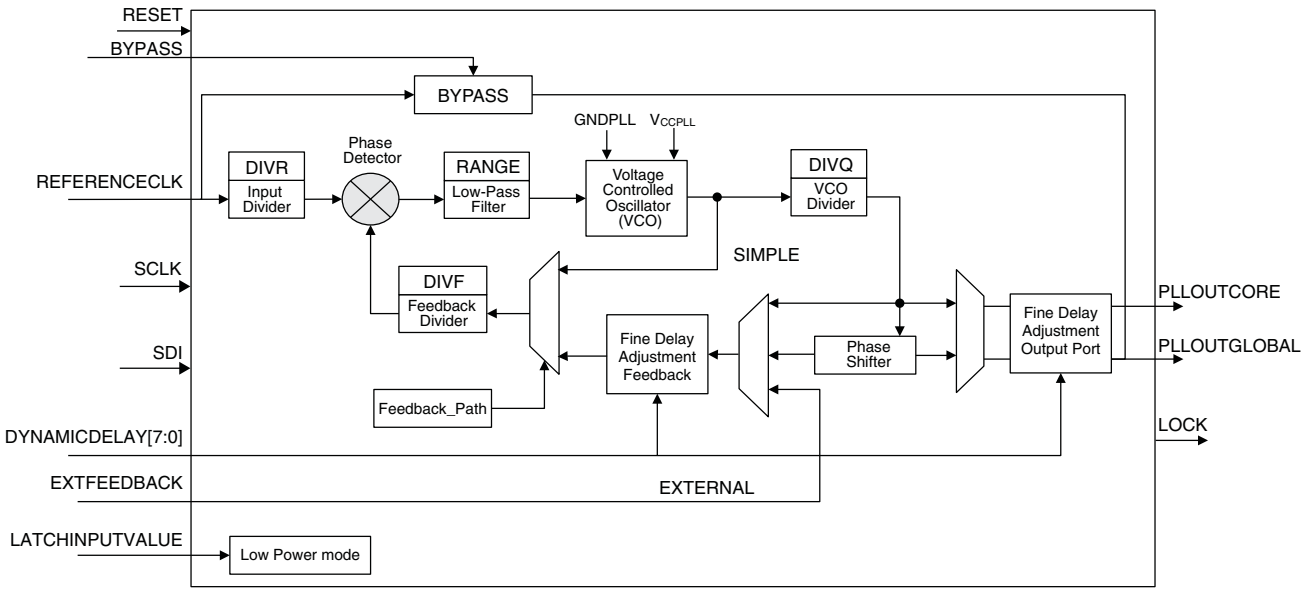


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 UltraLite device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 Ultra, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock and falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses falling-edge clocks on both Read and Write.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

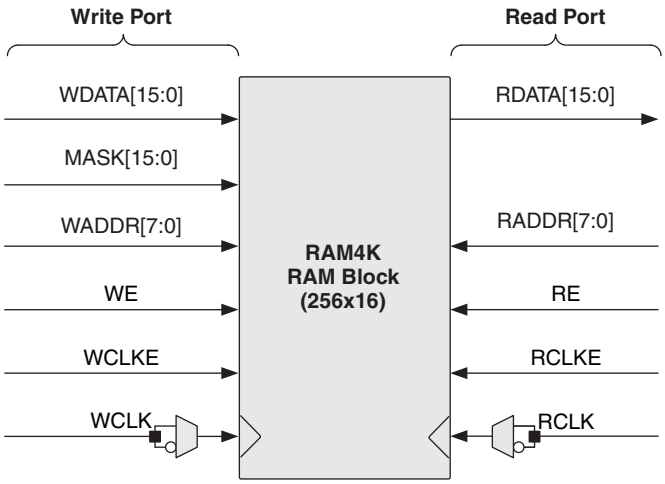


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

Figure 2-6. iCE I/O Register Block Diagram

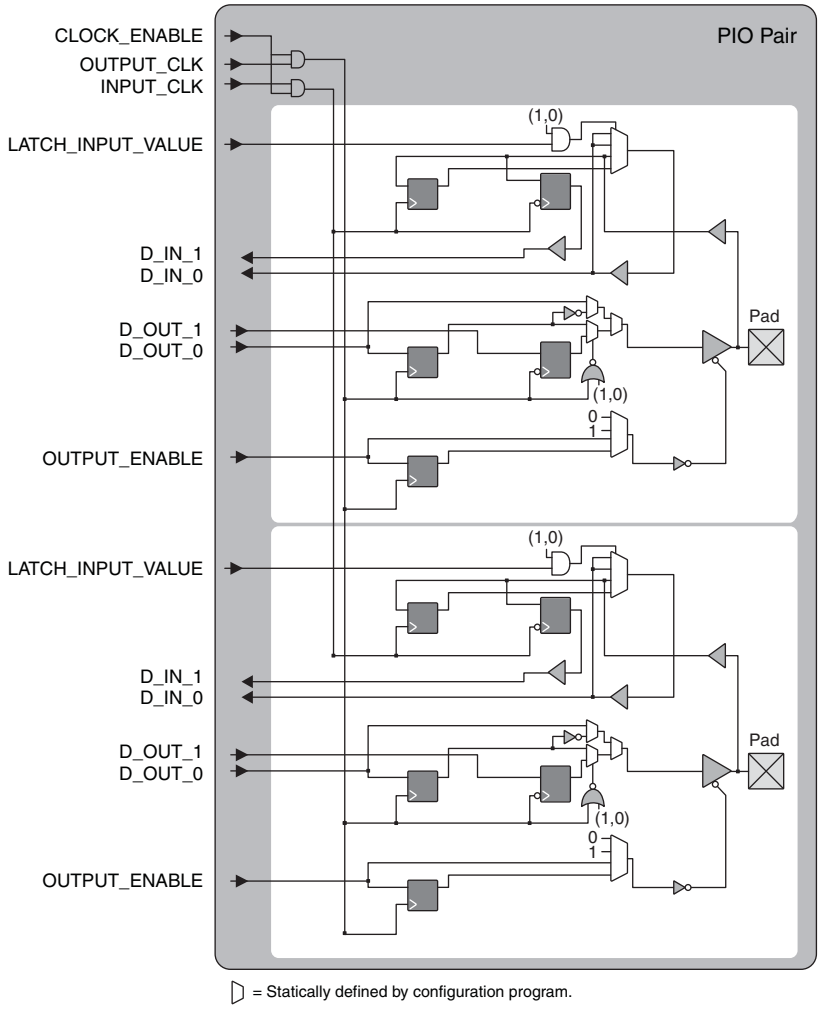


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

increments of 8.3 mA in half current mode. This output functions as General Purpose I/O with open drain when the high current drive is not needed.

There is one output on each device that can sink up to 400 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user programmable from 50 mA to 400 mA in increments of 50 mA in full current mode or from 25mA to 200mA in increments of 25mA in half current mode. This output functions as General Purpose I/O with open-drain when the high current drive is not needed. This output pin can also bond together with the Barcode output to drive higher current for IR LED.

The 400 mA IR LED drive output and the 100 mA Barcode LED drive output can be connected together to drive up to 500 mA IR LED, if higher than 400 mA driving capability is needed.

Table 2-9 shows the different LED driving current in the different selected Current Modes. IR500 LED applies with both IR LED and Barcode LED pins connected together.

Table 2-9. Current Drive

	Full Current Mode		Half Current Mode	
	mA (V_{CCIO}= 3.3 V)	mA (V_{CCIO}=2.5 V)	mA (V_{CCIO}= 3.3 V)	mA (V_{CCIO}=2.5 V)
RGB LED	0, 4, 8, 12, 16, 20, 24	not allowed	0, 2, 4, 6, 8, 10, 12	0, 2, 4, 6, 8, 10, 12
BARCODE LED	0, 16.6, 33.3, 50, 66.6, 83.3, 100	not allowed	0, 8.3, 16.6, 25, 33.3, 41.6, 50	not allowed
IR400 LED	0, 50, 100, 150, 200, 250, 300, 350, 400	not allowed	0, 25, 50, 75, 100, 125, 150, 175, 200	0, 25, 50, 75, 100, 125, 150, 175, 200
IR500 LED	0, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500	not allowed	0, 25, 50, 75, 100, 125, 150, 175, 200, 225, 250	0,25, 50, 75, 100, 125, 150, 175, 200, 225, 250

Hardened RGB PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be embedded into the user design. This PWM IP provides the flexibility for user to dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the PWM IP, please refer to TN1288, iCE40 LED Driver Usage Guide.

Hardened IR Transceiver IP

The IR Transceiver hard IP provides logic function to transmit and receive data through the Infrared LED data link. It takes the data residing inside the FPGA fabric to transmit with user specified frequency. In user enabled learning mode, it receives data from Infrared receiver and send the received data back to the FPGA fabric along with the measured receiving frequency.

For additional information on IR Transceiver IP, please see TN1288, iCE40 LED Driver Usage Guide.

Non-Volatile Configuration Memory

All iCE40 UltraLite devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration.

Power On Reset

iCE40 UltraLite devices have power-on reset circuitry to monitor V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5} voltage levels during power-up and operation. At power-up, the POR circuitry monitors these voltage levels. It then triggers

download from either the internal NVCM or the external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

iCE40 UltraLite Family Data Sheet DC and Switching Characteristics

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Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.30 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Internal Oscillators (HFOSC, LFOSC)

Parameter		Parameter Description	Spec/Recommended			Units
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	–10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t_J = –40 °C–100 °C)	–20%	48	20%	MHz
f_{CLKLF}		LFOSC CLKK clock frequency	–10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC clock frequency (t_J = –45 °C–100 °C)	40	50	60	%
DCH_{CLKLF}		LFOSC Duty Cycle (Clock High Period)	45	50	55	%
t_{WAKEUP}		Delay OSC Enable to output enable delay	—	—	100	µs
Tsync_on		Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off		Oscillator output disable delay	—	—	5	Cycles

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.4	8	–8
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 2.5	-0.3	0.7	1.7	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.4	6	–6
					0.2	V_{CCIO} - 0.2	0.1	–0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.4	4	–4
					0.2	V_{CCIO} - 0.2	0.1	–0.1

Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{REF}	Reference Voltage to compare, on V_{INM}	V_{CCIO} = 2.5 V	0.25	V_{CCIO} –0.25 V	V
V_{DIFFIN_H}	Differential input HIGH (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	250	—	mV
V_{DIFFIN_L}	Differential input LOW (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	—	–250	mV
I_{IN}	Input Current, V_{INP} and V_{INM}	V_{CCIO} = 2.5 V	–10	10	µA

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	µs
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices - Low Frequency (Default)	53	ms
		All devices - Medium frequency	25	ms
		All devices - High frequency	13	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraLite device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{MTSU}	MCLK setup time[4]		9.9	—	—	ns
t_{MTH}	MCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V VCC and at 25 C.
3. tSU and tHD timing must be met for all MCLK frequency choices
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

High Current LED, IR LED and Barcode LED Drives[1]

Symbol	Parameter	VCCIO = 3.3 V			VCCIO = 2.5 V		
		Min.	Max.	Units	Min.	Max.	Units
$I_{RGB\_ACCURACY\_FULL}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.5 ~ 2.5 V	–12	+12	%	not allowed	not allowed	%
$I_{RGB\_ACCURACY\_HALF}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.35 ~ 2.5 V	–14	+14	%	–14	+14	%
I_{RGB_MATCH}	RGB LED0, LED1, LED2 Sink Current Matching among the 3 outputs @ V_{PAD} = 0.35 ~ 2.5 V	–5	+5	%	–5	+5	%
$I_{IR\_ACCURACY\_FULL}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{IR\_ACCURACY\_HALF}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	–12	+12	%
$I_{BARCODE\_ACCURACY\_FULL}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{BARCODE\_ACCURACY\_HALF}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	not allowed	not allowed	%

1. Refer to Table 2-9 for valid current settings.

RGB LED Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	$F_{PWM\_OUT\_X}$ FR_{250} = 0	Frequency of the PWM output for color LED; When FR_{250} = 0		125		Hz
2	$F_{PWM\_OUT\_X}$ FR_{250} = 1	Frequency of the PWM output for color LED; When FR_{250} = 1		250		Hz
3	T_{HIGH_X}	PWM High percentage for color LED.	0		99	%
4	$T_{HIGH\_STEP\_X}$	PWM High percentage incremental step.		1/256		%

IR Transceiver IP Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	F_{IR_OUT}	Frequency of the IR output	25		120	kHz
2	F_{IR_IN}	Frequency of the IR input	25		120	kHz
3	$T_{HIGH\ (DUTY1/3\ =\ 0)}$	Duty Cycle when DUTY1/3 = 0.		50		%
4	$T_{HIGH\ (DUTY1/3\ =\ 1)}$	Duty Cycle when DUTY1/3 = 1.		33.33		%

PIOB_15b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_17b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_22b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer.
PIOT_21a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer.
PIOB_13b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer.
PIOB_8a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer.
PIOB_7b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer.
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer.
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.

RGB2	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
IRLED	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 400 mA output to drive external LED.
BARCODE	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 100 mA output to drive external LED.
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location).
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location).

iCE40 UltraLite Family Data Sheet Supplemental Information

July 2016 **Data Sheet DS1050**

For Further Information

A variety of technical notes for the iCE40 UltraLite family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1274, iCE40 I2C and SPI Hardened IP Usage Guide
- TN1276, Advanced iCE40 I2C and SPI Hardened IP Usage Guide
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- TN1252, iCE40 Hardware Checklist
- TN1288, iCE40 LED Driver Usage Guide
- iCE40 UltraLite Pinout Files
- iCE40 UltraLite Pin Migration Files
- Thermal Management document
- Lattice design tools
- Schematic Symbols

iCE40 UltraLite Family Data Sheet Revision History

November 2016 **Data Sheet DS1050**

Date	Version	Section	Change Summary
November 2016	1.4	DC and Switching Characteristics	Updated External Reset section. Added information on following supply sequence.
June 2016	1.3	Introduction	Updated General Description section. — Changed “embedded RGB PWM IP” to ”hardened RGB PWM IP”. — Changed “modulation logic” to “hardened TX/RX pulse logic”. — Updated information on the use of 500 mA IR driver.
			Updated Introduction section. — Added “RGB LED and IR LED” to configurable Controllers. — Added “LED” to RGB control functions.
		Architecture	Updated Architecture Overview section. — Changed caption to Figure 2-1, iCE40UL1K iCE40UL-1K Device, Top View. — Changed logic blocks to PLB. — Changed “LED sink” to “RGB and IR LED sinks, and a 100 mA Bar-code emulation output”. — Corrected headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. — Updated footnote in Table 2-4, sysMEM Block Configuration. — Updated sysIO Buffer Banks section. — Corrected V_{CCIO} format in Figure 2-5, I/O Bank and Programmable I/O Cell. — Updated Typical I/O Behavior During Power-up section. — Updated Supported Standards section. — Updated Programmable Pull Up Resistors section. — Changed “more than one byte” to “multiple bytes” in User I^2C IP section. — Updated High Current LED Drive I/O Pins section. Changed heading to High Current LED Drive I/O Pins. Added LED to “high current drive”. Added information on use of 500 mA IR LED. Added paragraph to reference Table 2-9. — Changed heading to Hardened RGB PWM IP. — Changed heading to Hardened IR Transceiver IP.
			Updated iCE40 UltraLite Programming and Configuration section. Changed VCCIO_1 to SPI_V_{CCIO1} in Device Programming.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Corrected V_{PP_2V5} and V_{CCPLL} format.
			Updated Recommended Operating Conditions section. — Changed heading to Hardened RGB PWM IP. — Updated footnote.
			Removed Power-up Sequence section.
			Added the following sections: — Power-On Reset — Power-Up Supply Sequencing — External Reset
			Updated DC Electrical Characteristics section. Revised footnote 4.
			Updated Supply Current section. — Changed V_{PP_2V5} format. — Updated footnote 5.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for f_{CLKHF} and DCH_{CLKHF}.
			Updated Differential Comparator Electrical Characteristics section.