Lattice Semiconductor Corporation - ICE40UL640-CM36AITR Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	57344
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40ul640-cm36aitr

iCE40 UltraLite Family Data Sheet Introduction

July 2016 Data Sheet DS1050

General Description

iCE40 UltraLite family is an optimum logic, smallest footprint, low I/O count ultra-low power FPGA and sensor manager with instant on capability. It is designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 UltraLite family includes integrated blocks to interface with virtually all mobile sensors and application processors. The iCE40 UltraLite family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The hardened RGB PWM IP, with the three 24 mA constant current RGB LED outputs on the iCE40 UltraLite provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 400 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the hardened TX/RX pulse logic that meets their needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. The 100 mA Barcode Emulation driver output provides a direct interface for applications such as barcode scanning. The 100 mA and 400 mA drivers can also be combined to be used as a 500 mA IR driver if higher than 400 mA current drive is required.

The iCE40 UltraLite family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 UltraLite family features two device densities of 640 or 1K Look Up Tables (LUTs) of logic with programmable I/Os that can be used as an interface port or general purpose I/O. It also has up to 56 kbits of Block RAMs to work with user logic.

Features

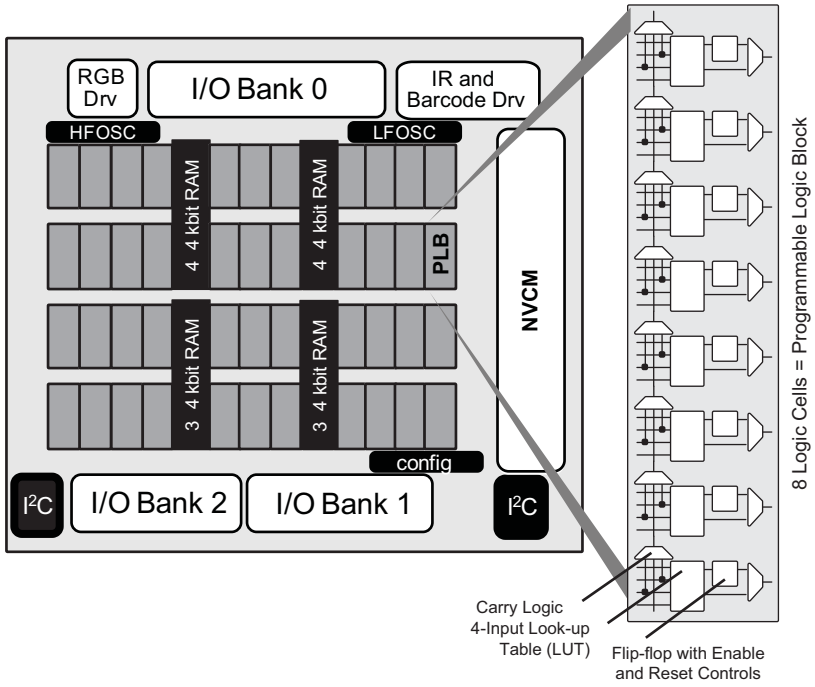
- **Flexible Logic Architecture**
  - Two devices with 640 or 1K LUTs
  - Offered in 16-ball WLCSP package
  - Offered in 36-ball ucBGA package
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - Typical 35 µA standby current which equals 42 uW standby power consumption
- **Embedded and Distributed Memory**
  - Up to 56 kbits sysMEM™ Embedded Block RAM
- **Two Hardened Interfaces**
  - Two optional FIFO mode I^2C interface up to 1 MHz
  - Either master or slave
- **Two On-Chip Oscillators**
  - Low Frequency Oscillator - 10 kHz
  - High Frequency Oscillator - 48 MHz
- **Hardened PWM circuit for RGB**
- **Hardened TX/RX Pulse Logic circuit for IR LED**
- **24 mA Current Drive RGB LED Outputs**
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- **400 or 500 mA Current Drive IR LED Output**
  - One IR drive output in each device
  - User selectable sink current up to 400 mA
  - Can be combined with 100 mA Barcode driver to form 500 mA IR driver
- **100 mA Current Drive Barcode Emulator**
  - One barcode driver output in each device
  - User selectable sink current up to 100 mA
  - Can be combined with 400 mA IR driver to use as 500 mA IR driver
- **Flexible On-Chip Clocking**
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device

iCE40 UltraLite Family Data Sheet Architecture

Architecture Overview

The iCE40 UltraLite family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable I²C controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE40UL-1K device.

Figure 2-1. iCE40UL-1K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

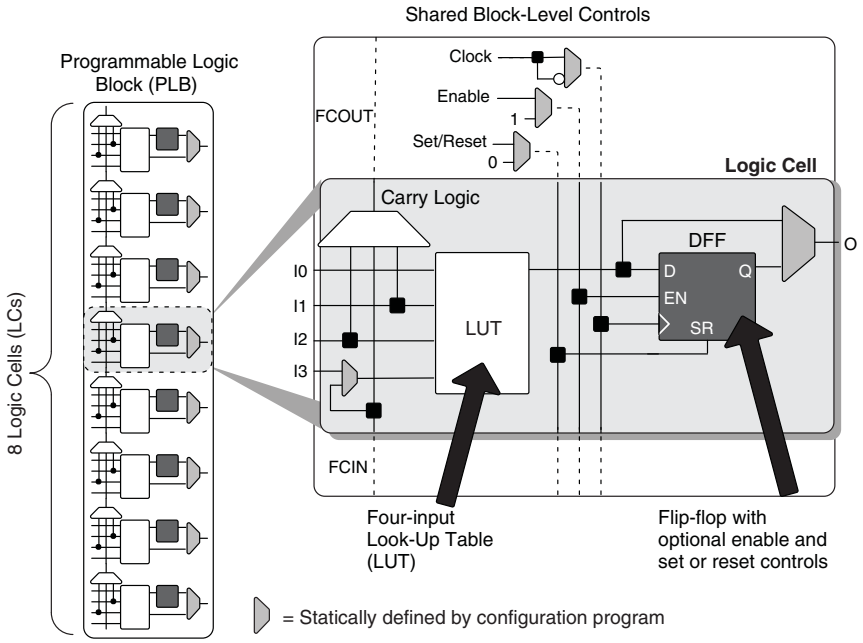
In the iCE40 UltraLite family, there are three sysIO banks, one on top and two at the bottom. User can connect all V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

The iCE40 UltraLite also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks, and a 100 mA Barcode emulation output.

PLB Blocks

The core of the iCE40 UltraLite device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

Routing

There are many resources provided in the iCE40 UltraLite devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 UltraLite device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 UltraLite External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraLite device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraLite device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysCLOCK Phase Locked Loops (PLLs) *(sysCLOCK PLL is only supported in 36-ball ucBGA package)*

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraLite devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraLite global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraLite PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

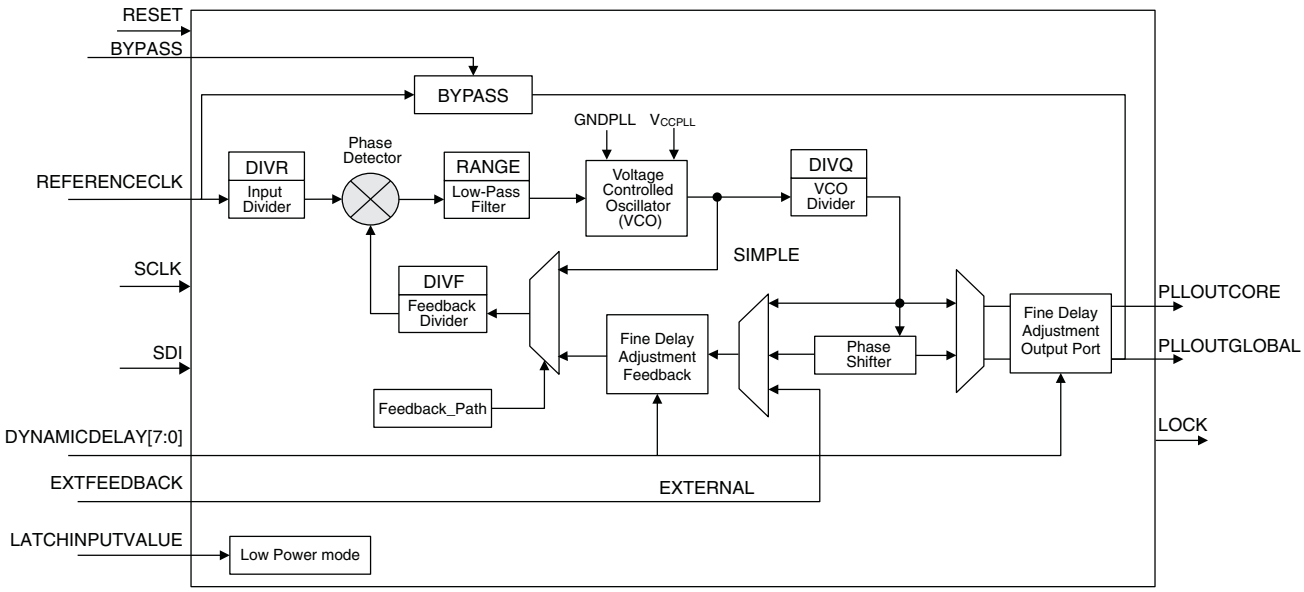


Table 2-3 provides signal descriptions of the PLL block.

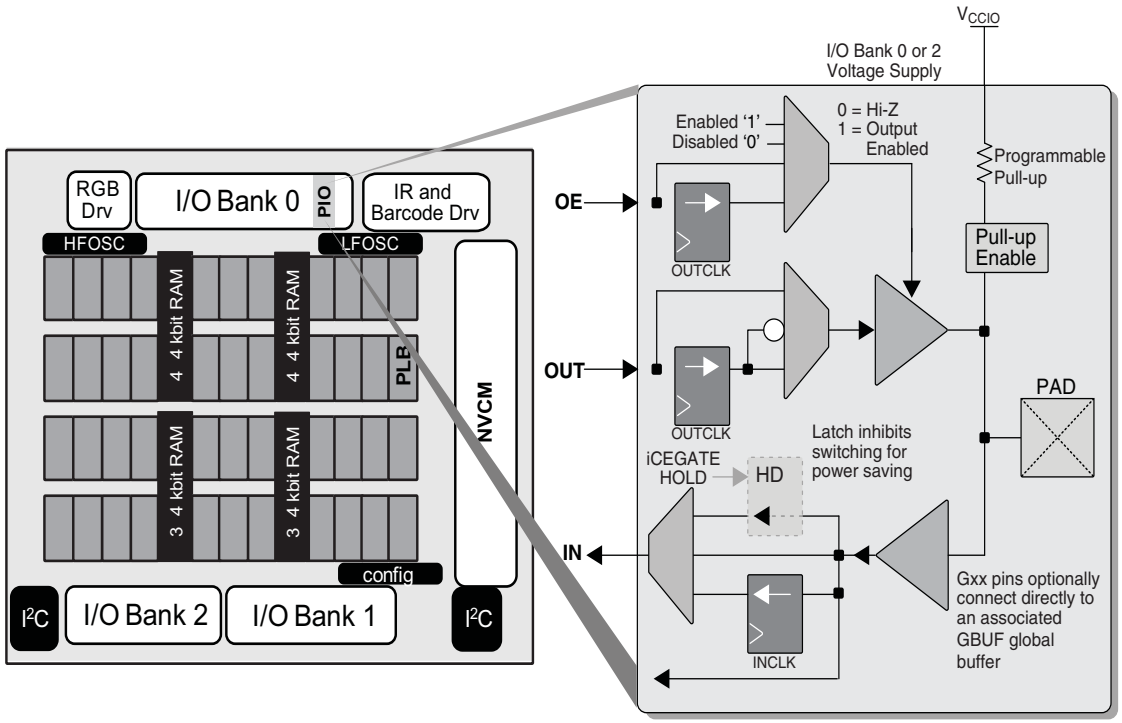
sysIO Buffer Banks

iCE40 UltraLite devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. On the 16 WLCSP package, V_{CCIO1} and V_{PP_2V5} are connected to the same pin on the package, and must meet the voltage requirement of both supplies. Please refer to the Pin Information Summary table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-5. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-6 shows the input/output register block for the PIOs.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO}, and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics chapter of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO}, and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 UltraLite sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 UltraLite devices.

Programmable Pull Up Resistors

The iCE40 UltraLite sysIO buffer can be configured with programmable pull up resistors on every I/O. The options are 3.3 kOhms, 6.8 kOhms, 10 kOhms or 100 kOhms (default). This feature is useful in supporting the I^2C interface. The user can also use it for other purposes.

Differential Comparators

The iCE40 UltraLite devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the Pin Information Summary section to locate the corresponding paired I/Os with differential comparators.

Table 2-7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes		
LVCMOS25		Yes	
LVCMOS18[1]			Yes

1. Not supported in bank 0 for 16-WLCP package.

Table 2-8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18[1]	1.8 V

1. Not supported in bank 0 for 16-WLCP package.

iCE40 UltraLite Programming and Configuration

This section describes the programming and configuration of the iCE40 UltraLite family.

Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO01} power supply.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 UltraLite, please see TN1248, iCE40 Programming and Configuration.

Power Saving Options

The iCE40 UltraLite devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-10 describes the function of these features.

Table 2-10. iCE40 UltraLite Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

iCE40 UltraLite Family Data Sheet DC and Switching Characteristics

November 2016 Data Sheet DS1050

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.30 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	VPP_2V5 NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10	30	°C

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. Please refer to Power-Up Supply Sequencing section. V_{CC} and V_{CCPLL} are recommended to tie to same supply with an RC-based noise filter between them. Please refer to TN1252, iCE40 Hardware Checklist.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration mode subject to the condition that none of the HFOSC/LFOSC and RGB LED / IR / Barcode LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.
2. Power-up sequence must be followed. Please refer to Power-Up Supply Sequencing section.

Power-On Reset

All iCE40 UltraLite devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) V_{CC}, (2) SPI_V_{CCIO1} and (3) V_{PP_2V5}. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

Power-Up Supply Sequencing

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5V, or higher, before any subsequent power supplies in the sequence are applied.

1. **V_{CC}** and **V_{CCPLL}** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the V_{CCPLL} (Please refer to TN1252, iCE40 Hardware Checklist.)

2. **SPI_V_{CCIO1}** should be the next supply, and can be applied any time after the previous supplies (V_{CC} and V_{CCPLL}) have reached as level of 0.5 V or higher.

3. **V_{PP_2V5}** should be the next supply, and can be applied any time after previous supplies (V_{CC}, V_{CCPLL} and SPI_V_{CCIO1}) have reached a level of 0.5 V or higher.

4. **Other Supplies** (V_{CCIO0} and V_{CCIO2}) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (V_{CC} and V_{CCPLL}) have reached a level of 0.5 V or greater. *On the 16*

Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.6	1	V
		SPI_V_{CCIO1}	0.7	1.6	V
		V_{PP_2V5}	0.7	1.6	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.85	V
		SPI_V_{CCIO1}	—	1.6	V
		V_{PP_2V5}	—	1.6	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2$ V	—	—	+/–10	µA
C_1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_3	24 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
C_4	400 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	53	—	pf
C_5	100 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	–3	—	–31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	–8	—	–72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

Supply Current [1, 2, 3, 4, 5]

Symbol	Parameter	Typ. V_{CC} = 1.2 V[4]	Units
$I_{CCSTDBY}$	Core Power Supply Static Current	35	µA
$I_{PP2V5STDBY}$	V_{PP_2V5} Power Supply Static Current	1	µA
$I_{CCPLLSTDBY}$	PLL Power Supply Static Current	1	µA
$I_{CCIOSTDBY}$	V_{CCIO} Power Supply Static Current	1 at VCCIO equal or less 2.5 V; 5 at VCCIO equal or less 3.465 V	µA
I_{CCPEAK}	Core Power Supply Startup Peak Current	3.06	mA
$I_{PP\_2V5PEAK}$	V_{PP_2V5} Power Supply Startup Peak Current	2.15	mA
$I_{CCPLLPEAK}$	PLL Power Supply Startup Peak Current	3.06[6]	mA
$I_{CCIOPEAK}$	V_{CCIO} Power Supply Startup Peak Current	4.65 for config bank, 0.25 for regular IO bank	mA

1. Assumes programmed pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. TJ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. Peak current is the in rush current - highest current during power supply start up within the power supply ramp rate. See Power Supply Ramp Rates1, 2 section. These currents are measured with decoupling capacitance of 0.1 uF, 10 nF, and 1 nF to the power supply. Higher decoupling capacitance causes higher current.
6. PLL power supply shared with Core Power supply.

Internal Pull-Up Resistor Specifications

Parameter	Condition	Spec			Units
		Min	Typ	Max	
Resistor_3.3K	1.71 < Vccio < 3.47 V	2.64	3.3	3.96	kOhm
Resistor_6.8K	1.71 < Vccio < 3.47 V	5.44	6.8	8.16	kOhm
Resistor_10K	1.71 < Vccio < 3.47 V	8	10	12	kOhm
Weak pull-up resistor	1.71 < Vccio < 1.89 V	—	100	—	kOhm
	2.38 < Vccio < 2.63 V	—	55	—	kOhm
	3.13 < Vccio < 3.47 V	—	40	—	kOhm

User I2C Specifications[1]

SN	Symbol	Parameter	STD Mode		FAST Mode		FAST Mode Plus		
			Min	Max	Min	Max	Min	Max	Units
1	fSCL	SCL clock frequency		100		400		1000[2]	kHz

1. Refer to the I2C specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I2C bus. Internal pull up may not be sufficient to support the maximum speed.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	µs
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices - Low Frequency (Default)	53	ms
		All devices - Medium frequency	25	ms
		All devices - High frequency	13	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

High Current LED, IR LED and Barcode LED Drives[1]

Symbol	Parameter	VCCIO = 3.3 V			VCCIO = 2.5 V		
		Min.	Max.	Units	Min.	Max.	Units
$I_{RGB\_ACCURACY\_FULL}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.5 ~ 2.5 V	–12	+12	%	not allowed	not allowed	%
$I_{RGB\_ACCURACY\_HALF}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.35 ~ 2.5 V	–14	+14	%	–14	+14	%
I_{RGB_MATCH}	RGB LED0, LED1, LED2 Sink Current Matching among the 3 outputs @ V_{PAD} = 0.35 ~ 2.5 V	–5	+5	%	–5	+5	%
$I_{IR\_ACCURACY\_FULL}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{IR\_ACCURACY\_HALF}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	–12	+12	%
$I_{BARCODE\_ACCURACY\_FULL}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{BARCODE\_ACCURACY\_HALF}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	not allowed	not allowed	%

1. Refer to Table 2-9 for valid current settings.

RGB LED Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	$F_{PWM\_OUT\_X}$ FR_{250} = 0	Frequency of the PWM output for color LED; When FR_{250} = 0		125		Hz
2	$F_{PWM\_OUT\_X}$ FR_{250} = 1	Frequency of the PWM output for color LED; When FR_{250} = 1		250		Hz
3	T_{HIGH_X}	PWM High percentage for color LED.	0		99	%
4	$T_{HIGH\_STEP\_X}$	PWM High percentage incremental step.		1/256		%

IR Transceiver IP Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	F_{IR_OUT}	Frequency of the IR output	25		120	kHz
2	F_{IR_IN}	Frequency of the IR input	25		120	kHz
3	$T_{HIGH\ (DUTY1/3\ =\ 0)}$	Duty Cycle when DUTY1/3 = 0.		50		%
4	$T_{HIGH\ (DUTY1/3\ =\ 1)}$	Duty Cycle when DUTY1/3 = 1.		33.33		%

Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-1.

Figure 3-3. Output Test Load, LVCMOS Standards

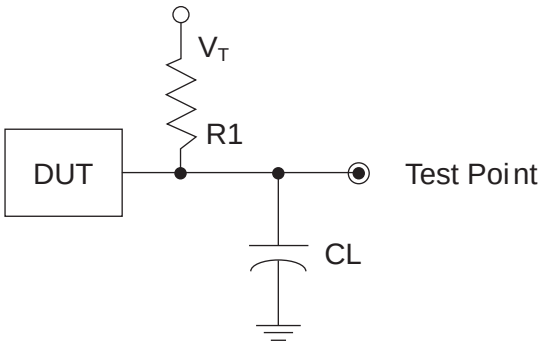


Table 3-1. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15 V	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

PIOB_15b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_17b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_22b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer.
PIOT_21a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer.
PIOB_13b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer.
PIOB_8a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer.
PIOB_7b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer.
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer.
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.

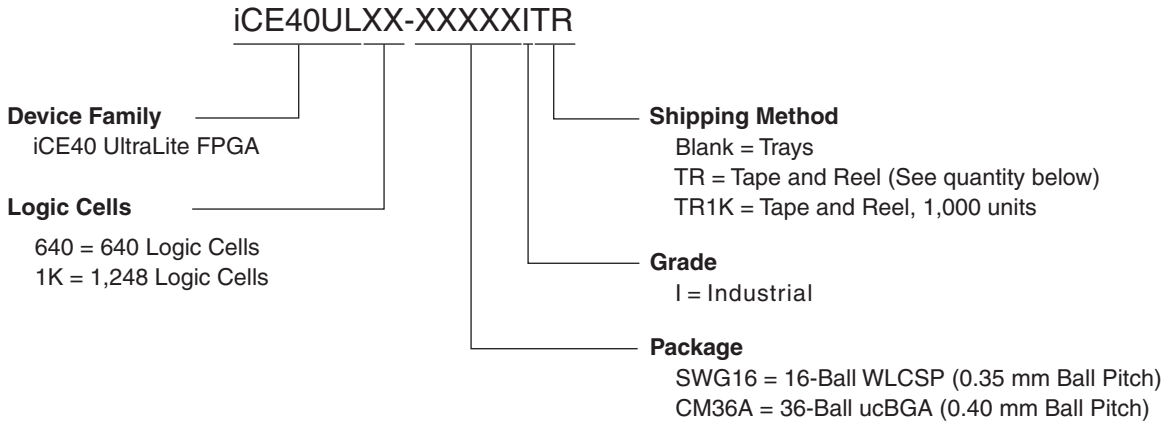
Pin Information Summary

Pin Type		iCE40UL1K		iCE40UL640	
		SWG16	36 ucBGA	SWG16	36 ucBGA
General Purpose I/O Per Bank	Bank 0	5	12	5	12
	Bank 1	4	4	4	4
	Bank 2	1	10	1	10
Total General Purpose I/Os		10	26	10	26
VCC		1	1	1	1
VCCIO	Bank 0	0	1	0	1
	Bank 1	0	1	0	1
	Bank 2	1	1	1	1
VCCPLL		0	1	0	1
VCPP_2V5		1	1	1	1
CRESET_B		1	1	1	1
CDONE		0	0	0	0
GND		1	2	1	2
GND_LED		1	1	1	1
Total Balls		16	36	16	36

iCE40 UltraLite Family Data Sheet Ordering Information

April 2016 Data Sheet DS1050

iCE40 UltraLite Part Number Description



Tape and Reel Quantity

Package	TR Quantity
CM36A	4,000
SWG16	5,000

Ordering Part Numbers

Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temp.
ICE40UL1K-SWG16ITR	1248	1.2	Halogen-Free WLCSP	16	IND
ICE40UL1K-CM36AITR	1248	1.2	36-Ball ucBGA	36	IND
ICE40UL1K-CM36AITR1K	1248	1.2	36-Ball ucBGA	36	IND
ICE40UL640-SWG16ITR	640	1.2	Halogen-Free WLCSP	16	IND
ICE40UL640-CM36AITR	640	1.2	36-Ball ucBGA	36	IND
ICE40UL640-CM36AITR1K	640	1.2	36-Ball ucBGA	36	IND

iCE40 UltraLite Family Data Sheet Revision History

November 2016 **Data Sheet DS1050**

Date	Version	Section	Change Summary
November 2016	1.4	DC and Switching Characteristics	Updated External Reset section. Added information on following supply sequence.
June 2016	1.3	Introduction	Updated General Description section. — Changed “embedded RGB PWM IP” to ”hardened RGB PWM IP”. — Changed “modulation logic” to “hardened TX/RX pulse logic”. — Updated information on the use of 500 mA IR driver.
			Updated Introduction section. — Added “RGB LED and IR LED” to configurable Controllers. — Added “LED” to RGB control functions.
		Architecture	Updated Architecture Overview section. — Changed caption to Figure 2-1, iCE40UL1K iCE40UL-1K Device, Top View. — Changed logic blocks to PLB. — Changed “LED sink” to “RGB and IR LED sinks, and a 100 mA Bar-code emulation output”. — Corrected headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. — Updated footnote in Table 2-4, sysMEM Block Configuration. — Updated sysIO Buffer Banks section. — Corrected V_{CCIO} format in Figure 2-5, I/O Bank and Programmable I/O Cell. — Updated Typical I/O Behavior During Power-up section. — Updated Supported Standards section. — Updated Programmable Pull Up Resistors section. — Changed “more than one byte” to “multiple bytes” in User I^2C IP section. — Updated High Current LED Drive I/O Pins section. Changed heading to High Current LED Drive I/O Pins. Added LED to “high current drive”. Added information on use of 500 mA IR LED. Added paragraph to reference Table 2-9. — Changed heading to Hardened RGB PWM IP. — Changed heading to Hardened IR Transceiver IP.
			Updated iCE40 UltraLite Programming and Configuration section. Changed VCCIO_1 to SPI_V_{CCIO1} in Device Programming.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Corrected V_{PP_2V5} and V_{CCPLL} format.
			Updated Recommended Operating Conditions section. — Changed heading to Hardened RGB PWM IP. — Updated footnote.
			Removed Power-up Sequence section.
			Added the following sections: — Power-On Reset — Power-Up Supply Sequencing — External Reset
			Updated DC Electrical Characteristics section. Revised footnote 4.
			Updated Supply Current section. — Changed V_{PP_2V5} format. — Updated footnote 5.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for f_{CLKHF} and DCH_{CLKHF}.
			Updated Differential Comparator Electrical Characteristics section.

Date	Version	Section	Change Summary
			Updated iCE40 UltraLite External Switching Characteristics section. Revised footnote.
			Updated sysCLOCK PLL Timing section. Revised t_{OPJIT} conditions.
			Updated sysCONFIG Port Timing Specifications section. — Added footnote to Master SPI. — Added footnote to MCLK setup time. — Revised t_{MTSU} minimum value. — Added footnotes 3 and 4.
		Supplemental Information	Updated For Further Information section. Added reference to TN1252, iCE40 Hardware Checklist.
April 2016	1.2	Introduction	Updated Features section. — Updated BGA package to ucBGA. — Corrected HF Oscillator unit in Table 1-1, iCE40 UltraLite Family Selection Guide.
		Architecture	Updated sysCLOCK Phase Locked Loops (PLLs) (sysCLOCK PLL is only supported in 36-ball ucBGA package) section. Updated BGA package to ucBGA in heading.
		DC and Switching Characteristics	Updated Recommended Operating Conditions section. Added footnote 4 regarding V_{PP_2V5}.
		Pinout Information	Updated Signal Descriptions and Pin Information Summary sections. — Updated BGA package to ucBGA. — Changed SPI_CSN to SPI_SS_B. — Corrected minor typo errors.
		Ordering Information	Updated iCE40 UltraLite Part Number Description section. — Added shipment types. — Updated BGA package to ucBGA.
			Added Tape and Reel Quantity section.
			Updated Ordering Part Numbers section. — Added part numbers. — Updated BGA package to ucBGA.
March 2015	1.1	All	Document status changed from Preliminary to Final.
		Introduction	Updated General Description and Features sections. Changed the LFOSC frequency value from 9.7 kHz to 10 kHz.
		Architecture	Updated On-Chip Oscillator section. Changed the LFOSC frequency value from 9.7 kHz to 10 kHz.
		DC and Switching Characteristics	Updated Power-up Sequence section. Revised power-up sequence description for 16-ball WLCSP. Added Power-up Sequence table.
			Updated User I2C Specifications section. Added footnote 2.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added and revised values. Removed footnote.
			Updated Maximum sysIO Buffer Performance section. Revised value for LED I/O used as GPIO open drain.
			Updated High Current LED, IR LED and Barcode LED Drives[1] section. Revised values.
January 2015	1.0	All	Initial release.