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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	57344
Number of I/O	26
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40ul640-cm36aitr1k

iCE40 UltraLite Family Data Sheet Introduction

General Description

iCE40 UltraLite family is an optimum logic, smallest footprint, low I/O count ultra-low power FPGA and sensor manager with instant on capability. It is designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 UltraLite family includes integrated blocks to interface with virtually all mobile sensors and application processors. The iCE40 UltraLite family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The hardened RGB PWM IP, with the three 24 mA constant current RGB LED outputs on the iCE40 UltraLite provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 400 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the hardened TX/RX pulse logic that meets their needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. The 100 mA Barcode Emulation driver output provides a direct interface for applications such as barcode scanning. The 100 mA and 400 mA drivers can also be combined to be used as a 500 mA IR driver if higher than 400 mA current drive is required.

The iCE40 UltraLite family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 UltraLite family features two device densities of 640 or 1K Look Up Tables (LUTs) of logic with programmable I/Os that can be used as an interface port or general purpose I/O. It also has up to 56 kbits of Block RAMs to work with user logic.

Features

- **Flexible Logic Architecture**
  - Two devices with 640 or 1K LUTs
  - Offered in 16-ball WLCSP package
  - Offered in 36-ball ucBGA package

- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - Typical 35 µA standby current which equals 42 uW standby power consumption

- **Embedded and Distributed Memory**
  - Up to 56 kbits sysMEM™ Embedded Block RAM

- **Two Hardened Interfaces**
  - Two optional FIFO mode I^{2}C interface up to 1 MHz
  - Either master or slave

- **Two On-Chip Oscillators**
  - Low Frequency Oscillator - 10 kHz
  - High Frequency Oscillator - 48 MHz

- **Hardened PWM circuit for RGB**

- **Hardened TX/RX Pulse Logic circuit for IR LED**

- **24 mA Current Drive RGB LED Outputs**
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA

- **400 or 500 mA Current Drive IR LED Output**
  - One IR drive output in each device
  - User selectable sink current up to 400 mA
  - Can be combined with 100 mA Barcode driver to form 500 mA IR driver

- **100 mA Current Drive Barcode Emulator**
  - One barcode driver output in each device
  - User selectable sink current up to 100 mA
  - Can be combined with 400 mA IR driver to use as 500 mA IR driver

- **Flexible On-Chip Clocking**
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device

■ **Flexible Device Configuration**
  • SRAM is configured through:
    — Standard SPI Interface
    — Internal Nonvolatile Configuration Memory (NVCM)

■ **Ultra-Small Form Factor**
  • As small as 1.409 mm x 1.409 mm

■ **Applications**
  • Smartphones
  • Tablets and Consumer Handheld Devices
  • Handheld Industrial Devices
  • Multi Sensor Management Applications
  • IR remote, Barcode emulator
  • RGB light control

Table 1-1. iCE40 UltraLite Family Selection Guide

Part Number	iCE40UL-640	iCE40UL-1K
Logic Cells (LUT + Flip-Flop)	**640**	**1248**
EBR Memory Blocks	14	14
EBR Memory Bits	56 k	56 k
PLL Block[1]	1	1
Hardened I2C	2	2
Hardened IR TX/RX	1	1
Hardened RGB PWM IP	1	1
HF Oscillator (48 MHz)	1	1
LF Oscillator (10 kHz)	1	1
24 mA LED Sink	3	3
100 mA LED Sink	1	1
400 mA LED Sink	1	1
Packages, ball pitch, dimension	**Programmable I/O Count**	
16-ball WLCSP, 0.35 mm, 1.409 mm x 1.409 mm	10	10
36-ball ucBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26

1. Only in 36-ball ucBGA package.

Introduction

The iCE40 UltraLite devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as user configurable RGB LED and IR LED Controllers, and two Oscillators.

The iCE40 UltraLite FPGAs are available in very small form factor packages, as small as 1.409 mm x 1.409 mm. The small form factor allows the device to easily fit into a lot of mobile applications. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40 UltraLite devices offer I/O features such as programmable multiple value pull-up resistors. Pull-up features are controllable on a "per-pin" basis.

The iCE40 UltraLite devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 UltraLite family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 UltraLite. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 UltraLite device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 UltraLite FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as IR remote, barcode emulator, and RGB LED control functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, please contact your local Lattice representative.

PLB Blocks

The core of the iCE40 UltraLite device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram
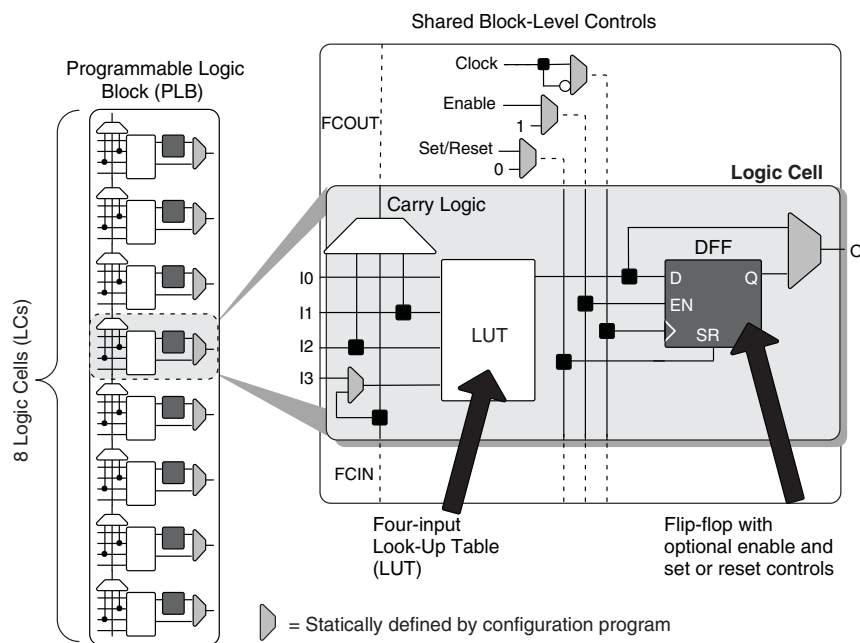
Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.

- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.

- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

Routing

There are many resources provided in the iCE40 UltraLite devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 UltraLite device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 UltraLite External Switching Characteristics tables later in this document.

Global Hi-Z Control
The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraLite device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control
The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraLite device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysCLOCK Phase Locked Loops (PLLs) *(sysCLOCK PLL is only supported in 36-ball ucBGA package)*

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraLite devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraLite global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraLite PLL. There are 2 FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, please refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.
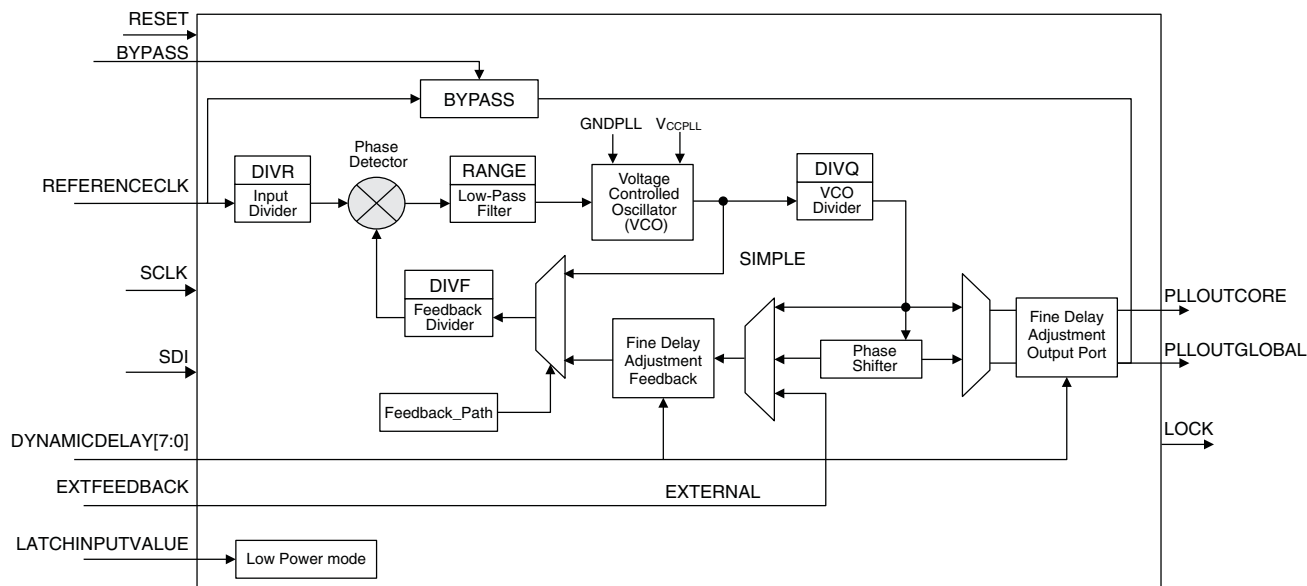
Figure 2-3. PLL Diagram

Table 2-3 provides signal descriptions of the PLL block.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 Ultra, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock and falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses falling-edge clocks on both Read and Write.

Figure 2-6. iCE I/O Register Block Diagram

= Statically defined by configuration program.
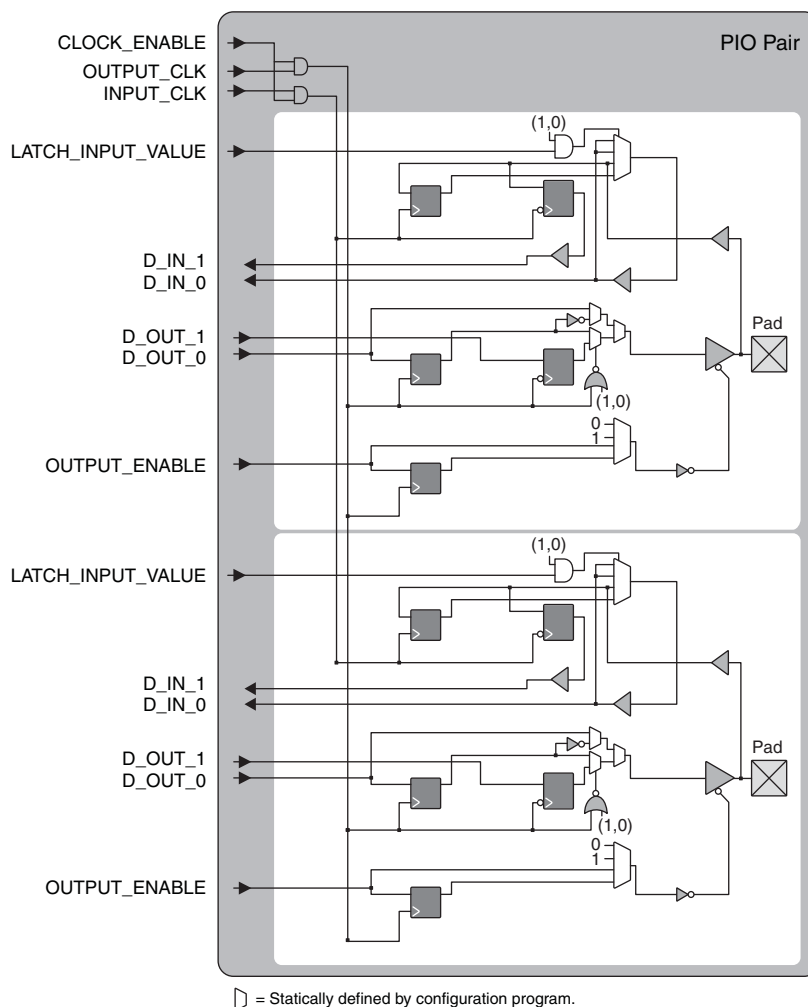
Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO}, and V_{PP_2V5} reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics chapter of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO}, and V_{PP_2V5} reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 UltraLite sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 UltraLite devices.

Programmable Pull Up Resistors

The iCE40 UltraLite sysIO buffer can be configured with programmable pull up resistors on every I/O. The options are 3.3 kOhms, 6.8 kOhms, 10 kOhms or 100 kOhms (default). This feature is useful in supporting the I²C interface. The user can also use it for other purposes.

Differential Comparators

The iCE40 UltraLite devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. Please refer to the Pin Information Summary section to locate the corresponding paired I/Os with differential comparators.

Table 2-7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes		
LVCMOS25		Yes	
LVCMOS18[1]			Yes

1. Not supported in bank 0 for 16-WLCP package.

Table 2-8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18[1]	1.8 V

1. Not supported in bank 0 for 16-WLCP package.

download from either the internal NVCM or the external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . –0.5 V to 1.42 V

Output Supply Voltage V_{CCIO} . . . . –0.5 V to 3.60 V

NVCM Supply Voltage V_{PP_2V5} . . . . –0.5 V to 3.60 V

PLL Supply Voltage V_{CCPLL} . . . . –0.5 V to 1.30 V

I/O Tri-state Voltage Applied. . . . . –0.5 V to 3.60 V

Dedicated Input Voltage Applied . . . . –0.5 V to 3.60 V

Storage Temperature (Ambient). . . . . –65 °C to 150 °C

Junction Temperature (T_J) . . . . –65 °C to 125 °C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

WLCSP package, VCCIO0 and VPP_2V5 are connected to the same pin on the package, and should be powered as VPP_2V5 in the sequence.

There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are repowered up again.

External Reset

When all power supplies have reached to their minimum operating voltage defined in Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of t_{CRESET_B}, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory.

Figure 3-1 shows Power-Up sequence when SPI_V_{CCIO1} and V_{PP_2V5} are connected separately, and the CRESET_B signal triggers configuration download. Figure 3-2 shows when SPI_V_{CCIO1} and V_{PP_2V5} connected together. If the supply sequence is not followed, extra peak current may be observed on the supplies during power up.

All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

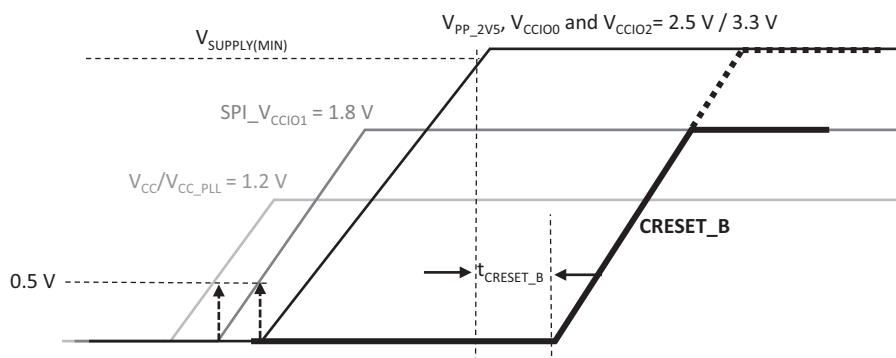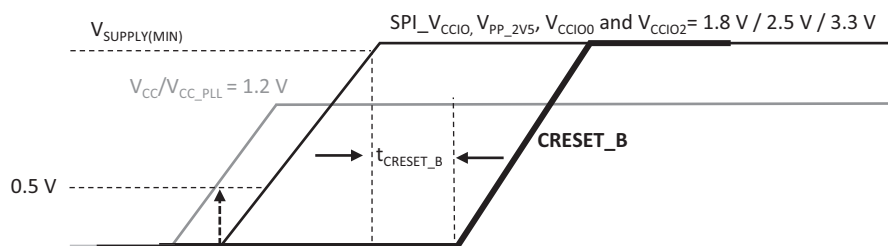*Figure 3-1. Power Up Sequence with SPI_V_{CCIO1} and V_{PP_2V5} Not Connected Together*

Figure 3-2. Power Up Sequence with All Supplies Connected Together

Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.6	1	V
		SPI_V_{CCIO1}	0.7	1.6	V
		V_{PP_2V5}	0.7	1.6	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.85	V
		SPI_V_{CCIO1}	—	1.6	V
		V_{PP_2V5}	—	1.6	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2$ V	—	—	+/−10	µA
C_1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_3	24 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
C_4	400 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	53	—	pf
C_5	100 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	−3	—	−31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	−8	—	−72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	−11	—	−128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

Internal Oscillators (HFOSC, LFOSC)

Parameter		Parameter Description	Spec/Recommended			Units
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency ($t_J = 0$ ℃–85 ℃)	−10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency ($t_J = -40$ ℃–100 ℃)	−20%	48	20%	MHz
f_{CLKLF}		LFOSC CLKK clock frequency	−10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC clock frequency ($t_J = 0$ ℃–85 ℃)	45	50	55	%
	Industrial Temp	HFOSC clock frequency ($t_J = -45$ ℃–100 ℃)	40	50	60	%
DCH_{CLKLF}		LFOSC Duty Cycle (Clock High Period)	45	50	55	%
t_{WAKEUP}		Delay OSC Enable to output enable delay	—	—	100	μs
Tsync_on		Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off		Oscillator output disable delay	—	—	5	Cycles

sysIO Recommended Operating Conditions

	V_{CCIO} (V)		
Standard	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.4	8	−8
					0.2	V_{CCIO} - 0.2	0.1	−0.1
LVCMOS 2.5	-0.3	0.7	1.7	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.4	6	−6
					0.2	V_{CCIO} - 0.2	0.1	−0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.4	4	−4
					0.2	V_{CCIO} - 0.2	0.1	−0.1

Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{REF}	Reference Voltage to compare, on V_{INM}	$V_{CCIO} = 2.5$ V	0.25	V_{CCIO} −0.25 V	V
V_{DIFFIN_H}	Differential input HIGH (V_{INP} - V_{INM})	$V_{CCIO} = 2.5$ V	250	—	mV
V_{DIFFIN_L}	Differential input LOW (V_{INP} - V_{INM})	$V_{CCIO} = 2.5$ V	—	−250	mV
I_{IN}	Input Current, V_{INP} and V_{INM}	$V_{CCIO} = 2.5$ V	−10	10	μA

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	µs
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices - Low Frequency (Default)	53	ms
		All devices - Medium frequency	25	ms
		All devices - High frequency	13	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraLite device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{MTSU}	MCLK setup time[4]		9.9	—	—	ns
t_{MTH}	MCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V VCC and at 25 C.
3. tSU and tHD timing must be met for all MCLK frequency choices
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

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Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V_{CC}		Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}		Power	—	Power for I/Os in Bank 0, 1, and 2. V_{CCIO0} is tied with V_{PP_2V5} and V_{CCIO2} is tied with SPI_V_{CCIO1} in 16 WLCS package.
V_{PP_2V5}		Power	—	Power for NVCM programming and operations
V_{CCPLL}		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board
Configuration				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. Include a weak internal pull-up resistor to V_{CCIO_2}. Or actively driven externally or connect an 10K-Ohm pull-up to V_{CCIO_2}.
PIOB_8a	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to V_{CCIO_2}. In 16 WLCS CDONE shared with PIOB_8a.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_11b	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to V_{CCIO_2}. In 36-ball ucBGA package CDONE shared with PIOB_11b.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_16a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_14a	SPI_SO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

PIOB_15b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_17b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_22b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer.
PIOT_21a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer.
PIOB_13b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer.
PIOB_8a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer.
PIOB_7b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer.
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer.
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.

RGB2	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
IRLED	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 400 mA output to drive external LED.
BARCODE	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 100 mA output to drive external LED.
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location).
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location).

Date	Version	Section	Change Summary
November 2016	1.4	DC and Switching Characteristics	Updated External Reset section. Added information on following supply sequence.
June 2016	1.3	Introduction	Updated General Description section. — Changed "embedded RGB PWM IP" to "hardened RGB PWM IP". — Changed "modulation logic" to "hardened TX/RX pulse logic". — Updated information on the use of 500 mA IR driver.
			Updated Introduction section. — Added "RGB LED and IR LED" to configurable Controllers. — Added "LED" to RGB control functions.
		Architecture	Updated Architecture Overview section. — Changed caption to Figure 2-1, iCE40UL1K iCE40UL-1K Device, Top View. — Changed logic blocks to PLB. — Changed "LED sink" to "RGB and IR LED sinks, and a 100 mA Barcode emulation output". — Corrected headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. — Updated footnote in Table 2-4, sysMEM Block Configuration. — Updated sysIO Buffer Banks section. — Corrected V_{CCIO} format in Figure 2-5, I/O Bank and Programmable I/O Cell. — Updated Typical I/O Behavior During Power-up section. — Updated Supported Standards section. — Updated Programmable Pull Up Resistors section. — Changed "more than one byte" to "multiple bytes" in User I^{2}C IP section. — Updated High Current LED Drive I/O Pins section. Changed heading to High Current LED Drive I/O Pins. Added LED to "high current drive". Added information on use of 500 mA IR LED. Added paragraph to reference Table 2-9. — Changed heading to Hardened RGB PWM IP. — Changed heading to Hardened IR Transceiver IP.
			Updated iCE40 UltraLite Programming and Configuration section. Changed VCCIO_1 to SPI_V_{CCIO1} in Device Programming.
		DC and Switching Characteristics	Updated Absolute Maximum Ratings section. Corrected V_{PP_2V5} and V_{CCPLL} format.
			Updated Recommended Operating Conditions section. — Changed heading to Hardened RGB PWM IP. — Updated footnote.
			Removed Power-up Sequence section.
			Added the following sections: — Power-On Reset — Power-Up Supply Sequencing — External Reset
			Updated DC Electrical Characteristics section. Revised footnote 4.
			Updated Supply Current section. — Changed V_{PP_2V5} format. — Updated footnote 5.
			Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for f_{CLKHF} and DCH_{CLKHF}
			Updated Differential Comparator Electrical Characteristics section.