Lattice Semiconductor Corporation - ICE40UL640-SWG16ITR50 Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	57344
Number of I/O	10
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	16-XFBGA, WLCSP
Supplier Device Package	16-WLCSP (1.4x1.48)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40ul640-swg16itr50

iCE40 UltraLite Family Data Sheet Introduction

July 2016 Data Sheet DS1050

General Description

iCE40 UltraLite family is an optimum logic, smallest footprint, low I/O count ultra-low power FPGA and sensor manager with instant on capability. It is designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 UltraLite family includes integrated blocks to interface with virtually all mobile sensors and application processors. The iCE40 UltraLite family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The hardened RGB PWM IP, with the three 24 mA constant current RGB LED outputs on the iCE40 UltraLite provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 400 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. Users simply implement the hardened TX/RX pulse logic that meets their needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. The 100 mA Barcode Emulation driver output provides a direct interface for applications such as barcode scanning. The 100 mA and 400 mA drivers can also be combined to be used as a 500 mA IR driver if higher than 400 mA current drive is required.

The iCE40 UltraLite family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 UltraLite family features two device densities of 640 or 1K Look Up Tables (LUTs) of logic with programmable I/Os that can be used as an interface port or general purpose I/O. It also has up to 56 kbits of Block RAMs to work with user logic.

Features

- **Flexible Logic Architecture**
  - Two devices with 640 or 1K LUTs
  - Offered in 16-ball WLCSP package
  - Offered in 36-ball ucBGA package
- **Ultra-low Power Devices**
  - Advanced 40 nm ultra-low power process
  - Typical 35 µA standby current which equals 42 uW standby power consumption
- **Embedded and Distributed Memory**
  - Up to 56 kbits sysMEM™ Embedded Block RAM
- **Two Hardened Interfaces**
  - Two optional FIFO mode I^2C interface up to 1 MHz
  - Either master or slave
- **Two On-Chip Oscillators**
  - Low Frequency Oscillator - 10 kHz
  - High Frequency Oscillator - 48 MHz
- **Hardened PWM circuit for RGB**
- **Hardened TX/RX Pulse Logic circuit for IR LED**
- **24 mA Current Drive RGB LED Outputs**
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- **400 or 500 mA Current Drive IR LED Output**
  - One IR drive output in each device
  - User selectable sink current up to 400 mA
  - Can be combined with 100 mA Barcode driver to form 500 mA IR driver
- **100 mA Current Drive Barcode Emulator**
  - One barcode driver output in each device
  - User selectable sink current up to 100 mA
  - Can be combined with 400 mA IR driver to use as 500 mA IR driver
- **Flexible On-Chip Clocking**
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device

- **Flexible Device Configuration**
  - SRAM is configured through:
    - — Standard SPI Interface
    - — Internal Nonvolatile Configuration Memory (NVCM)
- **Ultra-Small Form Factor**
  - As small as 1.409 mm x 1.409 mm
- **Applications**
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Industrial Devices
  - Multi Sensor Management Applications
  - IR remote, Barcode emulator
  - RGB light control

Table 1-1. iCE40 UltraLite Family Selection Guide

Part Number	iCE40UL-640	iCE40UL-1K
Logic Cells (LUT + Flip-Flop)	**640**	**1248**
EBR Memory Blocks	14	14
EBR Memory Bits	56 k	56 k
PLL Block[1]	1	1
Hardened I2C	2	2
Hardened IR TX/RX	1	1
Hardened RGB PWM IP	1	1
HF Oscillator (48 MHz)	1	1
LF Oscillator (10 kHz)	1	1
24 mA LED Sink	3	3
100 mA LED Sink	1	1
400 mA LED Sink	1	1
Packages, ball pitch, dimension	**Programmable I/O Count**	
16-ball WLCSP, 0.35 mm, 1.409 mm x 1.409 mm	10	10
36-ball ucBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26

1. Only in 36-ball ucBGA package.

Introduction

The iCE40 UltraLite devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as user configurable RGB LED and IR LED Controllers, and two Oscillators.

The iCE40 UltraLite FPGAs are available in very small form factor packages, as small as 1.409 mm x 1.409 mm. The small form factor allows the device to easily fit into a lot of mobile applications. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40 UltraLite devices offer I/O features such as programmable multiple value pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 UltraLite devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 UltraLite family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 UltraLite. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 UltraLite device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Routing

There are many resources provided in the iCE40 UltraLite devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 UltraLite device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 UltraLite External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraLite device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraLite device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

sysMEM Embedded Block RAM Memory

Larger iCE40 UltraLite device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

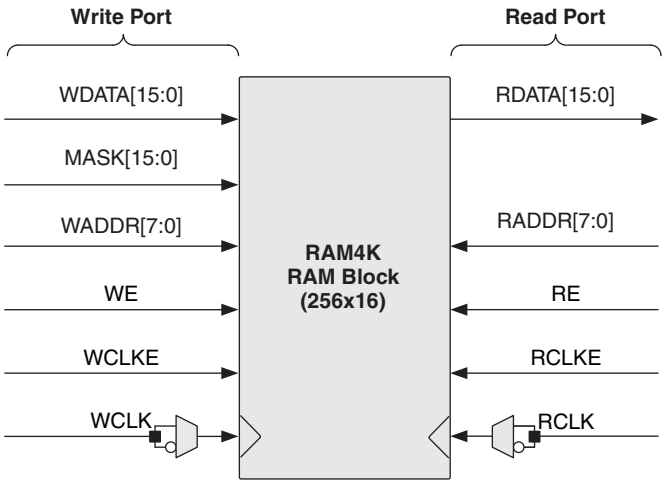


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit 1 = do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

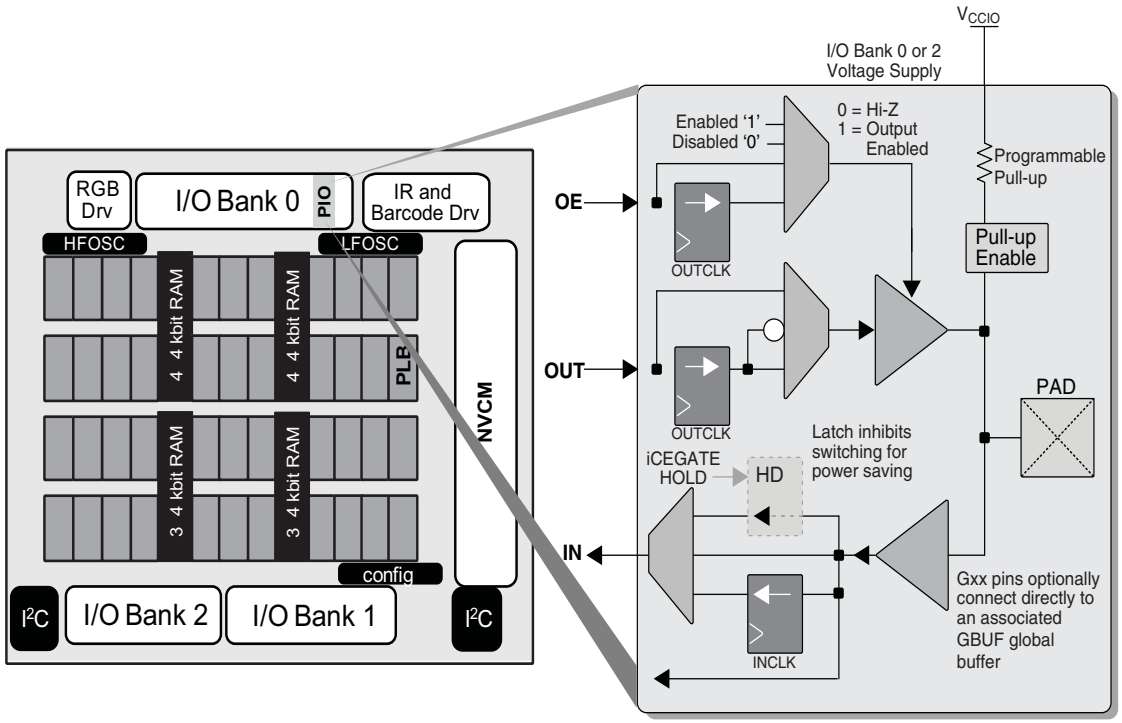
sysIO Buffer Banks

iCE40 UltraLite devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. On the 16 WLCSP package, V_{CCIO1} and V_{PP_2V5} are connected to the same pin on the package, and must meet the voltage requirement of both supplies. Please refer to the Pin Information Summary table.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

Figure 2-5. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 2-6 shows the input/output register block for the PIOs.

On-Chip Oscillator

The iCE40 UltraLite devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz, by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

User I²C IP

The iCE40 UltraLite devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. The pins for the I²C interface are not pre-assigned. User can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I²C components.

In optional FIFO mode, FIFOs are used for storing multiple bytes of data for transmit and / or receive in order to efficiently support the I²C sensor applications

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, please refer to TN1274, iCE40 SPI/I2C Hardened IP Usage Guide.

High Current LED Drive I/O Pins

The iCE40 UltraLite family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 UltraLite product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user programmable from 4 mA to 24 mA, in increments of 4 mA in full current mode or from 2 mA to 12 mA, in increments of 2 mA in half current mode. This output functions as General Purpose I/O with open-drain when the high current drive is not needed.

There is one output on each device that can sink up to 100 mA current. This output is open-drain, and provides sinking current to drive an external Barcode LED connecting to the positive supply. This Barcode drive current is user programmable from 16.6 mA to100 mA in increments of 16.6 mA in full current mode or 8.3 mA to 50 mA in

iCE40 UltraLite Family Data Sheet DC and Switching Characteristics

November 2016 Data Sheet DS1050

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.30 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–65 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

WLCSP package, VCCIO0 and VPP_2V5 are connected to the same pin on the package, and should be powered as VPP_2V5 in the sequence.

There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are repowered up again.

External Reset

When all power supplies have reached to their minimum operating voltage defined in Minimum Operation Condition Table, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of t_{CRESET_B}, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory.

Figure 3-1 shows Power-Up sequence when SPI_V_{CCIO1} and V_{PP_2V5} are connected separately, and the CRESET_B signal triggers configuration download. Figure 3-2 shows when SPI_V_{CCIO1} and V_{PP_2V5} connected together. If the supply sequence is not followed, extra peak current may be observed on the supplies during power up.

All power supplies should be powered up during configuration. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

Figure 3-1. Power Up Sequence with SPI_V_{CCIO1} and V_{PP_2V5} Not Connected Together

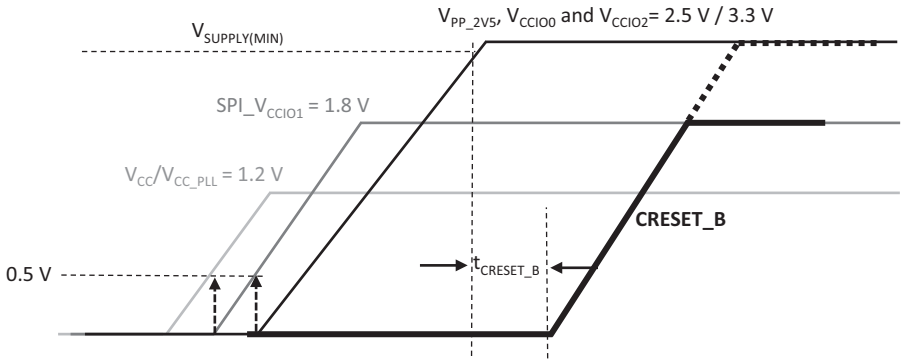
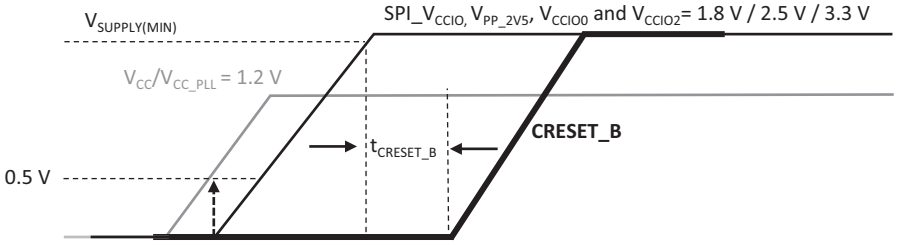


Figure 3-2. Power Up Sequence with All Supplies Connected Together



Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	0.6	1	V
		SPI_V_{CCIO1}	0.7	1.6	V
		V_{PP_2V5}	0.7	1.6	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, V_{PP_2V5})	V_{CC}	—	0.85	V
		SPI_V_{CCIO1}	—	1.6	V
		V_{PP_2V5}	—	1.6	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2$ V	—	—	+/–10	µA
C_1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_3	24 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
C_4	400 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	53	—	pf
C_5	100 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	–3	—	–31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	–8	—	–72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

Supply Current [1, 2, 3, 4, 5]

Symbol	Parameter	Typ. V_{CC} = 1.2 V[4]	Units
$I_{CCSTDBY}$	Core Power Supply Static Current	35	µA
$I_{PP2V5STDBY}$	V_{PP_2V5} Power Supply Static Current	1	µA
$I_{CCPLLSTDBY}$	PLL Power Supply Static Current	1	µA
$I_{CCIOSTDBY}$	V_{CCIO} Power Supply Static Current	1 at VCCIO equal or less 2.5 V; 5 at VCCIO equal or less 3.465 V	µA
I_{CCPEAK}	Core Power Supply Startup Peak Current	3.06	mA
$I_{PP\_2V5PEAK}$	V_{PP_2V5} Power Supply Startup Peak Current	2.15	mA
$I_{CCPLLPEAK}$	PLL Power Supply Startup Peak Current	3.06[6]	mA
$I_{CCIOPEAK}$	V_{CCIO} Power Supply Startup Peak Current	4.65 for config bank, 0.25 for regular IO bank	mA

1. Assumes programmed pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. TJ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. Peak current is the in rush current - highest current during power supply start up within the power supply ramp rate. See Power Supply Ramp Rates1, 2 section. These currents are measured with decoupling capacitance of 0.1 uF, 10 nF, and 1 nF to the power supply. Higher decoupling capacitance causes higher current.
6. PLL power supply shared with Core Power supply.

Internal Pull-Up Resistor Specifications

Parameter	Condition	Spec			Units
		Min	Typ	Max	
Resistor_3.3K	1.71 < Vccio < 3.47 V	2.64	3.3	3.96	kOhm
Resistor_6.8K	1.71 < Vccio < 3.47 V	5.44	6.8	8.16	kOhm
Resistor_10K	1.71 < Vccio < 3.47 V	8	10	12	kOhm
Weak pull-up resistor	1.71 < Vccio < 1.89 V	—	100	—	kOhm
	2.38 < Vccio < 2.63 V	—	55	—	kOhm
	3.13 < Vccio < 3.47 V	—	40	—	kOhm

User I2C Specifications[1]

SN	Symbol	Parameter	STD Mode		FAST Mode		FAST Mode Plus		
			Min	Max	Min	Max	Min	Max	Units
1	fSCL	SCL clock frequency		100		400		1000[2]	kHz

1. Refer to the I2C specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I2C bus. Internal pull up may not be sufficient to support the maximum speed.

Maximum sysIO Buffer Performance[1]

I/O Standard	Max. Speed	Units
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
LED I/O used as GPIO open drain	50	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz
LED I/O used as GPIO open drain	50[2]	MHz

1. Measured with a toggling pattern.
2. With external resistor from 180 Ohm to 250 Ohm and capacity of no more than 15 pF.

iCE40 UltraLite External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	Min	Max	Units
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	2	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	500	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[1]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All devices	—	410	ps
t_{CO}	Clock to Output - PIO Output Register	All devices	—	9.0	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All devices	–0.5	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	All devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output - PIO Output Register	All Devices	—	2.9	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	All Devices	7.9	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	All Devices	–0.6	—	ns

1. All the data is from the worst case condition.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)		16	275	MHz
f_{VCO}	PLL VCO Frequency		533	1066	MHz
f_{PFD}	Phase Detector Input Frequency		10	133	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle		40	60	%
t_{PH}	Output Phase Accuracy		—	+/–12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time		—	50	µs
t_{UNLOCK}	PLL Unlock Time		—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width		100	—	ns
t_{RST}	RESET Pulse Width		10	—	ns
t_{RSTREC}	RESET Recovery Time		10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Max.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices - Low Frequency (Default)	53	ms
		All devices - Medium frequency	25	ms
		All devices - High frequency	13	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40 UltraLite device is clearing its internal configuration memory		1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH		20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW		20	—	—	ns
t_{STSU}	CCLK setup time		12	—	—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge		1200	—	—	µs
t_{MTSU}	MCLK setup time[4]		9.9	—	—	ns
t_{MTH}	MCLK hold time		1	—	—	ns

1. Supported with 1.2 V Vcc and at 25 C.
2. Extended range fMAX Write operations support up to 53 MHz with 1.2 V VCC and at 25 C.
3. tSU and tHD timing must be met for all MCLK frequency choices
4. For considerations of SPI Master Configuration Mode, please refer to TN1248, iCE40 Programming and Configuration.

High Current LED, IR LED and Barcode LED Drives[1]

Symbol	Parameter	VCCIO = 3.3 V			VCCIO = 2.5 V		
		Min.	Max.	Units	Min.	Max.	Units
$I_{RGB\_ACCURACY\_FULL}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.5 ~ 2.5 V	–12	+12	%	not allowed	not allowed	%
$I_{RGB\_ACCURACY\_HALF}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.35 ~ 2.5 V	–14	+14	%	–14	+14	%
I_{RGB_MATCH}	RGB LED0, LED1, LED2 Sink Current Matching among the 3 outputs @ V_{PAD} = 0.35 ~ 2.5 V	–5	+5	%	–5	+5	%
$I_{IR\_ACCURACY\_FULL}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{IR\_ACCURACY\_HALF}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	–12	+12	%
$I_{BARCODE\_ACCURACY\_FULL}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{BARCODE\_ACCURACY\_HALF}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	not allowed	not allowed	%

1. Refer to Table 2-9 for valid current settings.

RGB LED Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	$F_{PWM\_OUT\_X}$ FR_{250} = 0	Frequency of the PWM output for color LED; When FR_{250} = 0		125		Hz
2	$F_{PWM\_OUT\_X}$ FR_{250} = 1	Frequency of the PWM output for color LED; When FR_{250} = 1		250		Hz
3	T_{HIGH_X}	PWM High percentage for color LED.	0		99	%
4	$T_{HIGH\_STEP\_X}$	PWM High percentage incremental step.		1/256		%

IR Transceiver IP Timing Specification

SN	Symbol	Parameter	Min	TYP	Max	Units
1	F_{IR_OUT}	Frequency of the IR output	25		120	kHz
2	F_{IR_IN}	Frequency of the IR input	25		120	kHz
3	$T_{HIGH\ (DUTY1/3\ =\ 0)}$	Duty Cycle when DUTY1/3 = 0.		50		%
4	$T_{HIGH\ (DUTY1/3\ =\ 1)}$	Duty Cycle when DUTY1/3 = 1.		33.33		%

Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-1.

Figure 3-3. Output Test Load, LVCMOS Standards

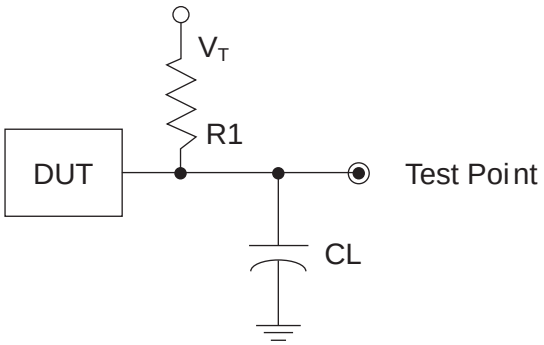


Table 3-1. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5 V	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15 V	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15 V	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name		Function	I/O	Description
Power Supplies				
V_{CC}		Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}		Power	—	Power for I/Os in Bank 0, 1, and 2. V_{CCIO0} is tied with V_{PP_2V5} and V_{CCIO2} is tied with SPI_V_{CCIO1} in 16 WLCS package.
V_{PP_2V5}		Power	—	Power for NVCM programming and operations
V_{CCPLL}		Power	—	Power for PLL
GND		GROUND	—	Ground
GND_LED		GROUND	—	Ground for LED drivers. Should connect to GND on board
Configuration				
Primary	Secondary			
CRESETB	—	Configuration	I	Configuration Reset, active LOW. Include a weak internal pull-up resistor to V_{CCIO_2}. Or actively driven externally or connect an 10K-Ohm pull-up to V_{CCIO_2}.
PIOB_8a	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to V_{CCIO_2}. In 16 WLCS CDONE shared with PIOB_8a.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_11b	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to V_{CCIO_2}. In 36-ball ucBGA package CDONE shared with PIOB_11b.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Config SPI				
Primary	Secondary			
PIOB_16a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_14a	SPI_SO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

PIOB_15b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function
PIOB_17b	SPI_SS_B	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
Global Signals				
Primary	Secondary			
PIOT_22b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer.
PIOT_21a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer.
PIOB_13b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer.
PIOB_8a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer.
PIOB_7b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer.
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer.
LED Signals				
RGB0		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
RGB1		General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
		LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.

RGB2	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24mA output to drive external LED.
IRLED	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 400 mA output to drive external LED.
BARCODE	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 100 mA output to drive external LED.
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location).
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location).

Pin Information Summary

Pin Type		iCE40UL1K		iCE40UL640	
		SWG16	36 ucBGA	SWG16	36 ucBGA
General Purpose I/O Per Bank	Bank 0	5	12	5	12
	Bank 1	4	4	4	4
	Bank 2	1	10	1	10
Total General Purpose I/Os		10	26	10	26
VCC		1	1	1	1
VCCIO	Bank 0	0	1	0	1
	Bank 1	0	1	0	1
	Bank 2	1	1	1	1
VCCPLL		0	1	0	1
VCPP_2V5		1	1	1	1
CRESET_B		1	1	1	1
CDONE		0	0	0	0
GND		1	2	1	2
GND_LED		1	1	1	1
Total Balls		16	36	16	36