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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128b1-an

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended Reading

- XMEGA B Manual
- XMEGA Application Notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA B Manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentations are available from www.atmel.com/avr.

5. Capacitive Touch Sensing

The Atmel QTouch® library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

The Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers and SRAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for save storing of nonvolatile data in the program memory.

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic are supported, and the instruction set allows for efficient implementation of 32-bit arithmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 69.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1 on page 14.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes for XMEGA B1 Devices

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega64B1	52	96	1E
ATxmega128B1	4D	97	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (i.e., if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

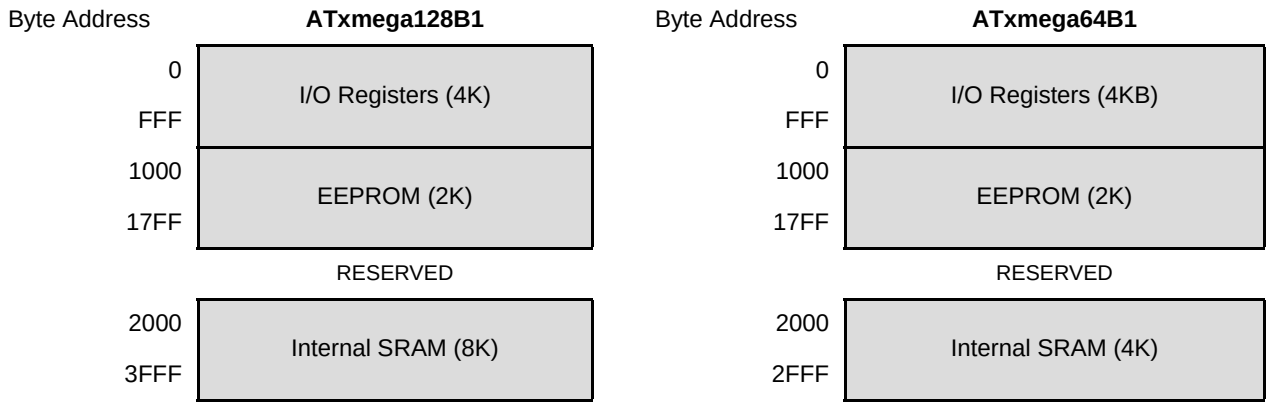
An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are re-programmable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM and optionally memory mapped EEPROM. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM, and SRAM will always have the same start addresses for all XMEGA devices.

Figure 7-2. Data Memory Map (hexadecimal address)



7.6 EEPROM

Atmel AVR XMEGA B1 devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

7.7 I/O Memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which are used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range of 0x00 to 0x3F directly. In the address range 0x00 - 0x1F, single-cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules in XMEGA B1 is shown in the “Peripheral Module Address Map” on page 60.

7.7.1 General Purpose I/O Registers

The lowest four I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

7.8 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the different bus masters (CPU, DMA controller read, and DMA controller write, etc.) can access different memory sections at the same time.

7.9 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. For burst read (DMA), new data are available every cycle. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

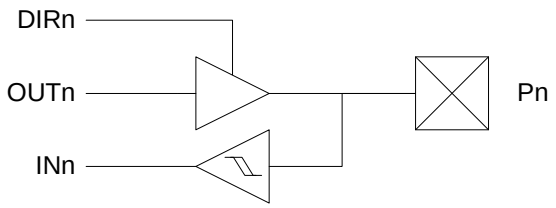
7.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

Program address (Base address)	Source	Interrupt description
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x03E	USB_INT_base	USB on port D Interrupt base
0x046	LCD_INT_base	LCD Interrupt base
0x048	AES_INT_vect	AES Interrupt vector
0x04A	NVM_INT_base	Non-Volatile Memory Interrupt base
0x04E	PORTB_INT_base	Port B Interrupt base
0x052	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x058	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x060	PORTD_INT_base	Port D Interrupt base
0x064	PORTG_INT_base	Port G Interrupt base
0x068	PORTM_INT_base	Port M Interrupt base
0x06C	PORTE_INT_base	Port E Interrupt base
0x074	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x08A	USARTE0_INT_base	USART 0 on port E Interrupt base
0x096	PORTA_INT_base	Port A Interrupt base
0x09A	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x0A0	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base

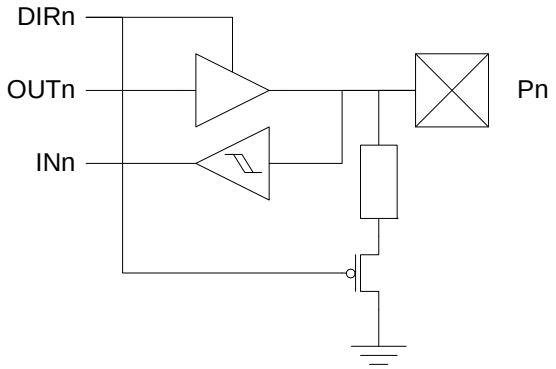
15.3.1 Push-pull

Figure 15-1. I/O Configuration - Totem-pole



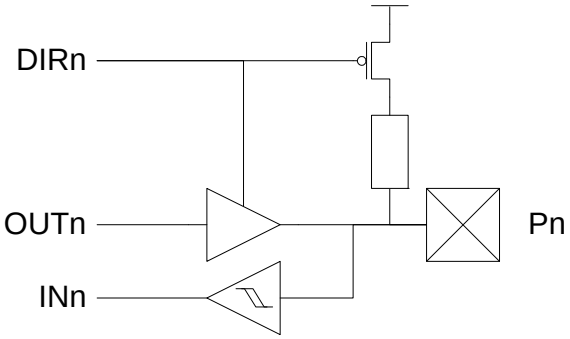
15.3.2 Pull-down

Figure 15-2. I/O Configuration - Totem-pole with Pull-down (on Input)



15.3.3 Pull-up

Figure 15-3. I/O Configuration - Totem-pole with Pull-up (on Input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

19. Hi-Res – High Resolution Extension

19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

Atmel AVR XMEGA B1 devices have one Hi-Res Extension that can be enabled for the timer/counters pair on PORTC. The notation of this is HIRESC.

32. Pinout and Pin Functions

The device pinout is shown in “Pinout/Block Diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

32.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

32.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground
AGND	Analog Ground

32.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

32.1.3 Analog Functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
AREF	Analog Reference input pin

32.1.4 LCD Functions

SEGn	LCD Segment Drive Output n
COMn	LCD Common Drive Output n
VLCD	LCD Voltage Multiplier Output
BIAS2	LCD Intermediate Voltage 2 Output (VLCD * 2/3)
BIAS1	LCD Intermediate Voltage 1 Output (VLCD * 1/3)
CAPH	LCD High End Of Flying Capacitor
CAPL	LCD Low End Of Flying Capacitor

Table 32-6. Port E - Alternate Functions

PORT E	PIN #	INTERRUPT	TCE0 (1)	USARTE0 (2)	CLOCKOUT (4)	EVENTOUT (5)	Alternate TOSC
PE0	19	SYNC	OC0A				
PE1	20	SYNC	OC0B	XCK0			
PE2	21	SYNC/ASYNC	OC0C	RXD0			
PE3	22	SYNC	OC0D	TXD0			
PE4	23	SYNC					
PE5	24	SYNC					
PE6	25	SYNC					TOSC2
PE7	26	SYNC			clk_{PER}	EVOUT	TOSC1

Table 32-7. LCD

LCD (1)(2)	PIN #	INTERRUPT (1)	GPIO (1)	BLINK (1)
GND	27			
VCC	28			
SEG39	29	SYNC	PG0	
SEG38	30	SYNC	PG1	
SEG37	31	SYNC/ASYNC	PG2	
SEG36	32	SYNC	PG3	
SEG35	33	SYNC	PG4	
SEG34	34	SYNC	PG5	
SEG33	35	SYNC	PG6	
SEG32	36	SYNC	PG7	
SEG31	37	SYNC	PM0	
SEG30	38	SYNC	PM1	
SEG29	39	SYNC/ASYNC	PM2	
SEG28	40	SYNC	PM3	
SEG27	41	SYNC	PM4	
SEG26	42	SYNC	PM5	
SEG25	43	SYNC	PM6	
SEG24	44	SYNC	PM7	
SEG23	45			
SEG22	46			
SEG21	47			
SEG20	48			
SEG19	49			

36.10 Brownout Detection Characteristics

Table 36-15. Brownout Detection Characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	BOD level 0 falling V_{CC}	T = 85°C, calibrated	1.5	1.6	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.6		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

36.11 External Reset Characteristics

Table 36-16. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width			90	1000	ns
V_{RST}	Reset threshold voltage	V_{CC} = 2.7 - 3.6V		0.50*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.40*V_{CC}		

36.12 Power-on Reset Characteristics

Table 36-17. Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-}(1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.3		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	V

Note: 1. Both V_{POT-} values are only valid when BOD is disabled. When BOD is enabled the µBOD is enabled, and V_{POT-} =V_{POT+}.

36.14.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 36-21. Calibrated 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.22		%

36.14.3 Calibrated and tunable 32MHz Internal Oscillator Characteristics

Table 36-22. Calibrated 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		35	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.23		%

36.14.4 32kHz Internal ULP Oscillator Characteristics

Table 36-23. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%

36.14.5 Phase Locked Loop (PLL) Characteristics

Table 36-24. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency(1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			23	100	µs
	re-lock time			20	50	µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.15 SPI Characteristics

Figure 36-5. SPI Timing Requirements in Master Mode

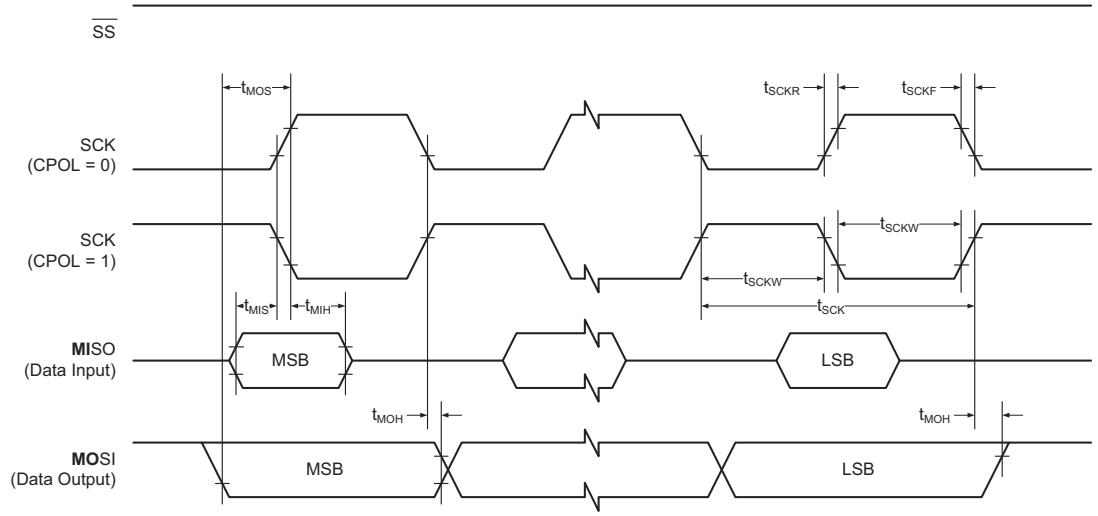
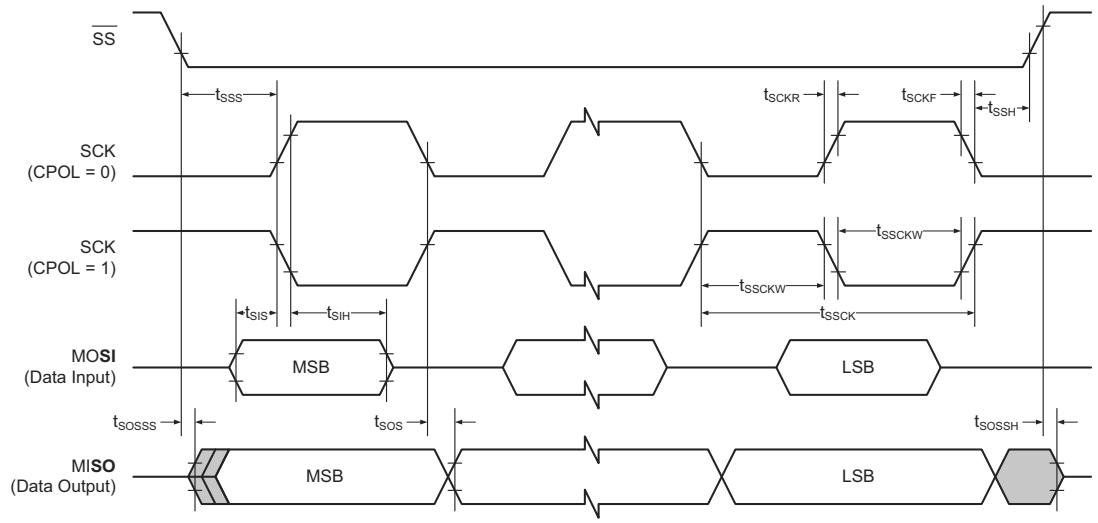


Figure 36-6. SPI Timing Requirements in Slave Mode



36.16 Two-wire Interface Characteristics

Table 36-30 describes the requirements for devices connected to the Two-wire Serial Bus. The Atmel AVR XMEGA Two-wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-7.

Figure 36-7. Two-wire Interface Bus Timing

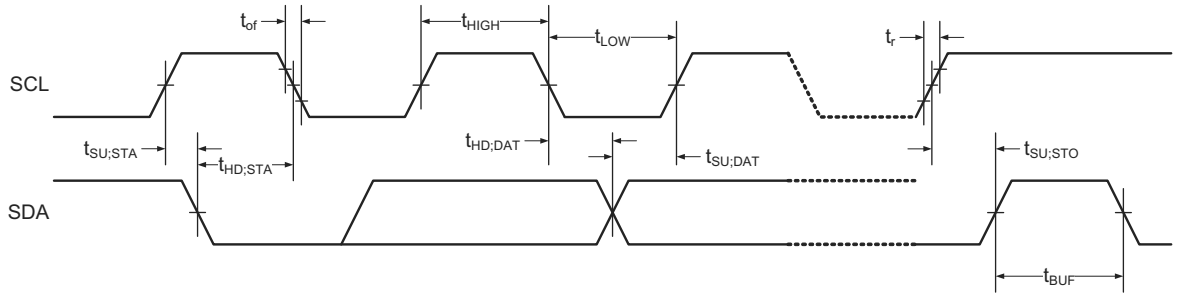


Table 36-30. Two-wire Serial Bus Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input low voltage		-0.5		0.3*V_{CC}	
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05V_{CC}[1]		0	
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		20+0.1C_b[1][2]		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF[2]	20+0.1C_b[1][2]		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	0.1V_{CC} < V_I < 0.9V_{CC}	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER}[3]>max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq$ 100kHz	$\frac{V_{CC}-0.4V}{3mA}$	$\frac{100ns}{C_b}$	$\frac{300ns}{C_b}$	Ω
		f_{SCL} > 100kHz				
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq$ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq$ 100kHz	4.0			
		f_{SCL} > 100kHz	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq$ 100kHz	0		3.5	
		f_{SCL} > 100kHz	0		0.9	

Figure 37-5. Active Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

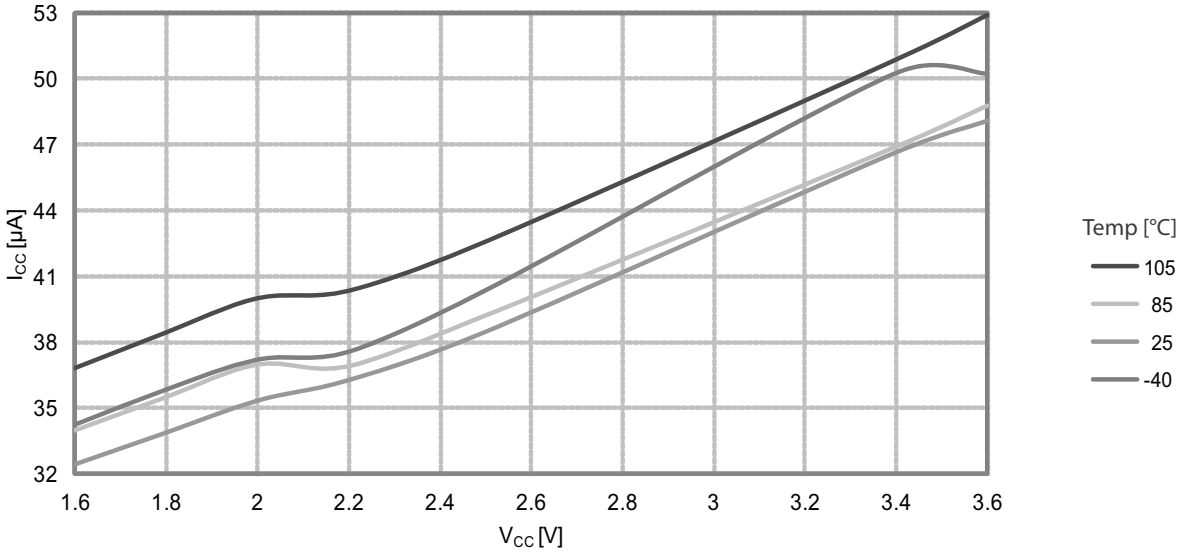


Figure 37-6. Active Mode Supply Current vs. V_{CC}

***f_{SYS} = 32MHz internal oscillator*.**

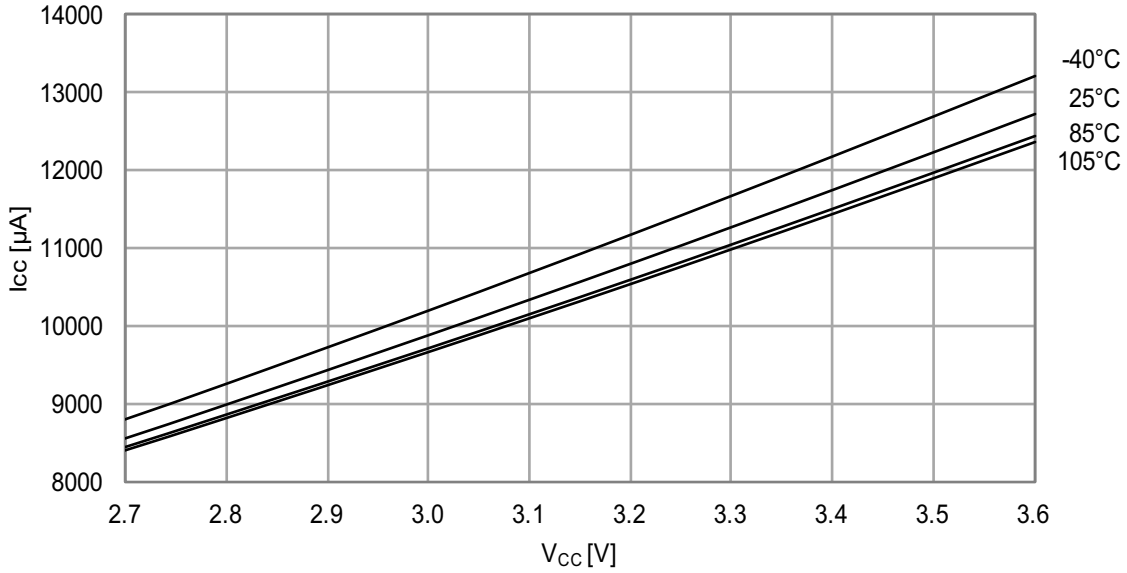


Figure 37-39. ADC Gain Error vs. V_{CC}.

Differential signed mode, external reference.

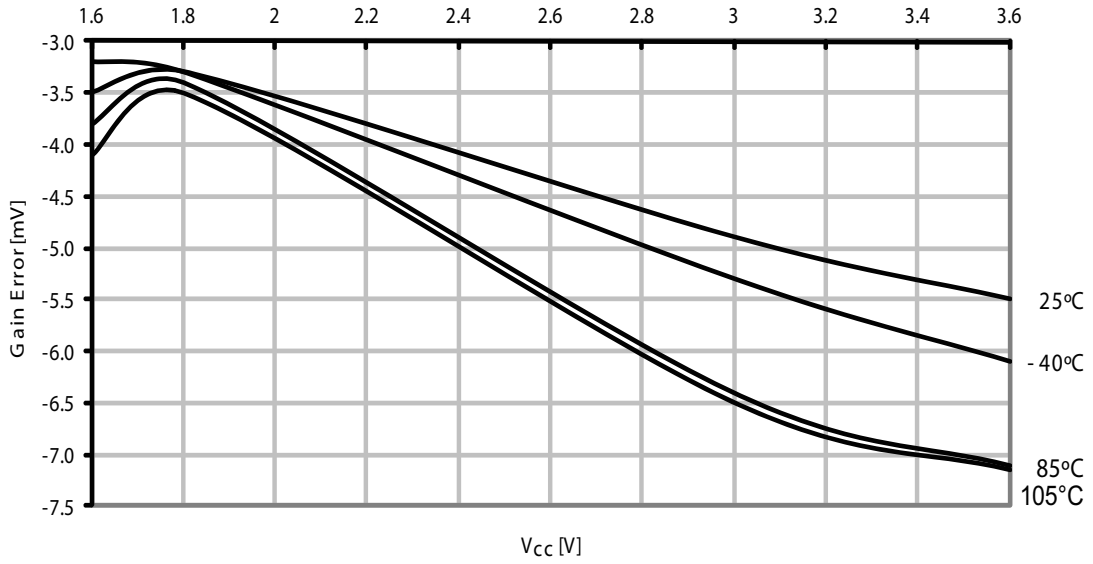
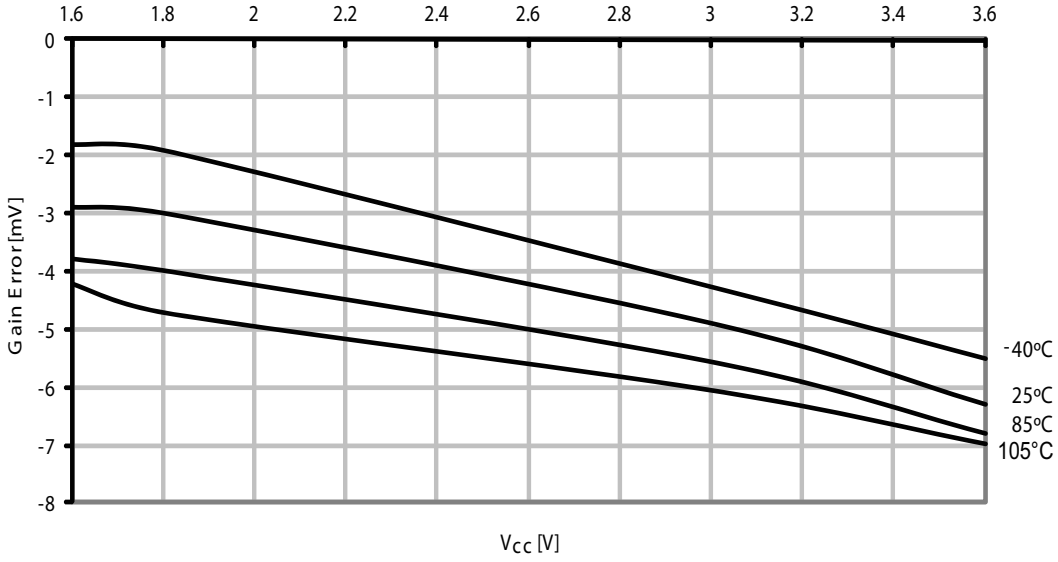


Figure 37-40. ADC Gain Error vs. V_{CC}.

SE Unsigned mode, external reference.



37.6 BOD Characteristics

Figure 37-51. BOD Thresholds vs. Temperature

***BOD level = 1.6V*.**

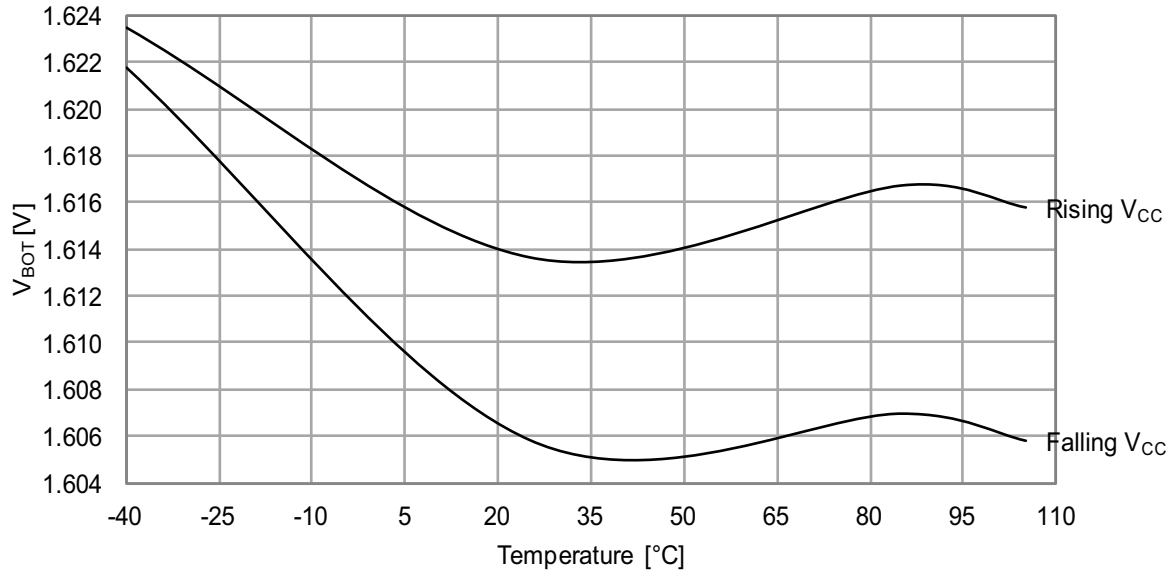
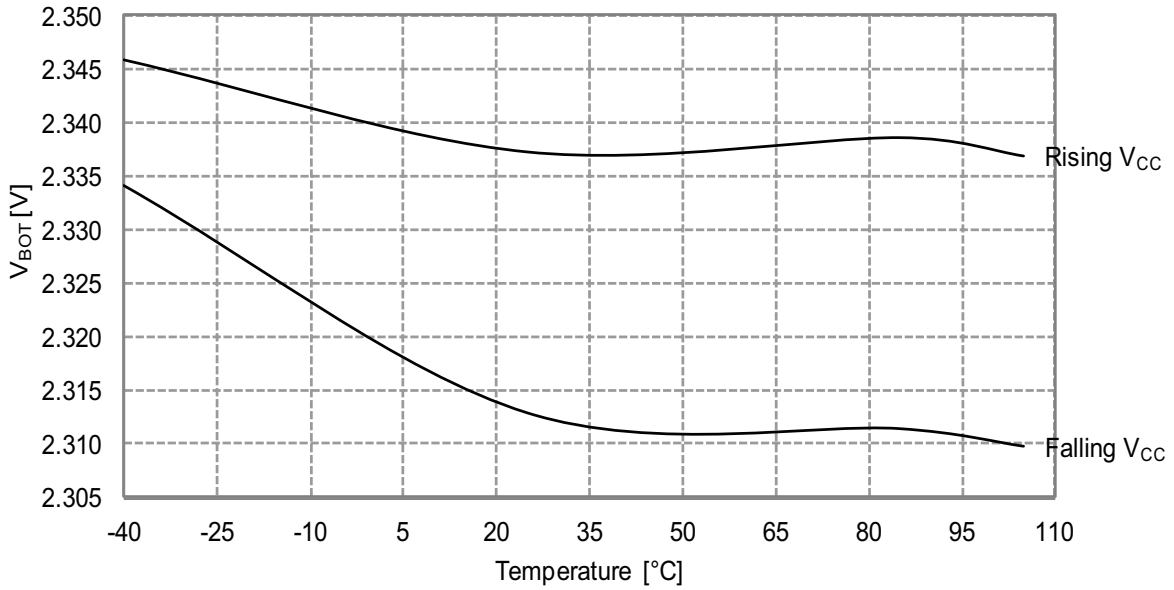


Figure 37-52. BOD Thresholds vs. Temperature

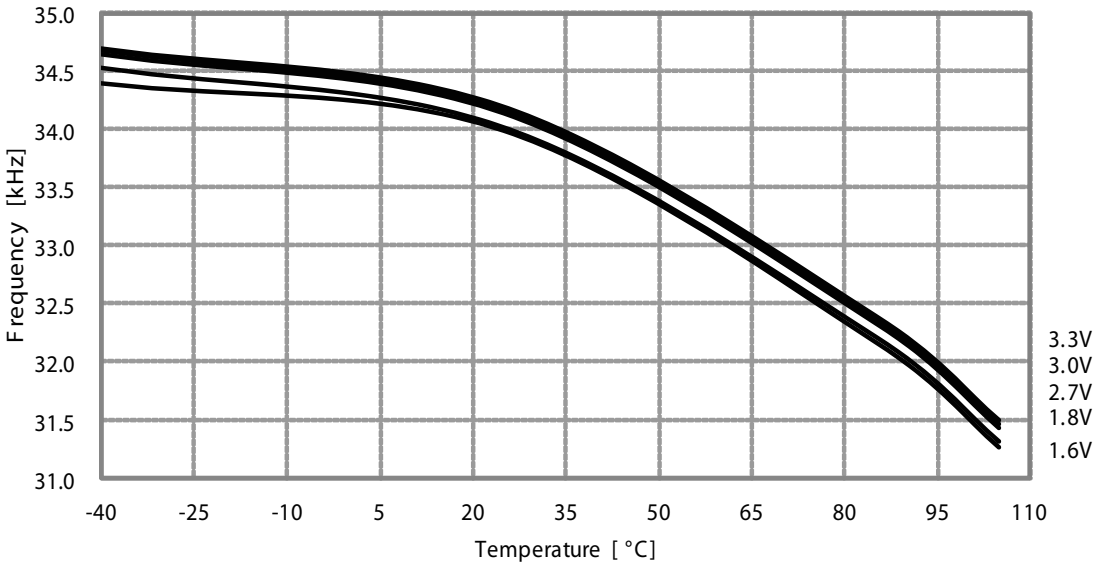
***BOD level = 2.2V*.**



37.8 Oscillator Characteristics

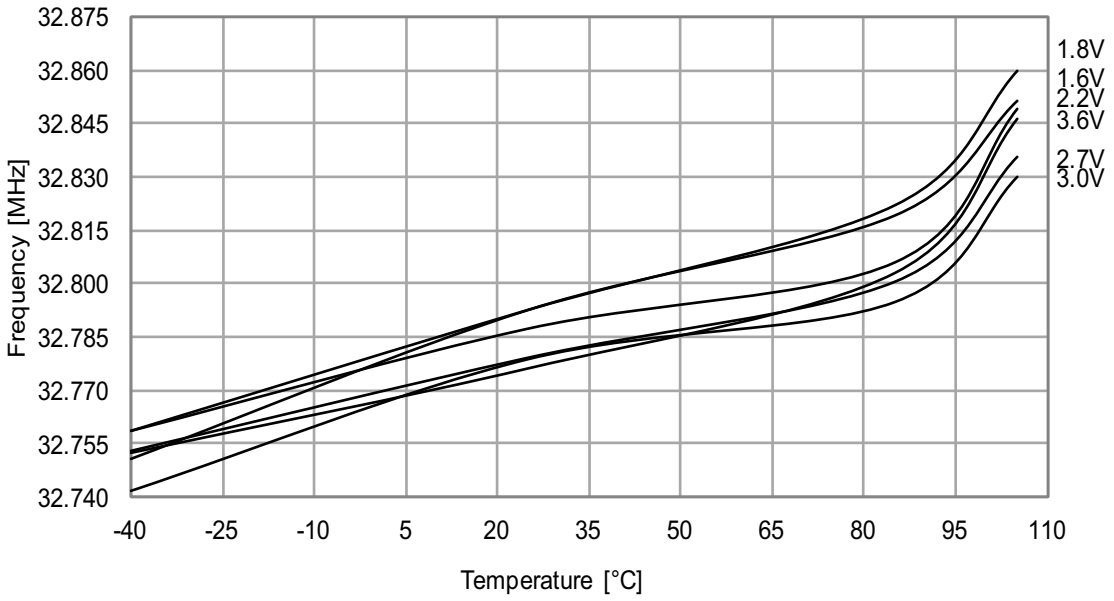
37.8.1 Ultra Low-power Internal Oscillator

Figure 37-62. Ultra Low-power Internal Oscillator Frequency vs. Temperature.



37.8.2 32.768kHz Internal Oscillator

Figure 37-63. 32.768kHz Internal Oscillator Frequency vs. Temperature.



37.8.3 2MHz Internal Oscillator

Figure 37-66. 2MHz Internal Oscillator Frequency vs. Temperature
***DFLL disabled*.**

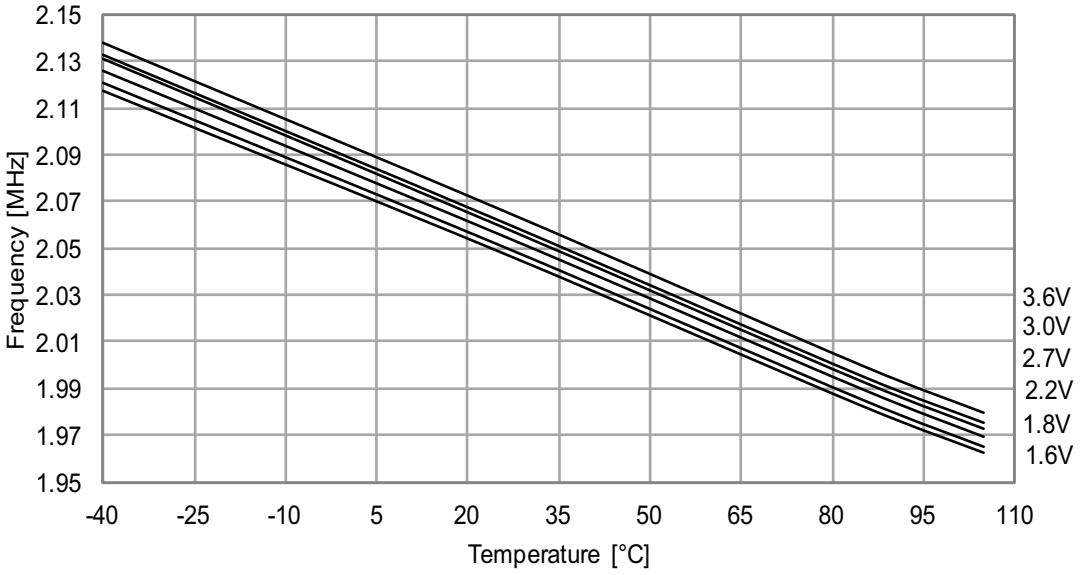


Figure 37-67. 2MHz Internal Oscillator Frequency vs. Temperature
***DFLL enabled*.**

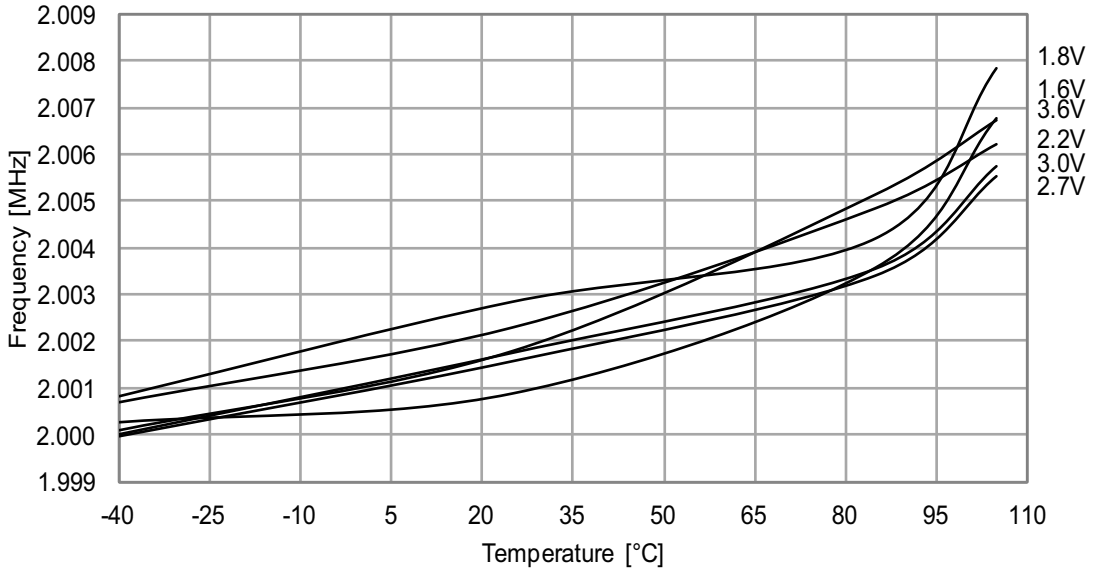


Figure 37-85. I_{CC} vs. Contrast

32Hz Low Power Frame Rate from 32.768kHz TOSC, w/o pixel load, V_{CC} = 3.0V.

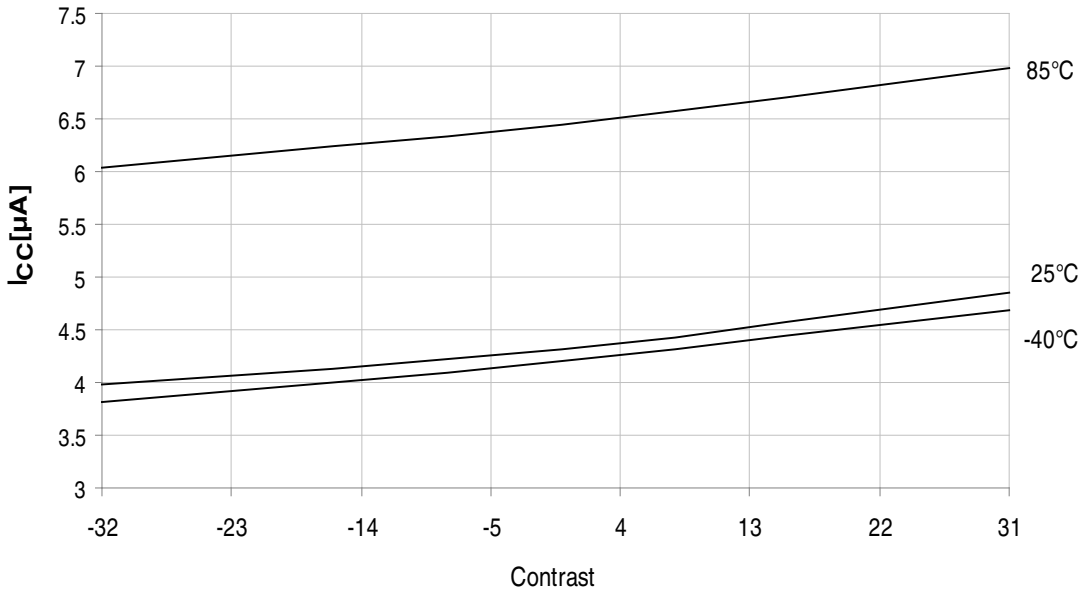


Figure 37-86. P_{SAVE} LCD LP 32Hz vs. Temperature