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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128b1-au

Figure 2-2. VFBGA Pinout

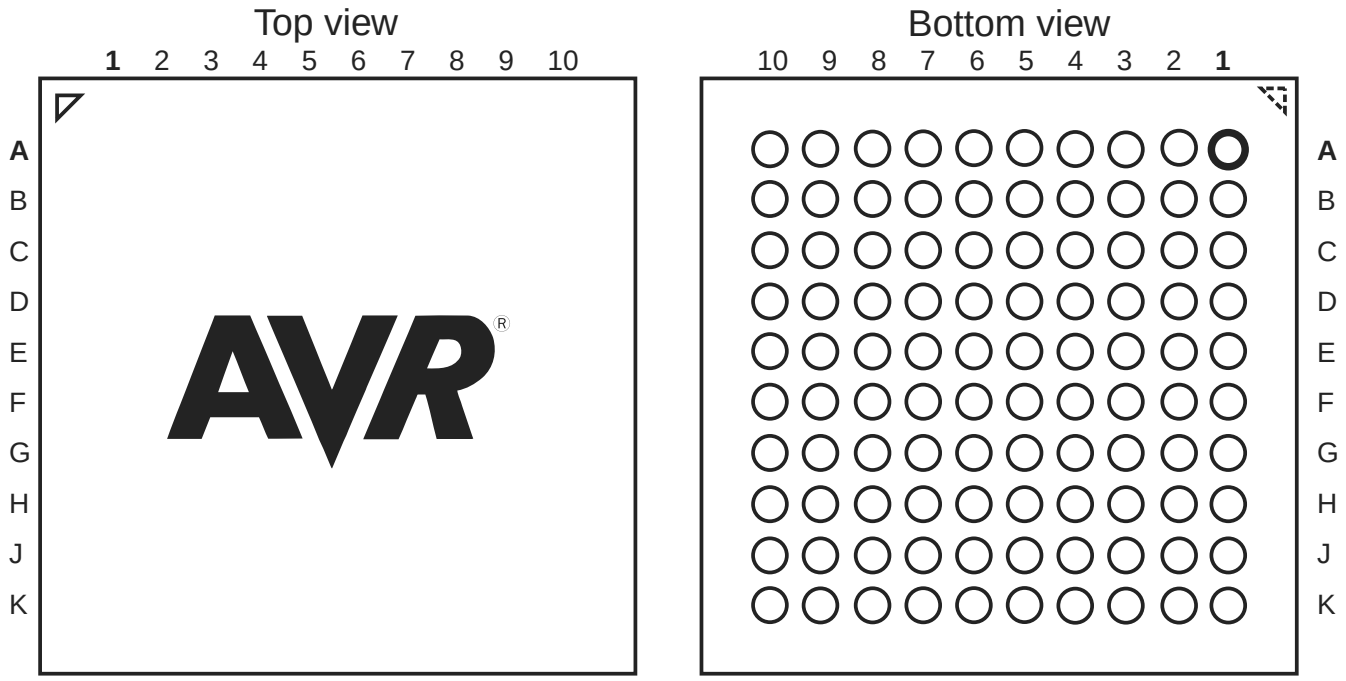


Table 2-1. VFBGA Pinout

	1	2	3	4	5	6	7	8	9	10
A	PC0	VCC	PB6	PB2	AVCC	PA5	PA1	PR1	COM2	CAPH
B	PC3	GND	PB7	PB4	AGND	PA4	PA0	PR0	COM1	CAPL
C	PC5	PC4	PC1	PB5	PA7	PA3	COM3	COM0	BIAS2	BIAS1
D	VCC	GND	PD0	PC2	PB0	PA6	SEG0	VLCD	GND	VCC
E	PD2	PDI/ RESET	PD1	PC6	PB1	PA2	SEG1	SEG4	SEG3	SEG2
F	VCC	GND	PDI	PC7	PB3	PM2/ SEG29	SEG10	SEG7	SEG6	SEG5
G	PE2	PE1	PE3	PE0	PE4	SEG23	SEG15	SEG13	SEG9	SEG8
H	PE5	PE6	PG1/ SEG38	PG4/ SEG35	PG7/ SEG32	PM5/ SEG26	SEG21	SEG18	SEG12	SEG11
J	PE7	PG0/ SEG39	PG3/ SEG36	PG6/ SEG33	PM1/ SEG30	PM4/ SEG27	PM7/ SEG24	SEG20	SEG16	SEG14
K	GND	VCC	PG2/ SEG37	PG5/ SEG34	PM0/ SEG31	PM3/ SEG28	PM6/ SEG25	SEG22	SEG19	SEG17

6.5 Program Flow

After reset, the CPU starts to execute instructions from the lowest address in the flash program memory '0.' The program counter (PC) addresses the next instruction to be fetched.

Program flow is provided by conditional and unconditional jump and call instructions capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number use a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the stack. The stack is allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. After reset, the stack pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

6.6 Status Register

The status register (SREG) contains information about the result of the most recently executed arithmetic or logic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the status register is updated after all ALU operations, as specified in the instruction set reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The status register is not automatically stored when entering an interrupt routine nor restored when returning from an interrupt. This must be handled by software.

The status register is accessible in the I/O memory space.

6.7 Stack and Stack Pointer

The stack is used for storing return addresses after interrupts and subroutine calls. It can also be used for storing temporary data. The stack pointer (SP) register always points to the top of the stack. It is implemented as two 8-bit registers that are accessible in the I/O memory space. Data are pushed and popped from the stack using the PUSH and POP instructions. The stack grows from a higher memory location to a lower memory location. This implies that pushing data onto the stack decreases the SP, and popping data off the stack increases the SP. The SP is automatically loaded after reset, and the initial value is the highest address of the internal SRAM. If the SP is changed, it must be set to point above address 0x2000, and it must be defined before any subroutine calls are executed or before interrupts are enabled.

During interrupts or subroutine calls, the return address is automatically pushed on the stack. The return address can be two or three bytes, depending on program memory size of the device. For devices with 128KB or less of program memory, the return address is two bytes, and hence the stack pointer is decremented/incremented by two. For devices with more than 128KB of program memory, the return address is three bytes, and hence the SP is decremented/ incremented by three. The return address is popped off the stack when returning from interrupts using the RETI instruction, and from subroutine calls using the RET instruction.

The SP is decremented by one when data are pushed on the stack with the PUSH instruction, and incremented by one when data is popped off the stack using the POP instruction.

To prevent corruption when updating the stack pointer from software, a write to SPL will automatically disable interrupts for up to four instructions or until the next I/O memory write.

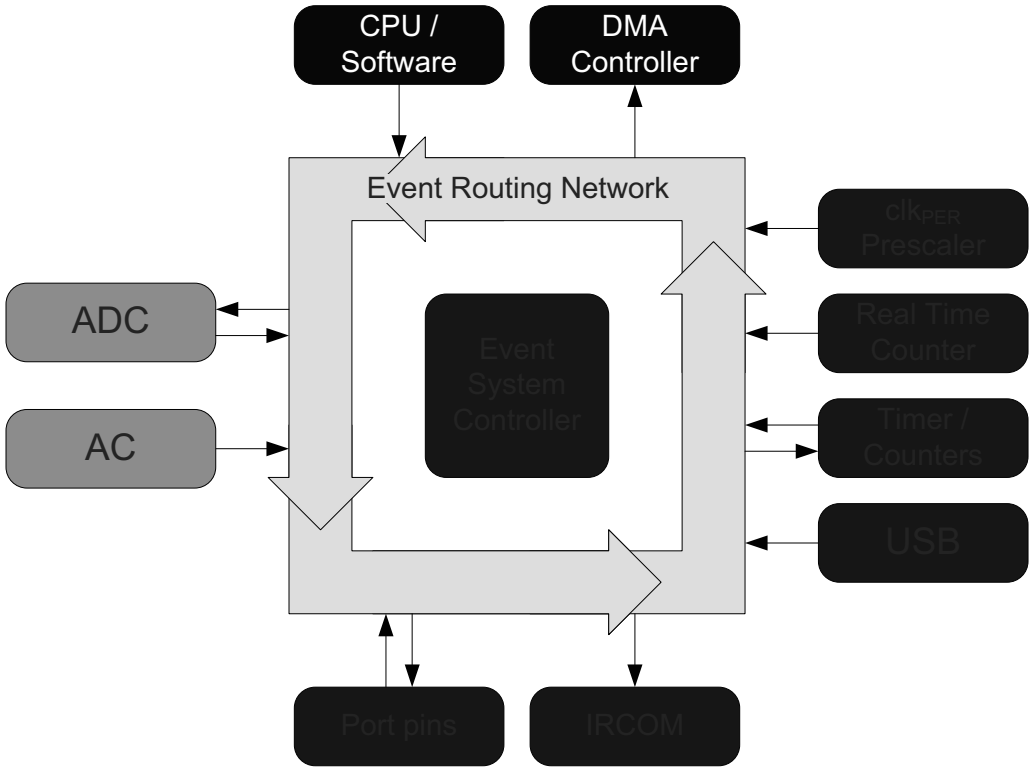
6.8 Register File

The register file consists of 32 x 8-bit general purpose working registers with single clock cycle access time. The register file supports the following input/output schemes:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in flash program memory.

Figure 9-1. Event System Overview and Connected Peripherals

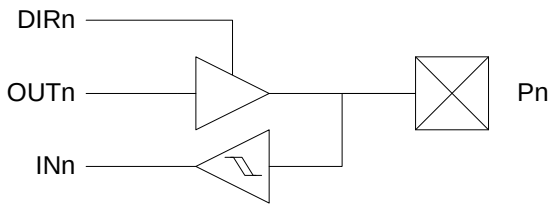


The event routing network consists of four software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to four parallel event configurations and routings. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

Program address (Base address)	Source	Interrupt description
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x03E	USB_INT_base	USB on port D Interrupt base
0x046	LCD_INT_base	LCD Interrupt base
0x048	AES_INT_vect	AES Interrupt vector
0x04A	NVM_INT_base	Non-Volatile Memory Interrupt base
0x04E	PORTB_INT_base	Port B Interrupt base
0x052	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x058	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x060	PORTD_INT_base	Port D Interrupt base
0x064	PORTG_INT_base	Port G Interrupt base
0x068	PORTM_INT_base	Port M Interrupt base
0x06C	PORTE_INT_base	Port E Interrupt base
0x074	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x08A	USARTE0_INT_base	USART 0 on port E Interrupt base
0x096	PORTA_INT_base	Port A Interrupt base
0x09A	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x0A0	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base

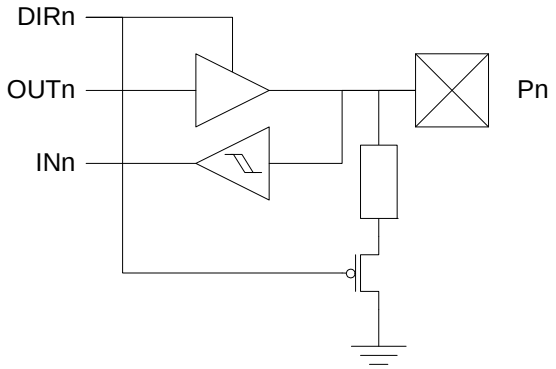
15.3.1 Push-pull

Figure 15-1. I/O Configuration - Totem-pole



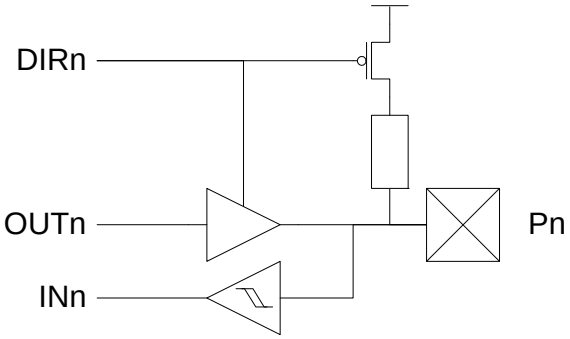
15.3.2 Pull-down

Figure 15-2. I/O Configuration - Totem-pole with Pull-down (on Input)



15.3.3 Pull-up

Figure 15-3. I/O Configuration - Totem-pole with Pull-up (on Input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

16. T/C – 16-bit Timer/Counter Type 0 and 1

16.1 Features

- Three 16-bit timer/counters
  - Two timer/counters of type 0
  - One timer/counters of type 1
- 32-bit Timer/Counter support by cascading two timer/counters
- Up to four compare or capture (CC) channels
  - Four CC channels for timer/counters of type 0
  - Two CC channels for timer/counters of type 1
- Double buffered timer period setting
- Double buffered capture or compare channels
- Waveform generation:
  - Frequency generation
  - Single-slope pulse width modulation
  - Dual-slope pulse width modulation
- Input capture:
  - Input capture with noise cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Timer overflow and error interrupts/events
- One compare match or input capture interrupt/event per CC channel
- Can be used with event system for:
  - Quadrature decoding
  - Count and direction control
  - Capture
- Can be used with DMA and to trigger DMA transactions
- High-resolution extension
  - Increases frequency and waveform resolution by 4x (2-bit) or 8x (3-bit)
- Advanced waveform extension:
  - Low- and high-side output with programmable dead-time insertion (DTI)
- Event controlled fault protection for safe disabling of drivers

16.2 Overview

Atmel AVR XMEGA devices have a set of three flexible 16-bit Timer/Counters (TC). Their capabilities include accurate program execution timing, frequency, and waveform generation, and input capture with time and frequency measurement of digital signals. Two timer/counters can be cascaded to create a 32-bit timer/counter with optional 32-bit capture.

A timer/counter consists of a base counter and a set of compare or capture (CC) channels. The base counter can be used to count clock cycles or events. It has direction control and period setting that can be used for timing. The CC channels can be used together with the base counter to do compare match control, frequency generation, and pulse width waveform modulation, as well as various input capture operations. A timer/counter can be configured for either capture or compare functions, but cannot perform both at the same time.

A timer/counter can be clocked and timed from the peripheral clock with optional prescaling or from the event system. The event system can also be used for direction control and capture trigger or to synchronize operations.

There are two differences between timer/counter type 0 and type 1. Timer/counter 0 has four CC channels, and timer/counter 1 has two CC channels. All information related to CC channels 3 and 4 is valid only for timer/counter 0.

36.3 DC Characteristics

Table 36-4. Current Consumption for Active and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active Power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		150		µA
			V_{CC} = 3.0V		320		
		1MHz, Ext. Clk	V_{CC} = 1.8V		350		
			V_{CC} = 3.0V		700		
		2MHz, Ext. Clk	V_{CC} = 1.8V		650	800	
			V_{CC} = 3.0V		1.0	1.6	mA
		32MHz, Ext. Clk			10	15	
	Idle Power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4.0		µA
			V_{CC} = 3.0V		8.0		
		1MHz, Ext. Clk	V_{CC} = 1.8V		80		
			V_{CC} = 3.0V		150		
		2MHz, Ext. Clk	V_{CC} = 1.8V		160	250	
			V_{CC} = 3.0V		300	600	
		32MHz, Ext. Clk			4.7	7	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			2.1	5	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2	2.5	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3	
		WDT and Sampled BOD enabled, T=85°C			3.1	7	
	Power-save power consumption(2)	RTC on ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC on 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8		
			V_{CC} = 3.0V		0.9		
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		1.3		
			V_{CC} = 3.0V		1.6		

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
	Gain error	Differential mode	External reference		-5		mV
			AV_{CC}/1.6		-5		
			AV_{CC}/2.0		-6		
			Bandgap		±10		
			Temperature drift		0.02		mV/K
			Operating voltage drift		2		mV/V
	Gain error	Single ended unsigned mode	External reference		-8		mV
			AV_{CC}/1.6		-8		
			AV_{CC}/2.0		-8		
			Bandgap		±10		
			Temperature drift		0.03		mV/K
			Operating voltage drift		2		mV/V

Notes: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 10% to 90% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 36-12. Gain Stage Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode		4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode		4.4		pF
	Signal range	Gain stage output	0		AV_{CC}- 0.3	V
	Propagation delay	ADC conversion rate		1		Clk_{ADC} cycles
	Clock rate	Same as ADC	100		1800	kHz
	Gain error	0.5x gain, normal mode		-1		%
		1x gain, normal mode		-1		
		8x gain, normal mode		-1		
		64x gain, normal mode		10		
	Offset error, input referred	0.5x gain, normal mode		10		mV
		1x gain, normal mode		10		
		8x gain, normal mode		-20		
		64x gain, normal mode		-150		

36.13 Flash and EEPROM Memory Characteristics

Table 36-18. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	100K			Cycle
			85°C	100K			
		Data retention	25°C	100			Year
			55°C	25			

Table 36-19. Programming Time

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
	Chip Erase	128KB flash, EEPROM(2)		75		ms
		64KB flash, EEPROM(2)		55		
	Flash	Page Erase		4		ms
		Page Write		4		
		Page Write Automatic Page Erase and Write		8		
	EEPROM	Page Erase		4		ms
		Page Write		4		
		Page Write Automatic Page Erase and Write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

36.14 Clock and Oscillator Characteristics

36.14.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 36-20. Calibrated 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibrated accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

Table 36-26. External Clock with Prescaler(1) for System Clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency(2)	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock high time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock low time	V_{CC} = 1.6 - 1.8V	4.5			
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.14.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 36-27. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0, FRQRANGE=0		0		ns
		XOSCPWR=0, FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1		0		
	Long term jitter	XOSCPWR=0, FRQRANGE=0		0		
		XOSCPWR=0, FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1		0		
	Frequency error	XOSCPWR=0, FRQRANGE=0		0.03		%
		XOSCPWR=0, FRQRANGE=1		0.03		
		XOSCPWR=0, FRQRANGE=2 or 3		0.03		
		XOSCPWR=1		0.03		
	Duty cycle	XOSCPWR=0, FRQRANGE=0		50		
		XOSCPWR=0, FRQRANGE=1		50		
		XOSCPWR=0, FRQRANGE=2 or 3		50		
		XOSCPWR=1		50		

Symbol	Parameter	Condition			Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance					5.9		pF
C_{XTAL2}	Parasitic capacitance					8.3		
C_{LOAD}	Parasitic capacitance load					3.5		

Note: 1. Numbers for negative impedance are not tested but guaranteed from design and characterization.

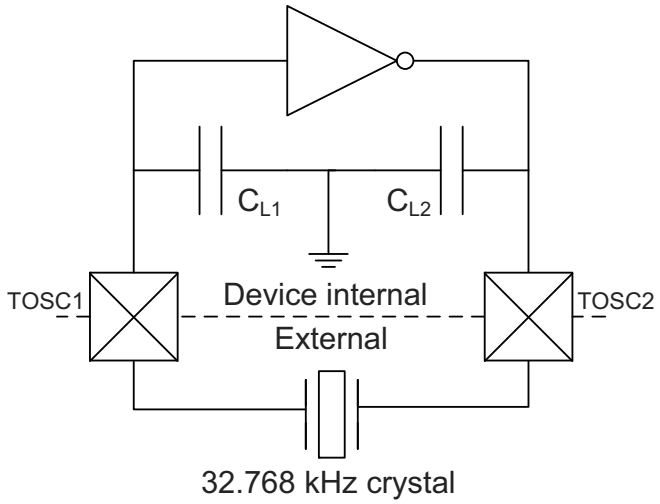
36.14.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 36-28. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12.0pF			28	
C_{IN_TOSC}	Input capacitance between TOSC pins	Normal mode		3.5		pF
		Low power mode		3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			
	Long term Jitter (SIT)			0		%

Note: 1. See Figure 36-4 for definition.

Figure 36-4. TOSC Input Capacitance



The input capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

36.16 Two-wire Interface Characteristics

Table 36-30 describes the requirements for devices connected to the Two-wire Serial Bus. The Atmel AVR XMEGA Two-wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-7.

Figure 36-7. Two-wire Interface Bus Timing

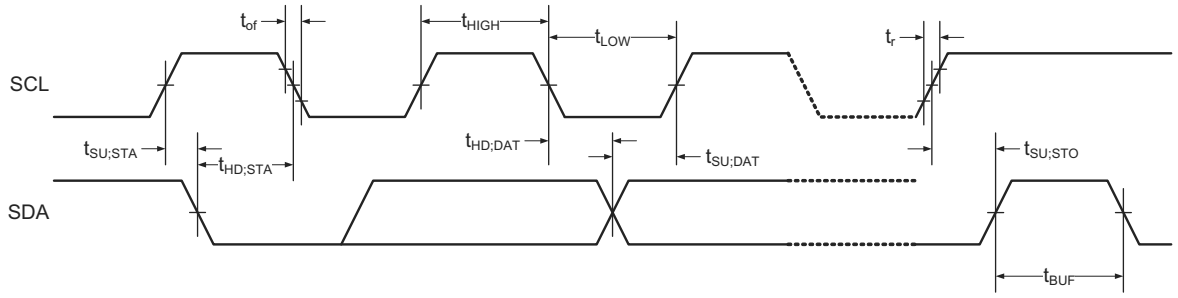
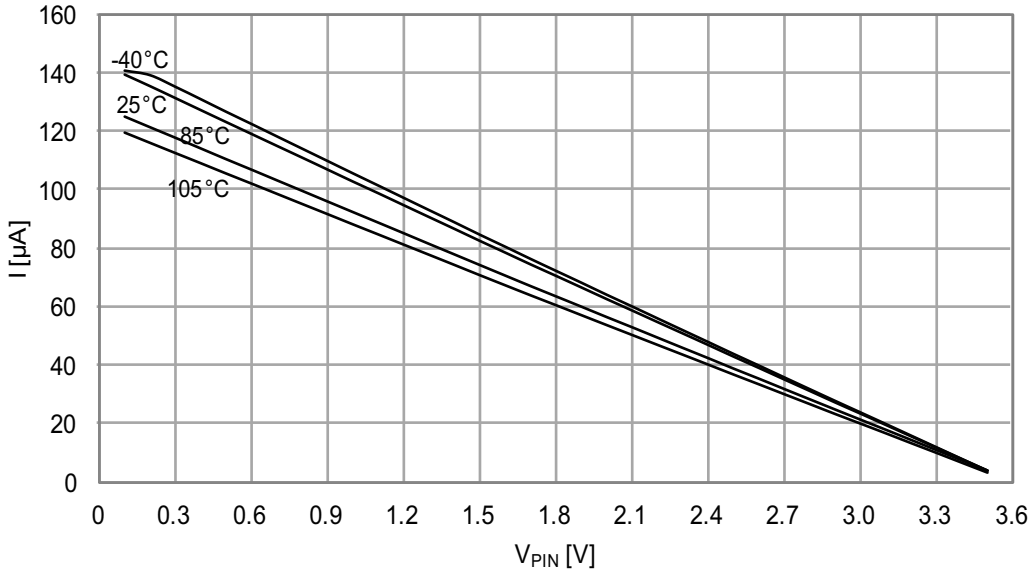


Table 36-30. Two-wire Serial Bus Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input low voltage		-0.5		0.3*V_{CC}	
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05V_{CC}[1]		0	
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		20+0.1C_b[1][2]		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF[2]	20+0.1C_b[1][2]		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	0.1V_{CC} < V_I < 0.9V_{CC}	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER}[3]>max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq$ 100kHz	$\frac{V_{CC}-0.4V}{3mA}$	$\frac{100ns}{C_b}$	$\frac{300ns}{C_b}$	Ω
		f_{SCL} > 100kHz				
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq$ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq$ 100kHz	4.0			
		f_{SCL} > 100kHz	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq$ 100kHz	0		3.5	
		f_{SCL} > 100kHz	0		0.9	

Figure 37-19. I/O Pin Pull-up Resistor Current vs. Pin Voltage

V_{CC} = 3.3V.



37.2.2 Output Voltage vs. Sink/Source Current

Figure 37-20. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V.

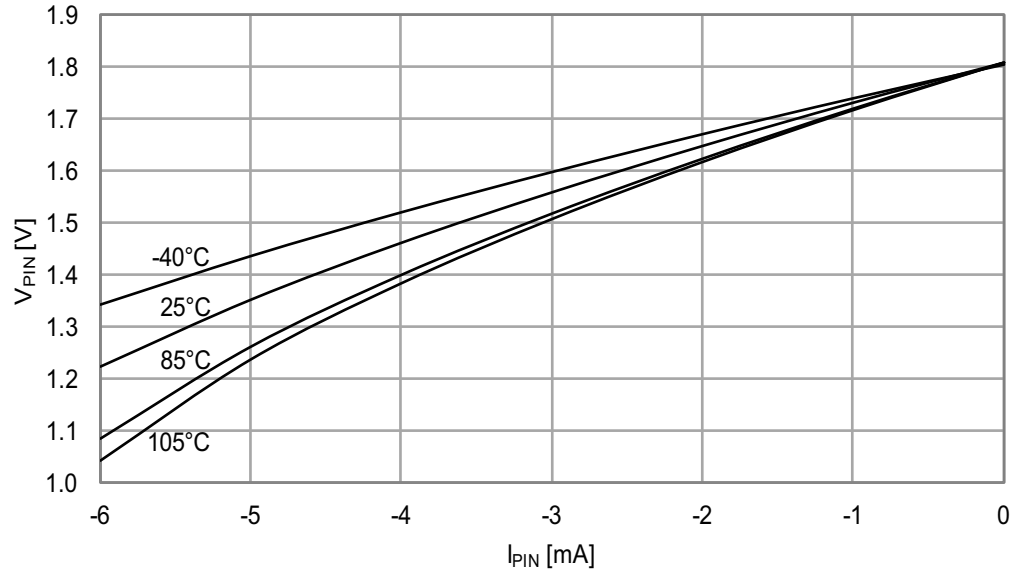
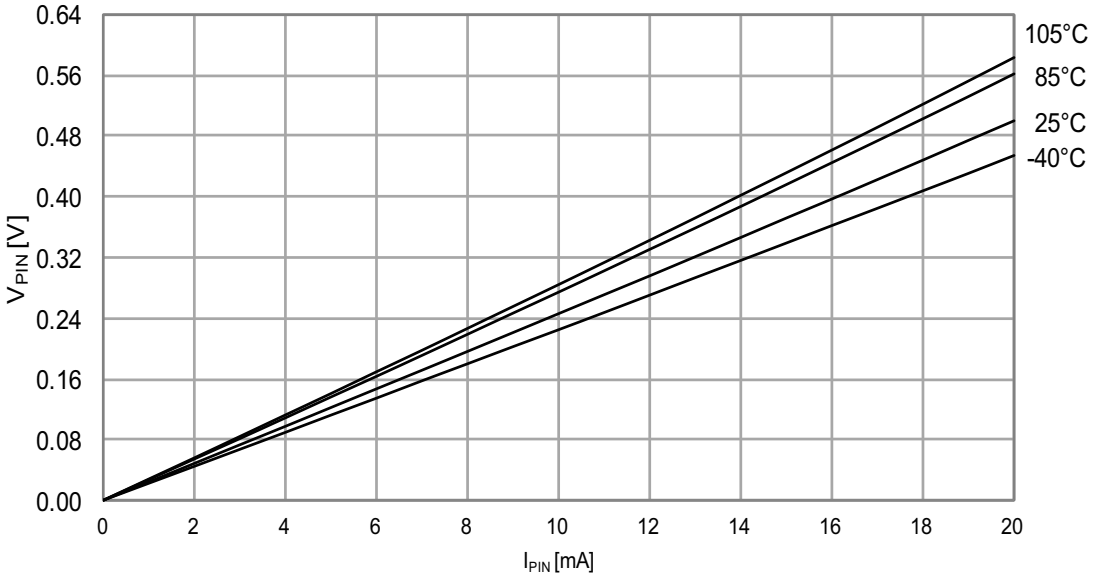


Figure 37-25. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.3V.



37.2.3 Thresholds and Hysteresis

Figure 37-26. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1".

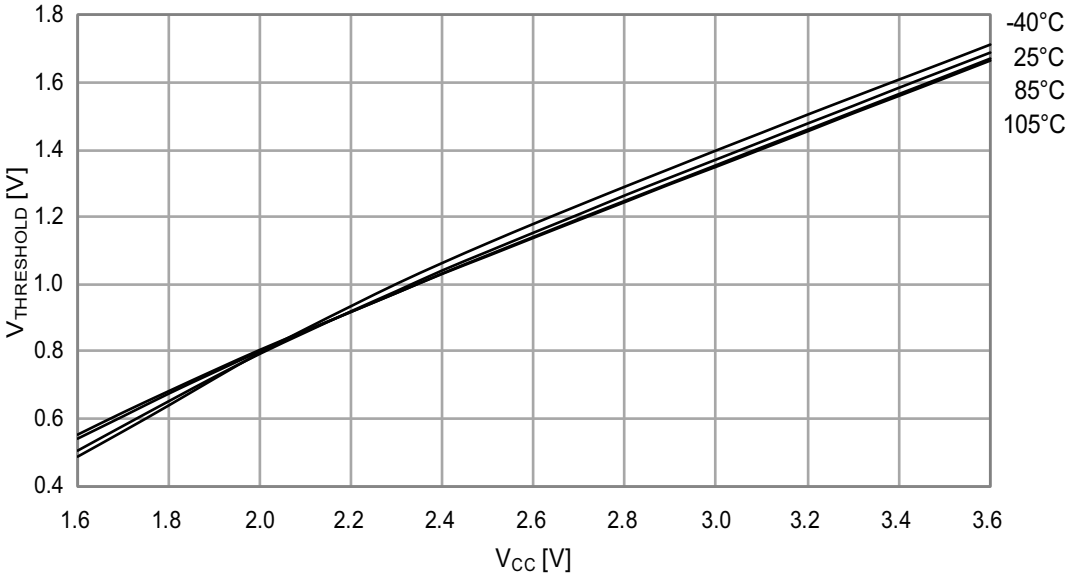


Figure 37-41. ADC Gain Error vs. Temperature

Differential signed mode, external reference.

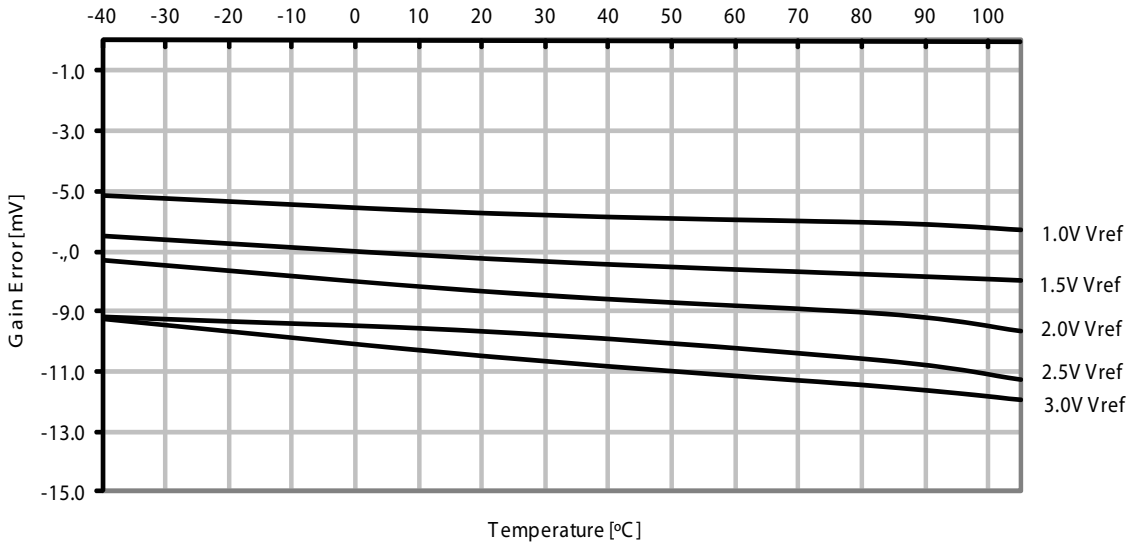


Figure 37-42. ADC Gain Error vs. Temperature

SE Unsigned mode, V_{CC} = 3.6V, external reference.

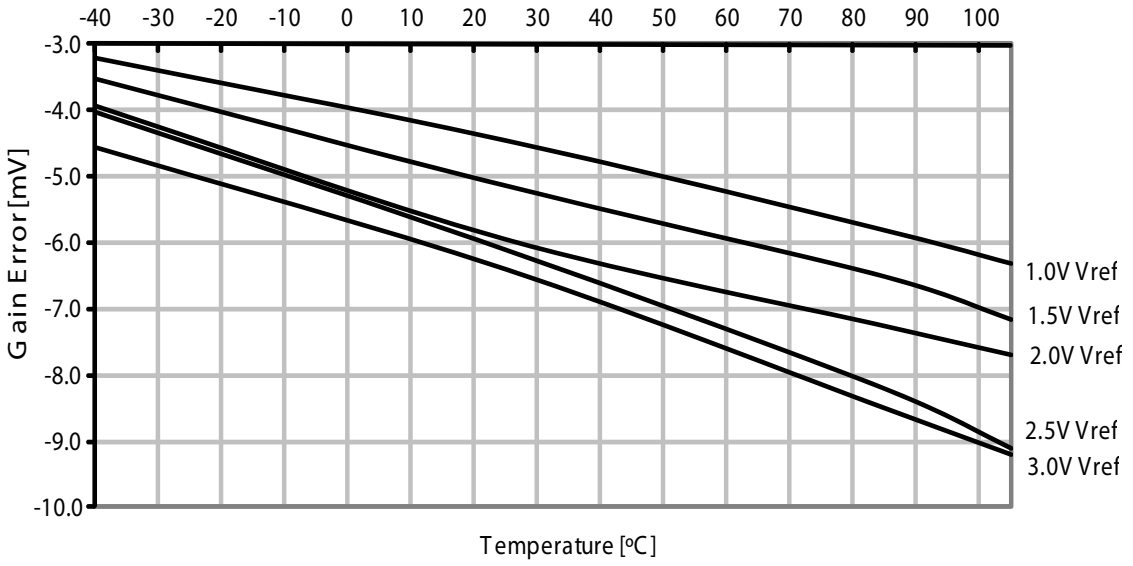
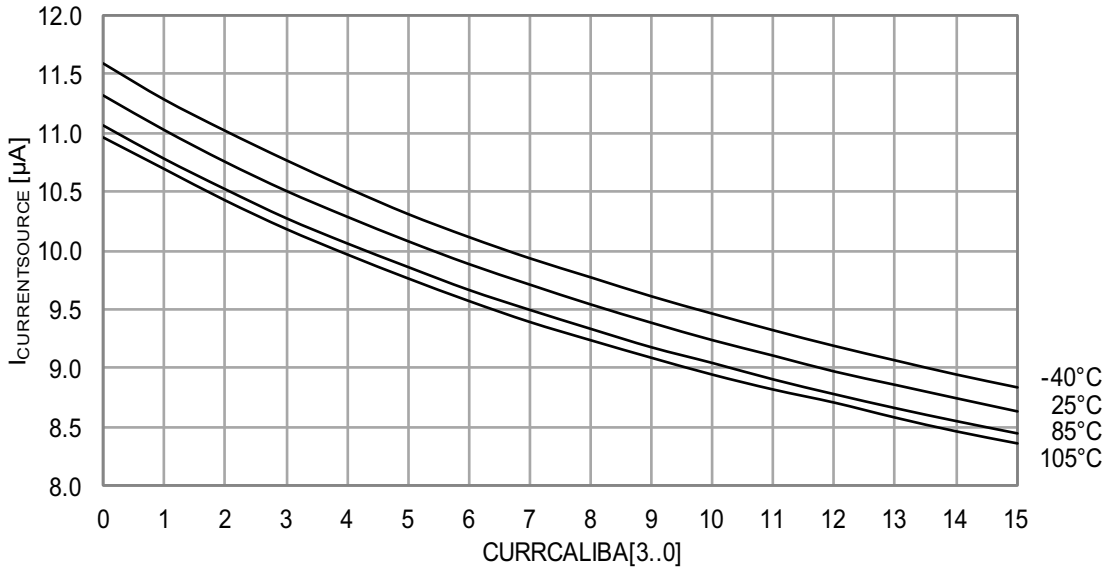


Figure 37-49. Analog Comparator Current Source vs. Calibration

***V_{CC} = 3.0V, double mode*.**



37.5 Internal 1.0V Reference Characteristics

Figure 37-50. ADC/DAC Internal 1.0V Reference vs. Temperature

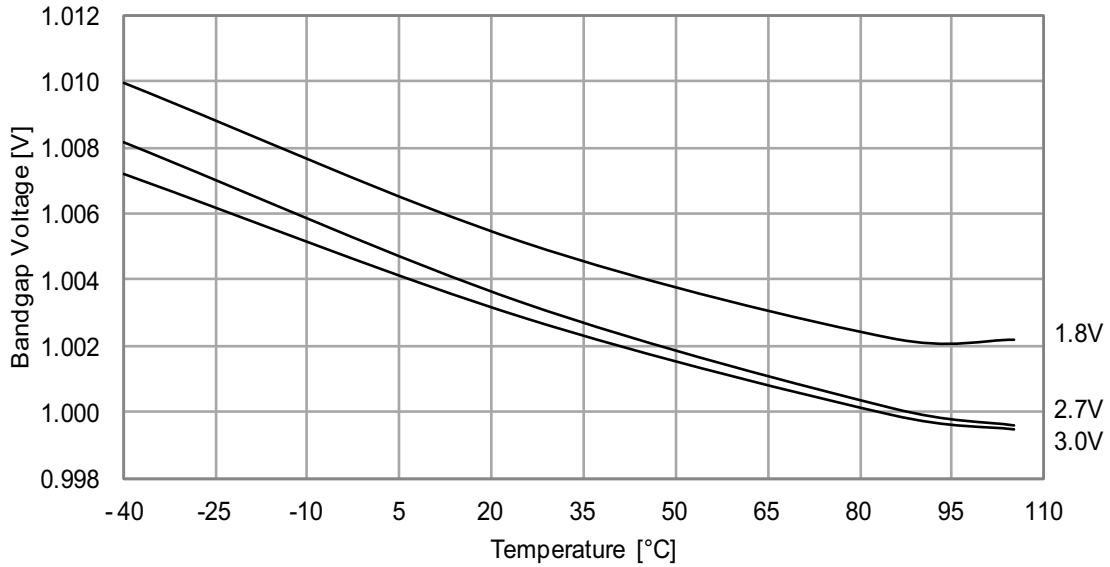
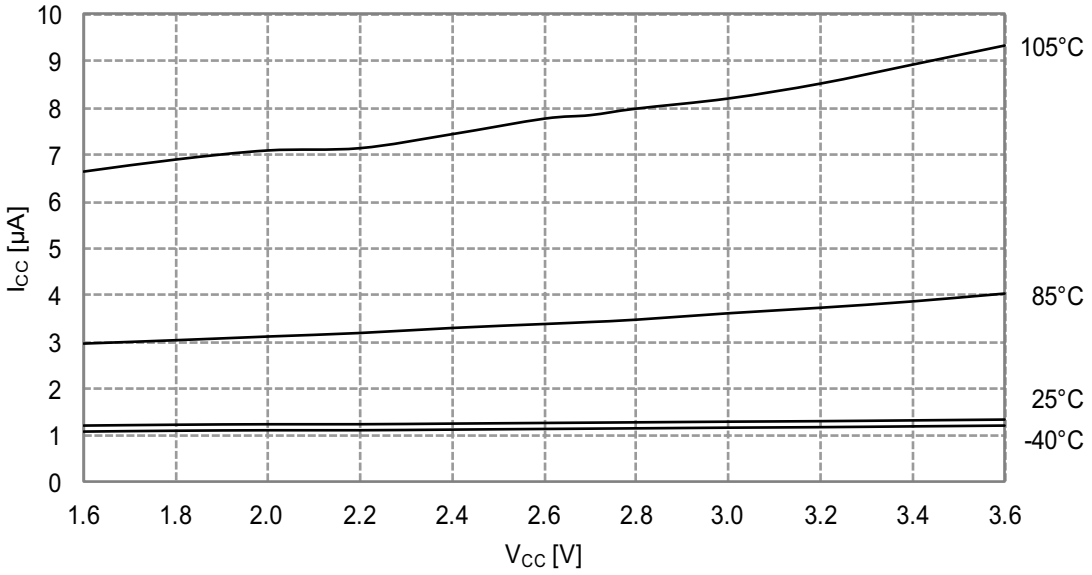


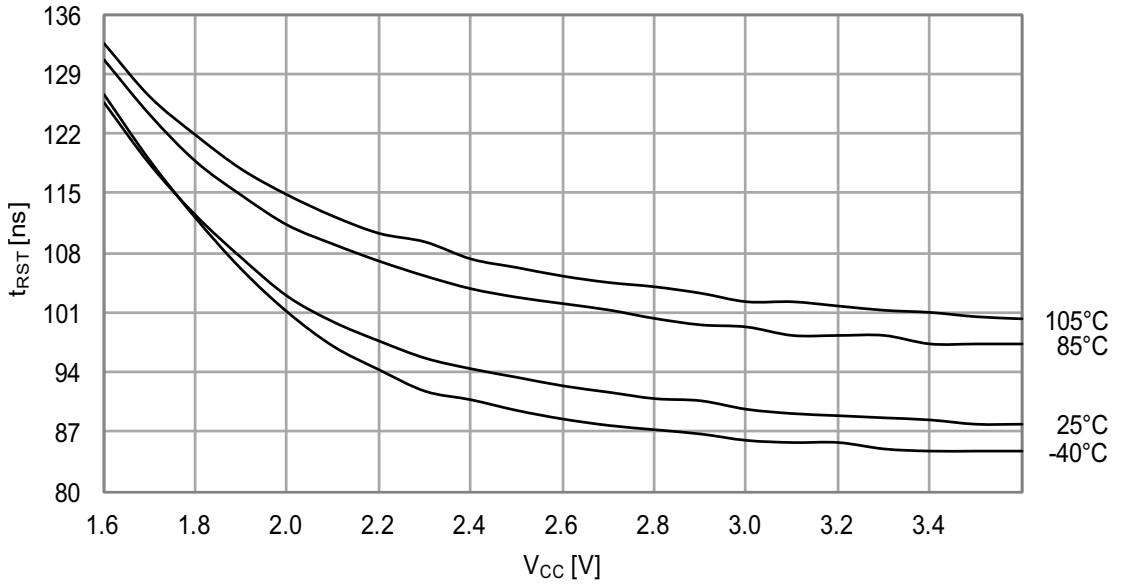
Figure 37-55. BOD Current Consumption vs. V_{CC}

***Sampled mode, BOD level = 1.6V*.**



37.7 External Reset Characteristics

Figure 37-56. Minimum Reset Pin Pulse Width vs. V_{CC}



37.8.4 32MHz Internal Oscillator

Figure 37-70. 32MHz Internal Oscillator Frequency vs. Temperature
DFLL disabled.

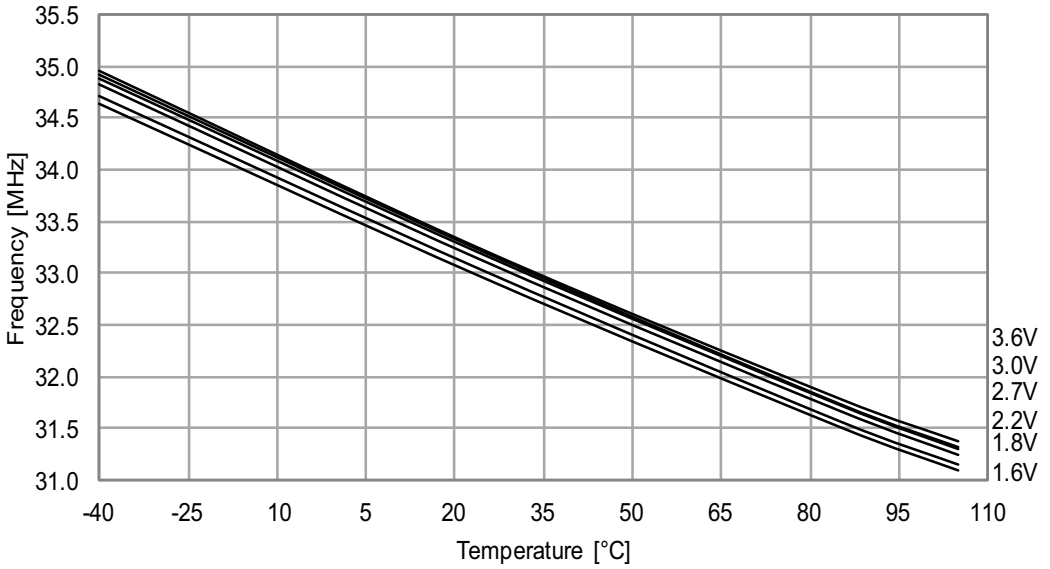
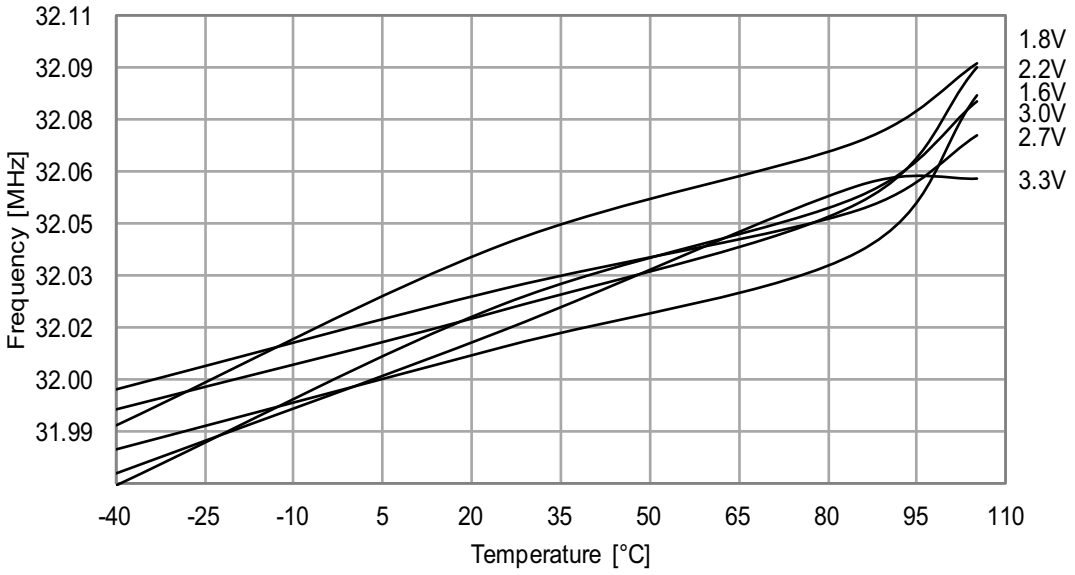


Figure 37-71. 32MHz Internal Oscillator Frequency vs. Temperature
DFLL enabled, from the 32.768kHz internal oscillator.



37.10 LCD Characteristics

Figure 37-81. I_{CC} vs. Frame Rate

32Hz Low Power Frame Rate from 32.768kHz TOSC, w/ and w/o pixel load, V_{CC} = 1.8V, T = 25°C.

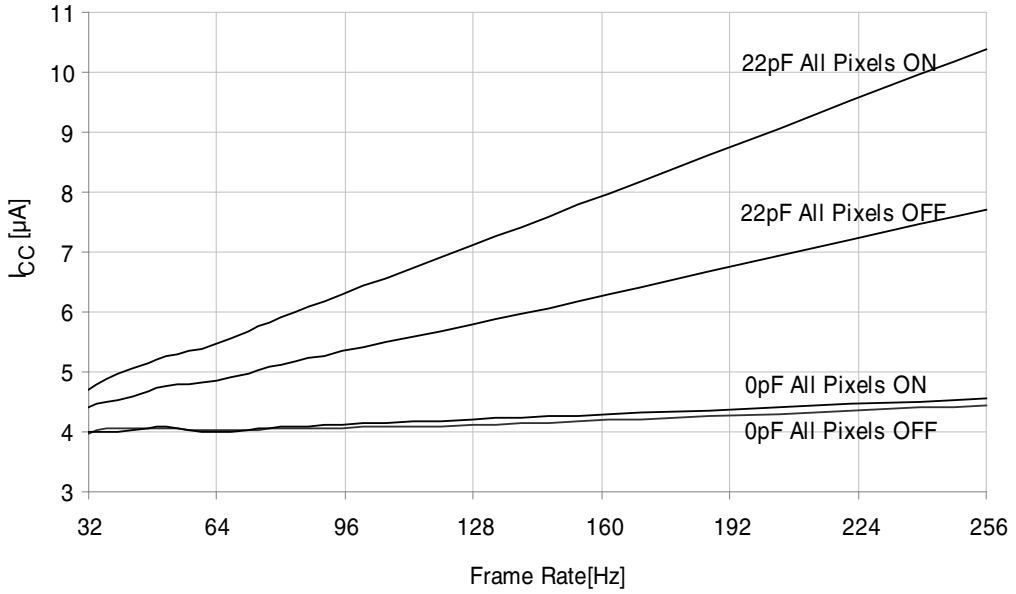


Figure 37-82. I_{CC} vs. Frame Rate

32Hz Low Power Frame Rate from 32.768kHz TOSC, w/ and w/o pixel load, V_{CC} = 3.0V, T = 25°C.

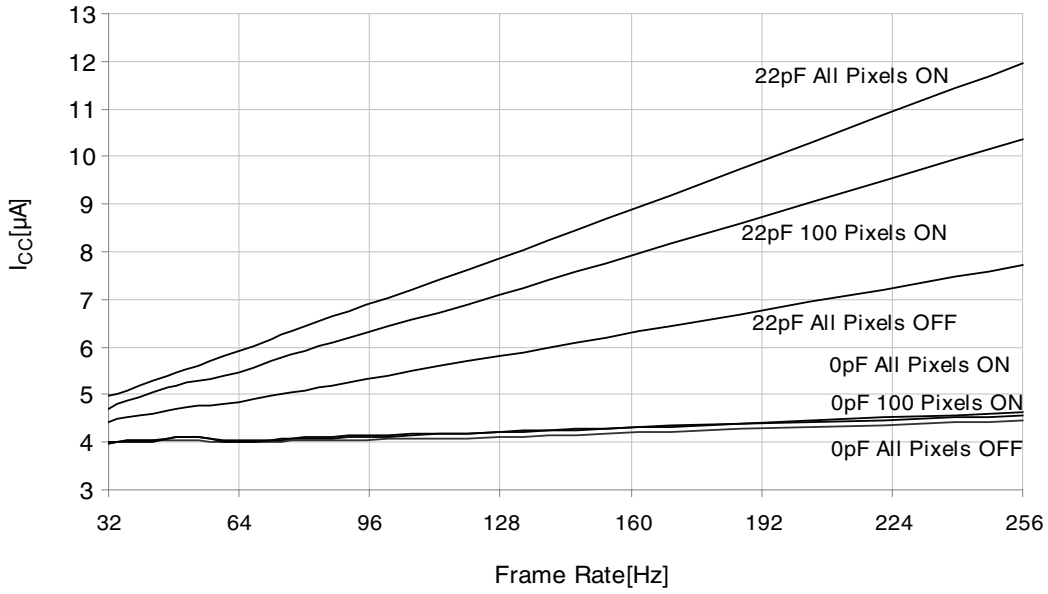


Figure 37-83. I_{CC} vs. Frame Rate
0pF load.

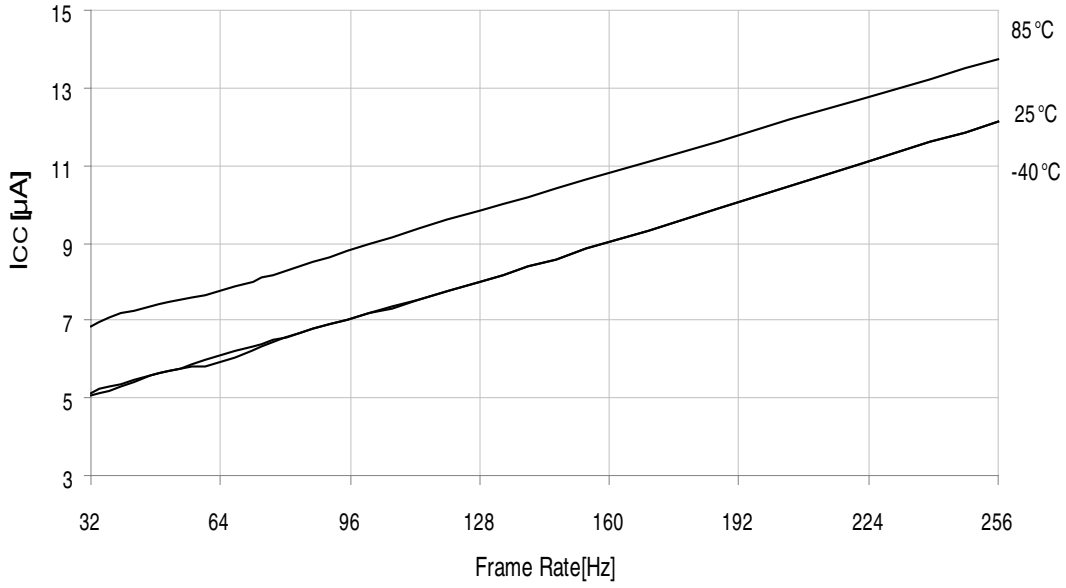


Figure 37-84. I_{CC} vs. Contrast
32Hz Low Power Frame Rate from 32.768kHz TOSC, w/o pixel load, V_{CC} = 1.8V.