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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128b1-aur

7. Memories

7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or bootloader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - Four bit-accessible general purpose registers for global variables or flags
  - Bus arbitration
    - Safe and deterministic handling of priority between CPU, DMA controller, and other bus masters
  - Separate buses for SRAM, EEPROM and I/O memory
    - Simultaneous bus access for CPU and DMA controller
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

7.2 Overview

The Atmel AVR architecture has two main memory spaces; the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in “Ordering Information” on page 2. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

10. System Clock and Clock Options

10.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz Ultra Low Power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1x to 31x multiplication
  - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

10.2 Overview

Atmel AVR XMEGA devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 10-1 on page 21 presents the principal clock system in the XMEGA B1 family of devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 23.

19. Hi-Res – High Resolution Extension

19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

Atmel AVR XMEGA B1 devices have one Hi-Res Extension that can be enabled for the timer/counters pair on PORTC. The notation of this is HIRESC.

21. USB – Universal Serial Bus Interface

21.1 Features

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface
- Integrated on-chip USB transceiver, no external components needed
- 16 endpoint addresses with full endpoint flexibility for up to 31 endpoints
  - One input endpoint per endpoint address
  - One output endpoint per endpoint address
- Endpoint address transfer type selectable to:
  - Control transfers
  - Interrupt transfers
  - Bulk transfers
  - Isochronous transfers
- Configurable data payload size per endpoint, up to 1023 bytes
- Endpoint configuration and data buffers located in internal SRAM
  - Configurable location for endpoint configuration data
  - Configurable location for each endpoint's data buffer
- Built-in direct memory access (DMA) to internal SRAM for:
  - Endpoint configurations
  - Reading and writing endpoint data
- Ping-pong operation for higher throughput and double buffered operation
  - Input and output endpoint data buffers used in a single direction
  - CPU/DMA controller can update data buffer during transfer
- Multi-packet transfer for reduced interrupt load and software intervention
  - Data payload exceeding maximum packet size is transferred in one continuous transfer
  - No interrupts or software interaction on packet transaction level
- Transaction complete FIFO for workflow management when using multiple endpoints
  - Tracks all completed transactions in a first-come, first-served work queue
- Clock selection independent of system clock source and selection
- Minimum 1.5MHz CPU clock required for low speed USB operation
- Minimum 12MHz CPU clock required for full speed operation
- Connection to event system
- On chip debug possibilities during USB transactions

21.2 Overview

The USB module is a USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface.

The USB supports 16 endpoint addresses. All endpoint addresses have one input and one output endpoint, for a total of 31 configurable endpoints and one control endpoint. Each endpoint address is fully configurable and can be configured for any of the four transfer types: control, interrupt, bulk, or isochronous. The data payload size is also selectable, and it supports data payloads up to 1023 bytes.

No dedicated memory is allocated for or included in the USB module. Internal SRAM is used to keep the configuration for each endpoint address and the data buffer for each endpoint. The memory locations used for endpoint configurations and data buffers are fully configurable. The amount of memory allocated is fully dynamic, according to the number of endpoints in use and the configuration of these. The USB module has built-in direct memory access (DMA), and will read/write data from/to the SRAM when a USB transaction takes place.

To maximize throughput, an endpoint address can be configured for ping-pong operation. When done, the input and output endpoints are both used in the same direction. The CPU or DMA controller can then read/write one data buffer while the USB module writes/reads the others, and vice versa. This gives double buffered communication.

26. AES and DES Crypto Engine

26.1 Features

- Data Encryption Standard (DES) CPU instruction
- Advanced Encryption Standard (AES) crypto module
- DES Instruction
  - Encryption and decryption
  - DES supported
  - Encryption/decryption in 16 CPU clock cycles per 8-byte block
- AES crypto module
  - Encryption and decryption
  - Supports 128-bit keys
  - Supports XOR data load mode to the state memory
  - Encryption/decryption in 375 clock cycles per 16-byte block

26.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for cryptography. These are supported through an AES peripheral module and a DES CPU instruction, and the communication interfaces and the CPU can use these for fast, encrypted communication and secure data storage.

DES is supported by an instruction in the AVR CPU. The 8-byte key and 8-byte data blocks must be loaded into the register file, and then the DES instruction must be executed 16 times to encrypt/decrypt the data block.

The AES crypto module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done. The encrypted/encrypted data can then be read out, and an optional interrupt can be generated. The AES crypto module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

28. LCD - Liquid Crystal Display Controller

28.1 Features

- Display capacity up to 40 segment and up to four common terminals
- Supports up to 16 GPIOs
- Shadow display memory gives full freedom in segment update
- ASCII character mapping
- Swap capability option on segment and/or common terminal buses
- Supports from static up to 1/4 duty
- Supports static and 1/3 bias
- LCD driver active in power save mode for low power operation
- Software selectable low power waveform
- Flexible selection of frame frequency
- Programmable blink mode and frequency on two segment terminals
- Uses Only 32kHz RTC clock source
- On-chip LCD power supply
- Software contrast adjustment control
- Equal source and sink capability to Increase glass life time
- Extended interrupt mode for display update or wake-up from sleep mode

28.2 Overview

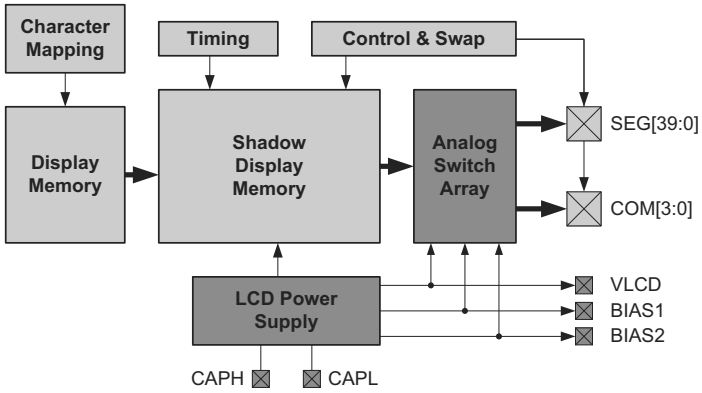
The LCD controller is intended for monochrome passive liquid crystal display (LCD) with up to four common terminals and up to 40 Segments terminals. If the application does not need all the LCD segments available on the XMEGA, up to 16 of the unused LCD pins can be used as general purpose I/O pins.

The LCD controller can be clocked by an internal or an external asynchronous 32kHz clock source. This 32kHz oscillator source selection is the same as for the real time counter (RTC).

Dedicated Low Power Waveform, Contrast Control, Extended Interrupt Mode, Selectable Frame Frequency and Blink functionality are supported to off-load the CPU, reduce interrupts and reduce power consumption.

To reduce hardware design complexity, the LCD includes integrated LCD buffers, an integrated power supply voltage and an innovative SWAP mode. Using SWAP mode, the hardware designers have more flexibility during board layout as they can rearrange the pin sequence on Segment and/or Common Terminal Buses.

Figure 28-1. LCD Overview



29. ADC – 12-bit Analog to Digital Converter

29.1 Features

- Two Analog to Digital Converters (ADCs)
- 12-bit resolution
- Up to three hundred thousand samples per second
  - Down to 2.3µs conversion time with 8-bit resolution
  - Down to 3.35µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 16 single-ended inputs
  - 16x4 differential inputs without gain
  - 16x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Three internal inputs
  - Internal temperature sensor
  - AV_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional DMA transfer of conversion results
- Optional interrupt/event on compare result

29.2 Overview

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to three hundred thousand samples per second (KSPS). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

The ADC measurements can either be started by application software or an incoming event from another peripheral in the device. The ADC measurements can be started with predictable timing, and without software intervention. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The output from the AV_{CC}/10 and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

32. Pinout and Pin Functions

The device pinout is shown in “Pinout/Block Diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

32.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

32.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground
AGND	Analog Ground

32.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

32.1.3 Analog Functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
AREF	Analog Reference input pin

32.1.4 LCD Functions

SEGn	LCD Segment Drive Output n
COMn	LCD Common Drive Output n
VLCD	LCD Voltage Multiplier Output
BIAS2	LCD Intermediate Voltage 2 Output (VLCD * 2/3)
BIAS1	LCD Intermediate Voltage 1 Output (VLCD * 1/3)
CAPH	LCD High End Of Flying Capacitor
CAPL	LCD Low End Of Flying Capacitor

32.1.5 Timer/Counter and AWEX Functions

OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

32.1.6 Communication Functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI
D-	Data- for USB
D+	Data+ for USB

32.1.7 Oscillators, Clock, and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel 0 Output
RTCOUT	RTC Clock Source Output

32.1.8 Debug/System Functions

RESET	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

Symbol	Parameter	Condition			Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance					5.9		pF
C_{XTAL2}	Parasitic capacitance					8.3		
C_{LOAD}	Parasitic capacitance load					3.5		

Note: 1. Numbers for negative impedance are not tested but guaranteed from design and characterization.

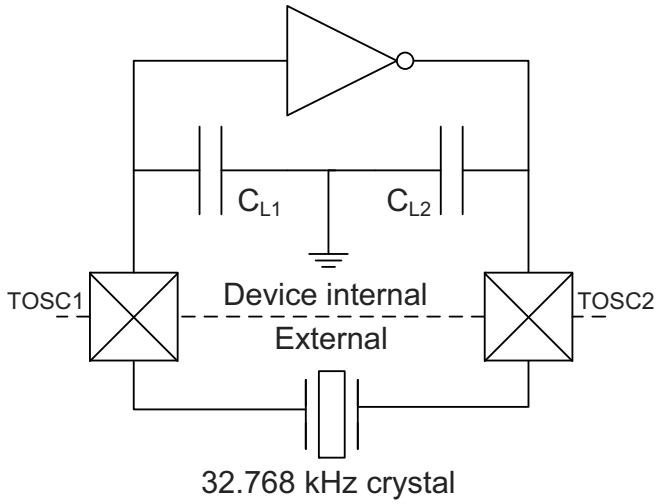
36.14.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 36-28. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12.0pF			28	
C_{IN_TOSC}	Input capacitance between TOSC pins	Normal mode		3.5		pF
		Low power mode		3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			
	Long term Jitter (SIT)			0		%

Note: 1. See Figure 36-4 for definition.

Figure 36-4. TOSC Input Capacitance



The input capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

37. Typical Characteristics

37.1 Current Consumption

37.1.1 Active Mode Supply Current

Figure 37-1. Active Supply Current vs. Frequency
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

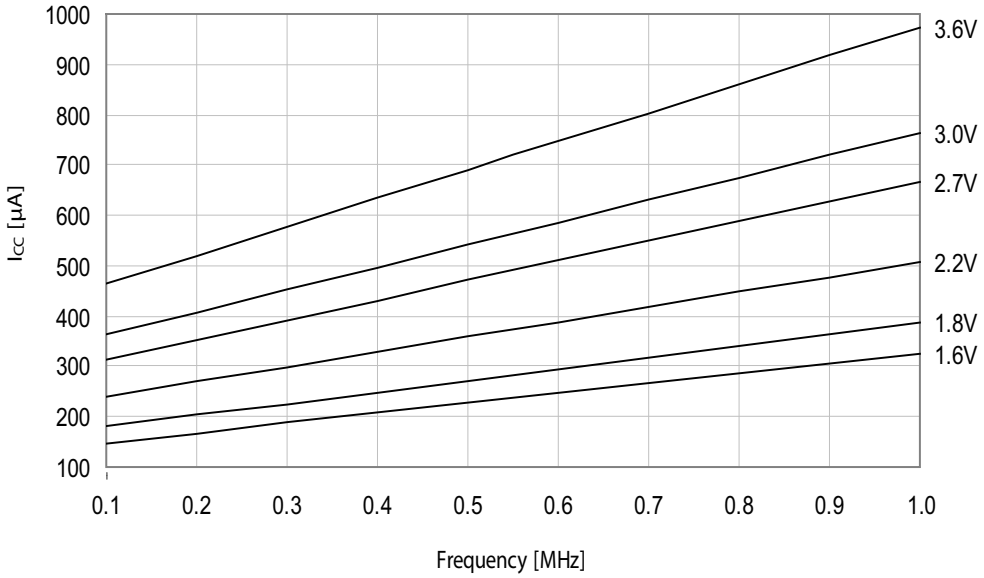


Figure 37-2. Active Supply Current vs. Frequency
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

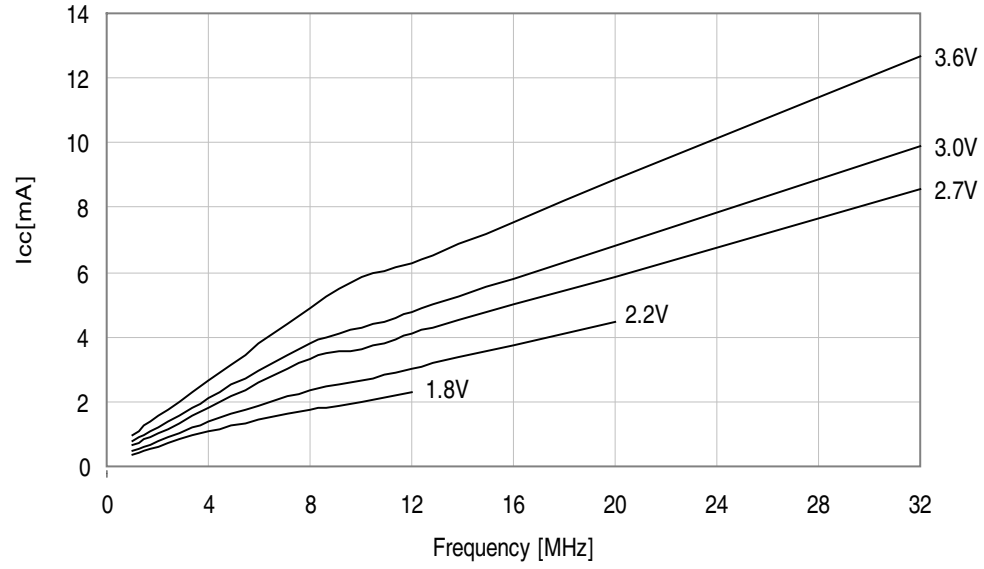


Figure 37-15. Power-down Mode Supply Current vs. V_{CC}

***All functions disabled*.**

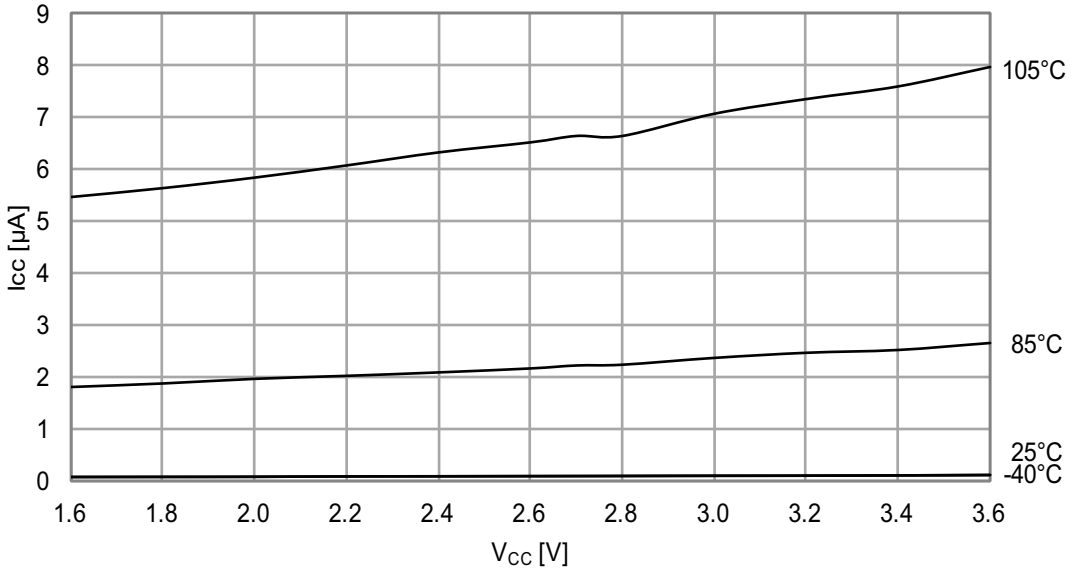


Figure 37-16. Power-down Mode Supply Current vs. V_{CC}

***Watchdog and sampled BOD enabled and running from internal ULP oscillator*.**

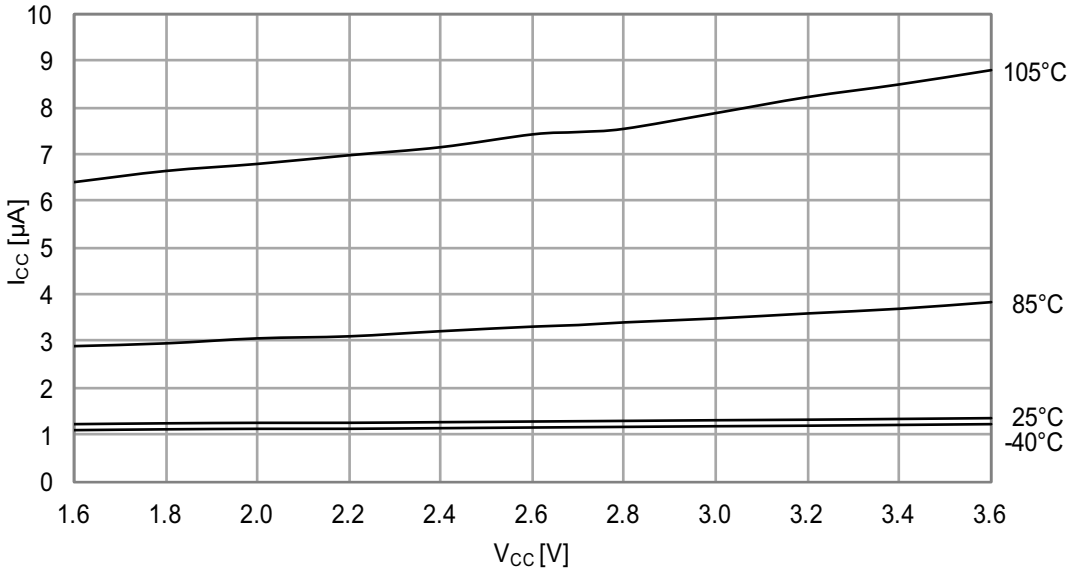


Figure 37-23. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 1.8V.

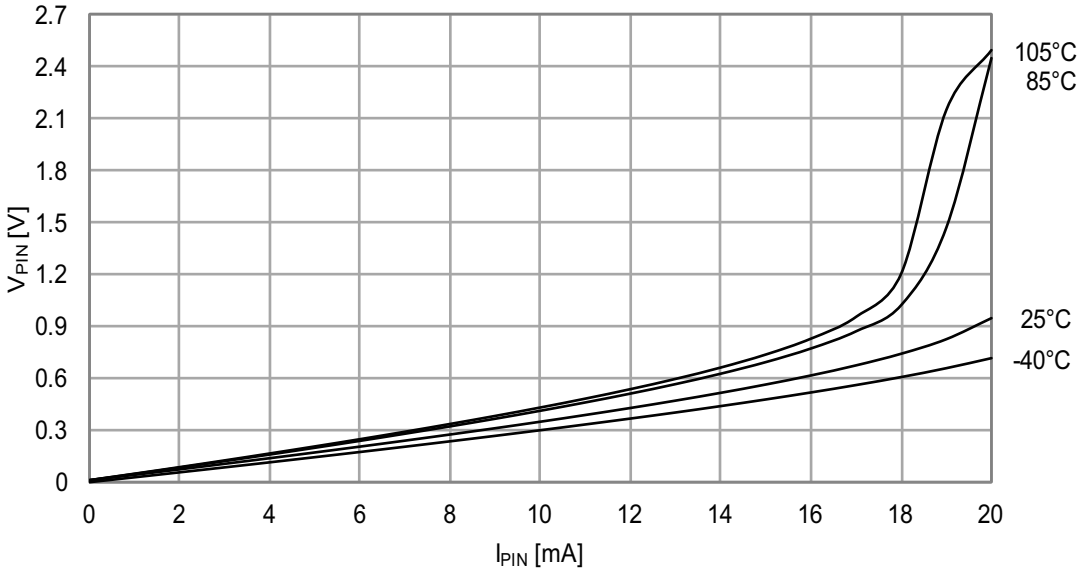


Figure 37-24. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 3.0V.

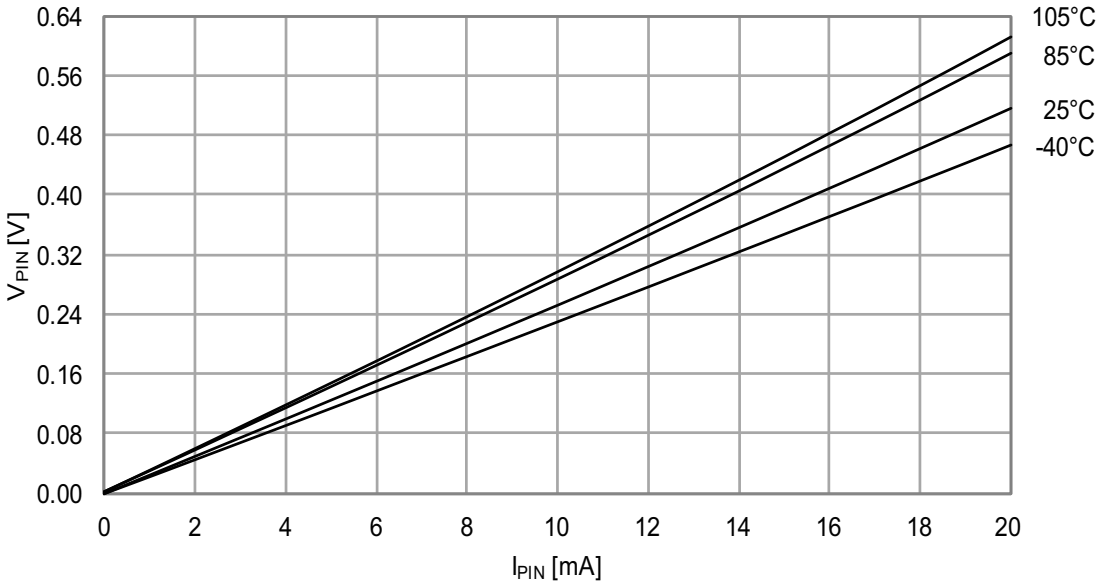


Figure 37-31. ADC DNL vs. V_{REF}

Differential signed mode, V_{CC} = 3.6V external reference.

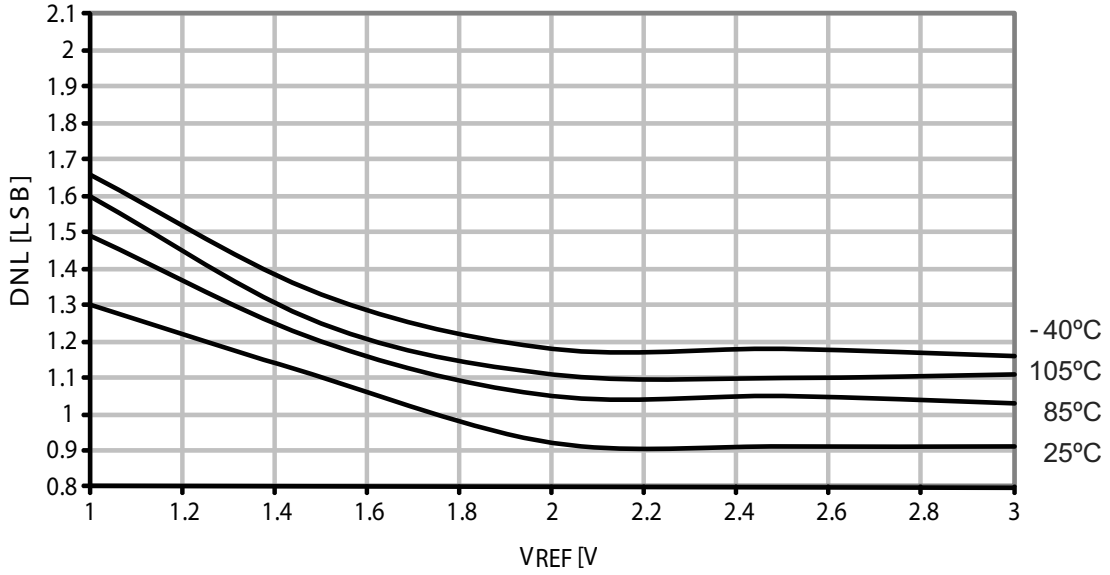


Figure 37-32. ADC DNL vs. V_{REF}

SE unsigned mode, V_{CC} = 3.6V, external reference.

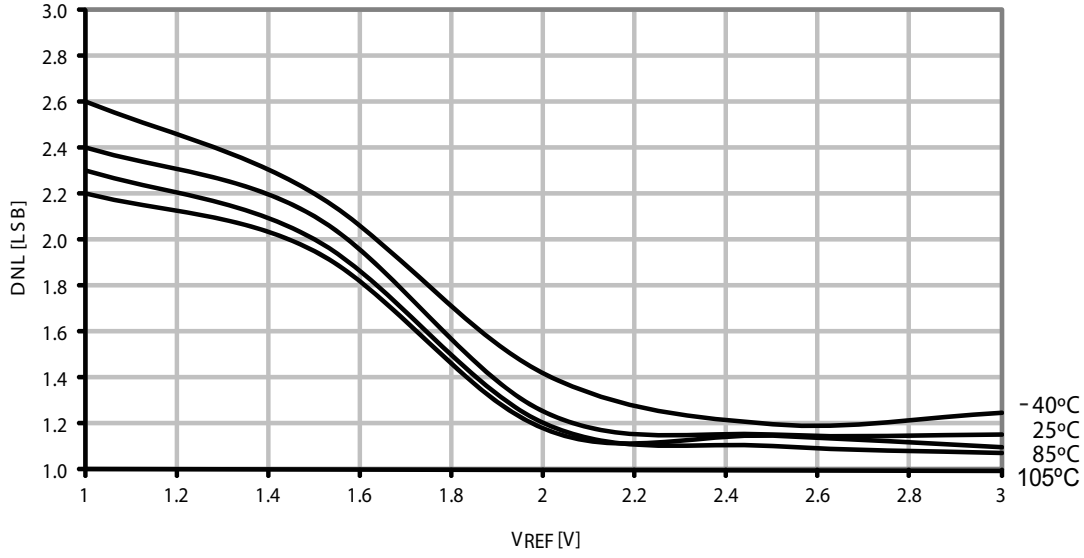


Figure 37-45. Analog Comparator Propagation Delay vs. V_{CC}

***High speed mode*.**

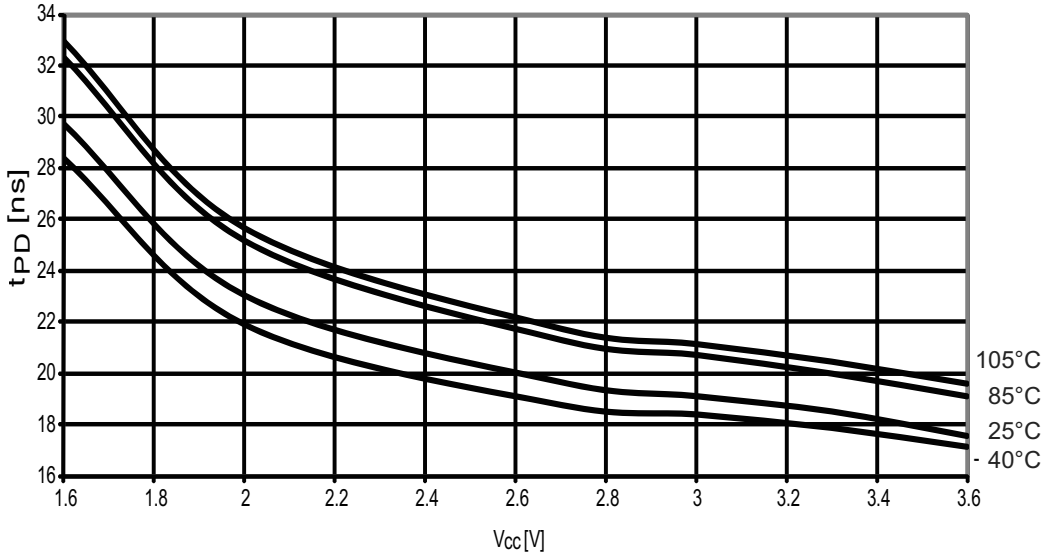


Figure 37-46. Analog Comparator Current Consumption vs. V_{CC}

High-speed mode.

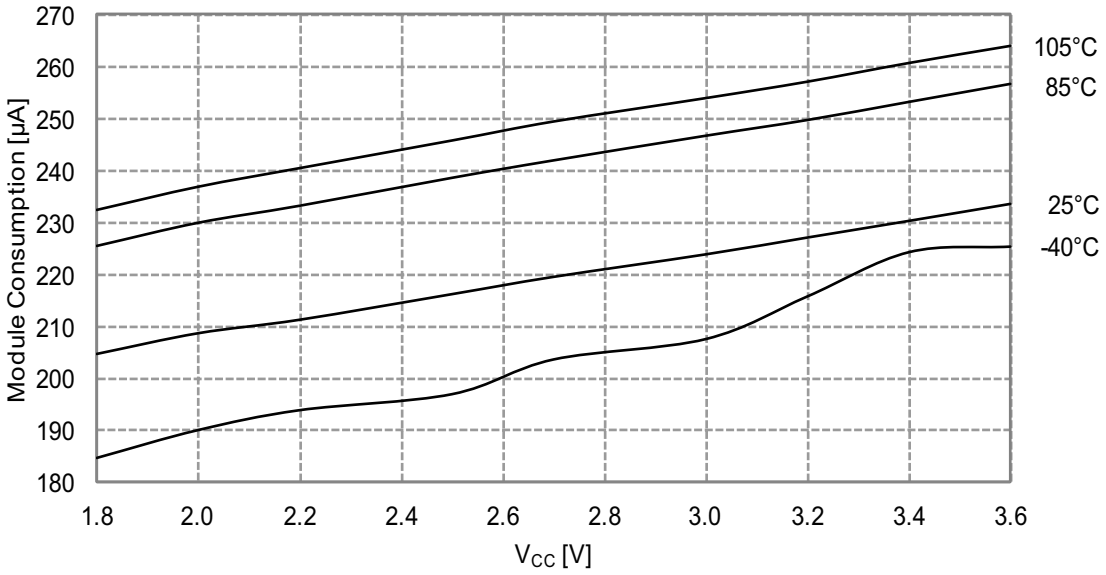


Figure 37-72. 32MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V.

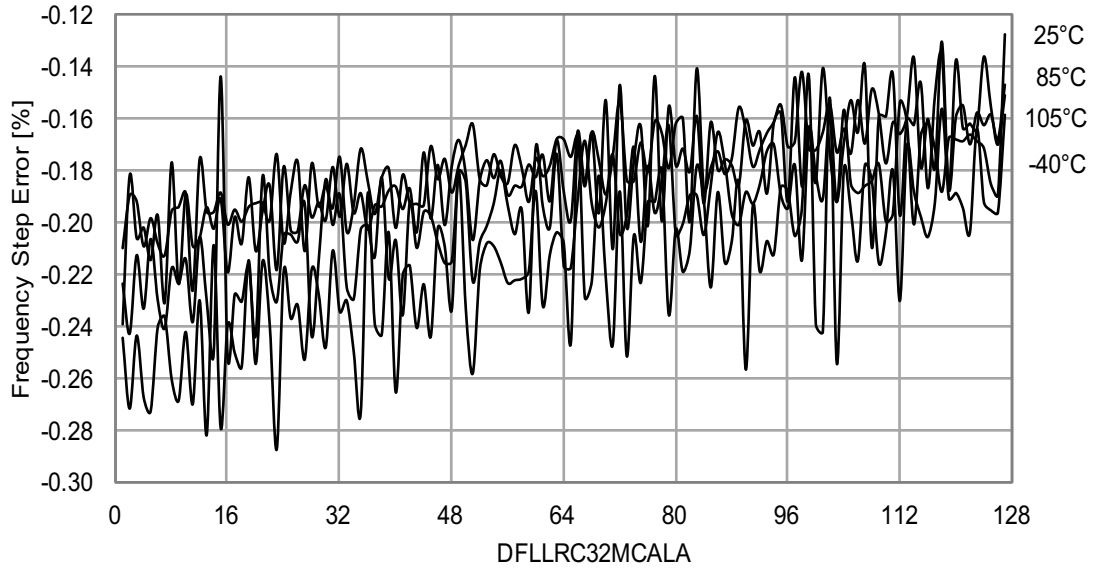
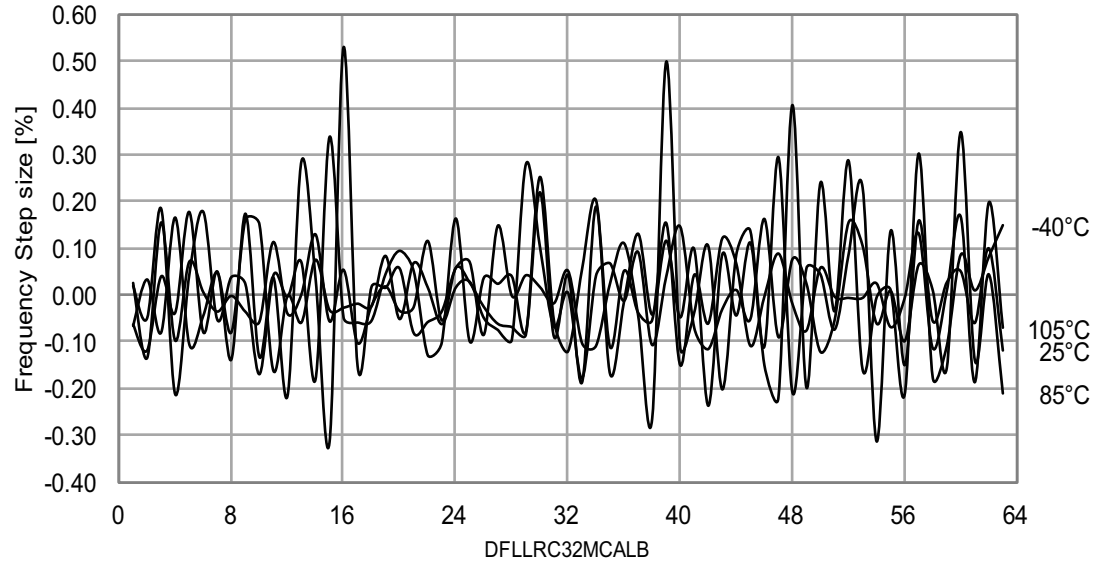


Figure 37-73. 32MHz Internal Oscillator CALB Calibration Step Size

V_{CC} = 3.0V, CALA = mid value.



37.8.5 32MHz Internal Oscillator Calibrated to 48MHz

Figure 37-76. 48MHz Internal Oscillator Frequency vs. Temperature
DFLL disabled.

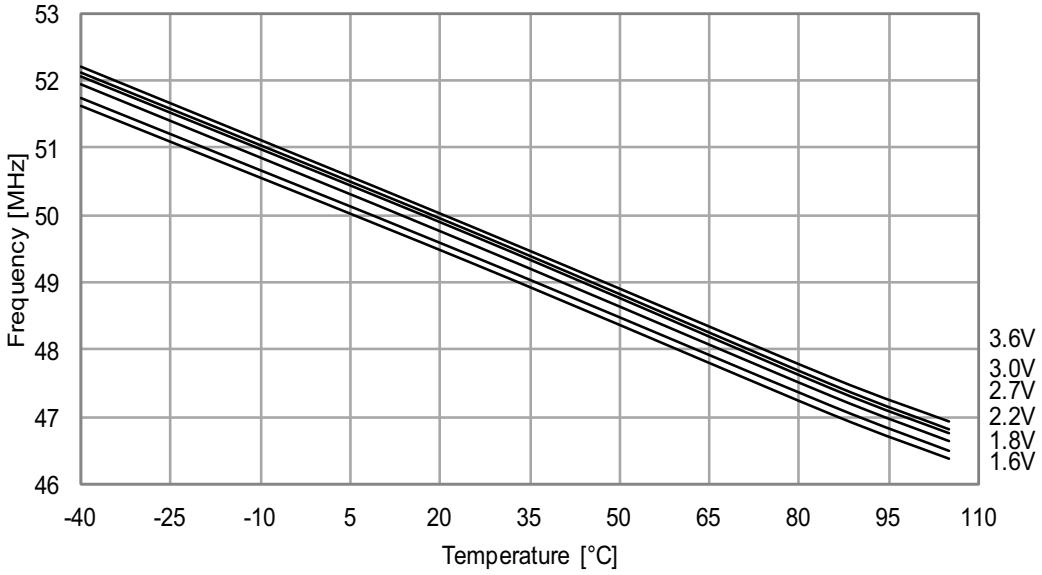


Figure 37-77. 48MHz Internal Oscillator Frequency vs. Temperature
***DFLL enabled, from the 32.768kHz internal oscillator*.**

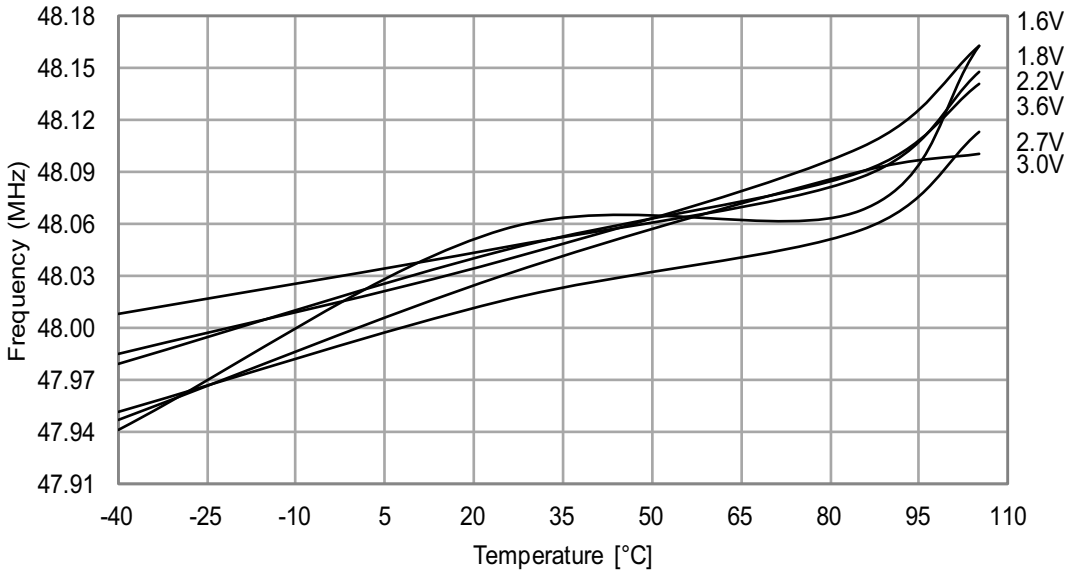


Figure 37-78. 32MHz Internal Oscillator CALA Calibration Step Size

Using 48MHz calibration value from signature row, V_{CC} = 3.0V.

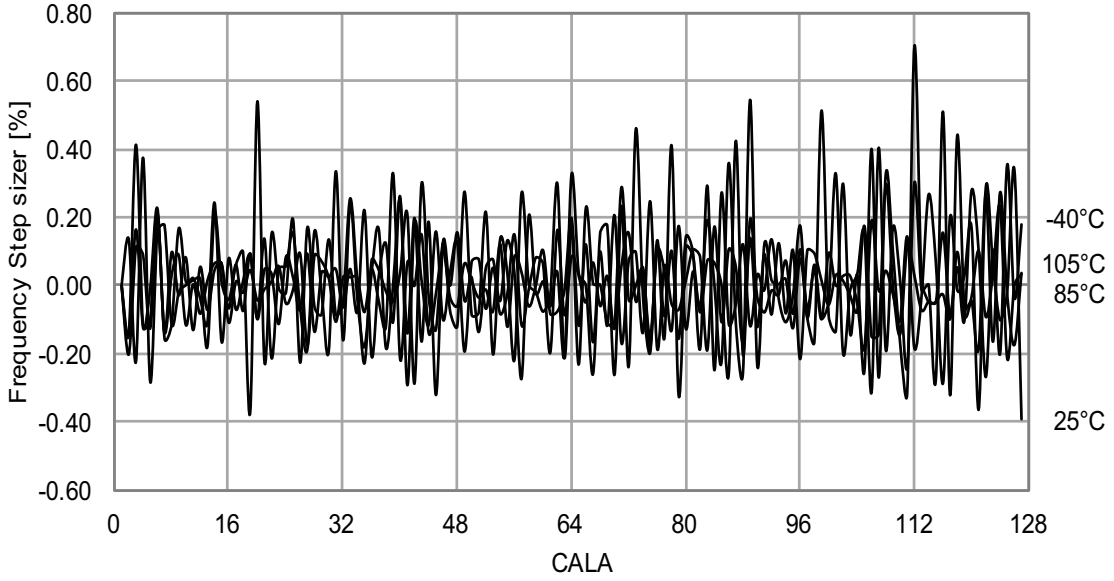
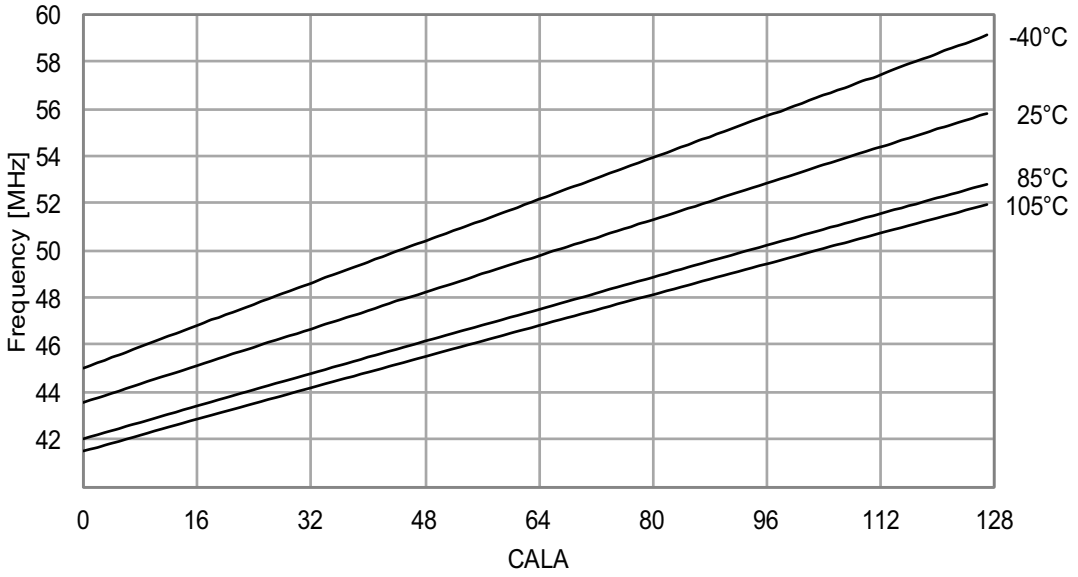


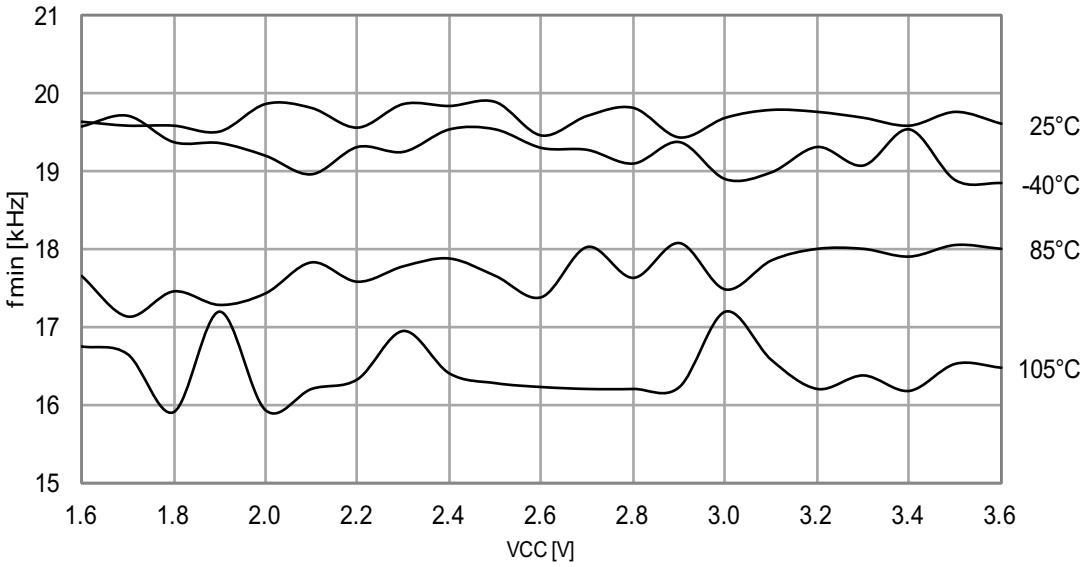
Figure 37-79. 48MHz Internal Oscillator Frequency vs. CALA Calibration Value

V_{CC} = 3.0V.



37.9 PDI Characteristics

Figure 37-80. Maximum PDI Frequency vs. V_{CC}



39. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

39.1 8330H – 12/2014

1.	Corrected description for VFBGA pinout in Table 2-1 on page 5.

39.2 8330G – 11/2014

1.	Information for 105°C are added.
2.	Several small changes are made to set up the document according to the new template.
3.	AVDD in Table 32-2 on page 56 has been corrected to AVCC.
4.	Changed Vcc to AVcc in Section 29. “ADC – 12-bit Analog to Digital Converter” on page 49 and Section 30. “AC – Analog Comparator” on page 51.
5.	Added error information on USART transmitter to Section 38. “Errata” on page 136.
6.	Changed pin names in Table 2-1 on page 5 from VCC1, LVCC1 and LVCC01 to VCC from GND1, LGND1 and LGND01 to GND from D2W_D to PDI_DATA
7.	Changed unit value for parameter $t_{SU;DAT}$ to ns in Table 36-30 on page 89.
8.	Corrected description for VFBGA pinout. Pin F2 changed from VCC to GND in Table 2-1 on page 5.

39.3 8330F – 02/2014

1.	Added the correct VFBGA package drawing: ● Replaced the package 100C1 (CBGA) by the package 7A1 (VFBGA) ● Updated the package type in “Ordering Information” on page 2 ● Updated the title in Figure 2-2 on page 5 and in the Table 2-1 on page 5 ● Updated the package type in “Typical Characteristics” on page 91
2.	Updated the title name of the Table 36-24 on page 82.

39.4 8330E – 06/2013

1.	Added pinout for CBGA package option: Figure 2-2 and Table 2-1 on page 5.