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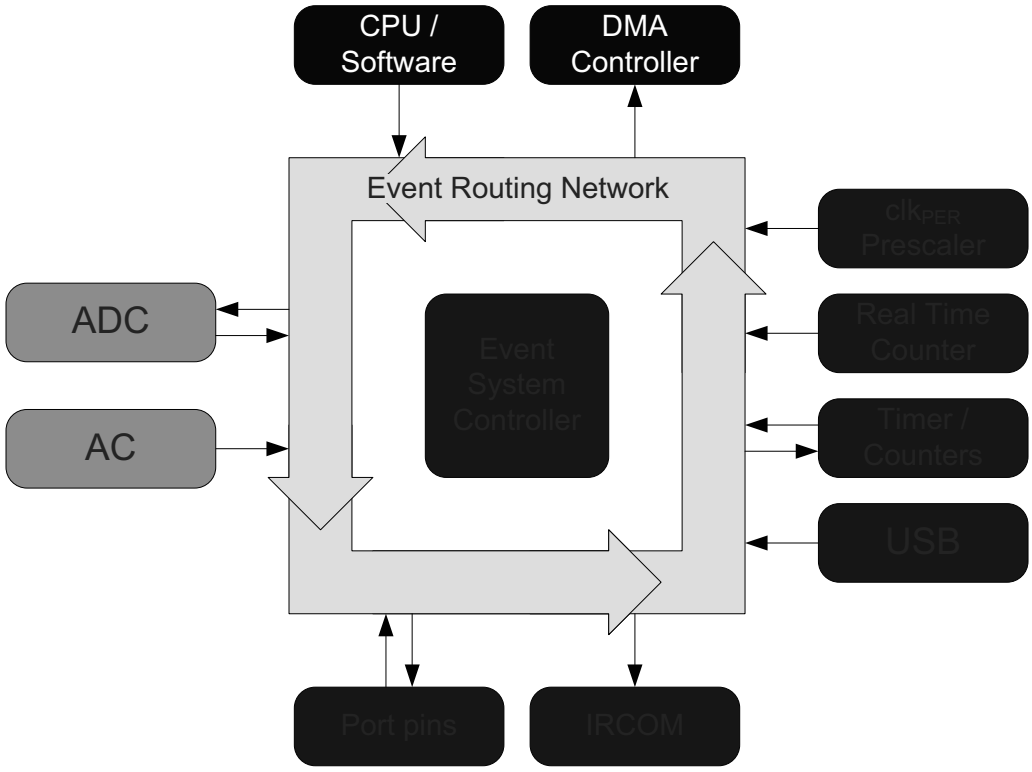
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-CBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128b1-cur

Figure 9-1. Event System Overview and Connected Peripherals



The event routing network consists of four software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to four parallel event configurations and routings. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

14. Interrupts and Programmable Multilevel Interrupt Controller

14.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium, and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

14.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

14.3 Interrupt Vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA B1 devices are shown in Table 14-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA B manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1. The program address is the word address.

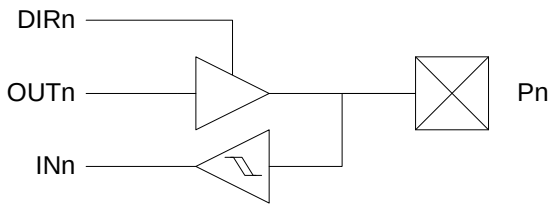
Table 14-1. Reset and Interrupt Vectors

Program address (Base address)	Source	Interrupt description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base
0x008	PORTR_INT_base	Port R Interrupt base
0x00C	DMA_INT_base	DMA Controller Interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base

Program address (Base address)	Source	Interrupt description
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x03E	USB_INT_base	USB on port D Interrupt base
0x046	LCD_INT_base	LCD Interrupt base
0x048	AES_INT_vect	AES Interrupt vector
0x04A	NVM_INT_base	Non-Volatile Memory Interrupt base
0x04E	PORTB_INT_base	Port B Interrupt base
0x052	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x058	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x060	PORTD_INT_base	Port D Interrupt base
0x064	PORTG_INT_base	Port G Interrupt base
0x068	PORTM_INT_base	Port M Interrupt base
0x06C	PORTE_INT_base	Port E Interrupt base
0x074	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x08A	USARTE0_INT_base	USART 0 on port E Interrupt base
0x096	PORTA_INT_base	Port A Interrupt base
0x09A	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x0A0	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base

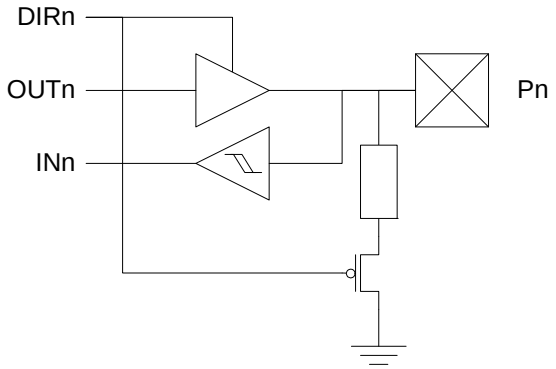
15.3.1 Push-pull

Figure 15-1. I/O Configuration - Totem-pole



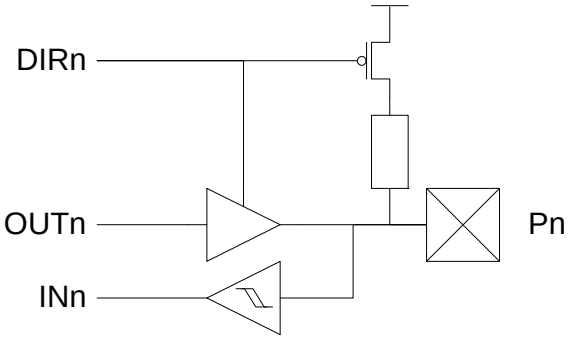
15.3.2 Pull-down

Figure 15-2. I/O Configuration - Totem-pole with Pull-down (on Input)



15.3.3 Pull-up

Figure 15-3. I/O Configuration - Totem-pole with Pull-up (on Input)



15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

31. Programming and Debugging

31.1 Features

- Programming
  - External programming through PDI or JTAG interfaces
    - Minimal protocol overhead for fast operation
    - Built-in error detection and handling for reliable operation
  - Boot loader support for programming through any communication interface
- Debugging
  - Non-intrusive, real-time, on-chip debug system
  - No software or hardware resources required from device except pin connection
  - Program flow control
    - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
  - Unlimited number of user program breakpoints
  - Unlimited number of user data breakpoints, break on:
    - Data location read, write, or both read and write
    - Data location content equal or not equal to a value
    - Data location content is greater or smaller than a value
    - Data location content is within or outside a range
  - No limitation on device clock frequency
- Program and Debug Interface (PDI)
  - Two-pin interface for external programming and debugging
  - Uses the Reset pin and a dedicated pin
  - No I/O pins required during programming or debugging
- JTAG interface
  - Four-pin, IEEE Std. 1149.1 compliant interface for programming and debugging
  - Boundary scan capabilities according to IEEE Std. 1149.1 (JTAG)

31.2 Overview

The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device.

The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPOM, fuses, lock bits, and the user signature row.

Debug is supported through an on-chip debug system that offers non-intrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassembler level.

Programming and debugging can be done through two physical interfaces. The primary one is the PDI physical layer, which is available on all devices. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). A JTAG interface is also available on most devices, and this can be used for programming and debugging through the four-pin JTAG interface. The JTAG interface is IEEE Std. 1149.1 compliant, and supports boundary scan. Any external programmer or on-chip debugger/emulator can be directly connected to either of these interfaces. Unless otherwise stated, all references to the PDI assume access through the PDI physical layer.

32. Pinout and Pin Functions

The device pinout is shown in “Pinout/Block Diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

32.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

32.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground
AGND	Analog Ground

32.1.2 Port Interrupt Functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

32.1.3 Analog Functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
AREF	Analog Reference input pin

32.1.4 LCD Functions

SEGn	LCD Segment Drive Output n
COMn	LCD Common Drive Output n
VLCD	LCD Voltage Multiplier Output
BIAS2	LCD Intermediate Voltage 2 Output (VLCD * 2/3)
BIAS1	LCD Intermediate Voltage 1 Output (VLCD * 1/3)
CAPH	LCD High End Of Flying Capacitor
CAPL	LCD Low End Of Flying Capacitor

34. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One’s Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two’s Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 ← Encrypt(R15:R0, K) else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K)		1/2
Branch instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3

36.6 Liquid Crystal Display Characteristics

Table 36-8. Liquid Crystal Display Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
SEG	Segment terminal pins		0		40	
COM	Common terminal pins		0		4	
f_{Frame}	LCD frame frequency	F(clk_{LCD})=32.768kHz	31.25		512	Hz
C_{Flying}	Flying capacitor			100		nF
Contrast	Contrast adjustment		-0.5	0	0.5	V
V_{LCD}	LCD regulated voltages	C_{Flying} = 0.1µF 0.1µF on V_{LCD}, BIAS2 and BIAS1 pins		3		V
BIAS2				2*V_{LCD}/3		
BIAS1				V_{LCD}/3		
R_{COM}	Common output impedance	COM0 to COM3(1)	0.25	0.5	1	kΩ
R_{SEG}	Segment output impedance	SEG0 to SEG39(1)	2	4	8	

Notes: 1. Applies to Static and 1/3 bias.

36.7 ADC Characteristics

Table 36-9. Power Supply, Reference, and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched			4.5	kΩ
C_{in}	Input capacitance	Switched			5	pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
Vin	Input range		0		V_{REF}	V
Vin	Conversion range	Differential mode, Vinp - Vinn	- 0.95*V_{REF}		0.95*V_{REF}	
Vin	Conversion range	Single ended unsigned mode, Vinp	- 0.05*V_{REF}		0.95*V_{REF}	

Table 36-10. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		1800	kHz
		Measuring internal signals		125		
f_{ClkADC}	Sample rate		16		300	ksps

36.8 Analog Comparator Characteristics

Table 36-13. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			10		mV
I_{lk}	Input leakage current			<10	50	nA
	Input voltage range		0.1		AV_{CC}- 0.1	V
	AC startup time			50		µs
V_{hys1}	Hysteresis, none	V_{CC} = 1.6V - 3.6V		0		mV
V_{hys2}	Hysteresis, small	V_{CC} = 1.6V - 3.6V		12		
V_{hys3}	Hysteresis, large	V_{CC} = 1.6V - 3.6V		28		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C		22	30	ns
		V_{CC} = 1.6V - 3.6V		21	40	
	64-Level Voltage Scaler Integral non-linearity (INL)			0.3	0.5	LSB
	Current source accuracy after calibration			5		%
	Current source calibration range	Single mode	4		6	µA
	Current source calibration range	Double mode	8		12	

36.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-14. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference for ADC	T= 85°C, after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Calibrated at T= 85°C		2.25		%

36.15 SPI Characteristics

Figure 36-5. SPI Timing Requirements in Master Mode

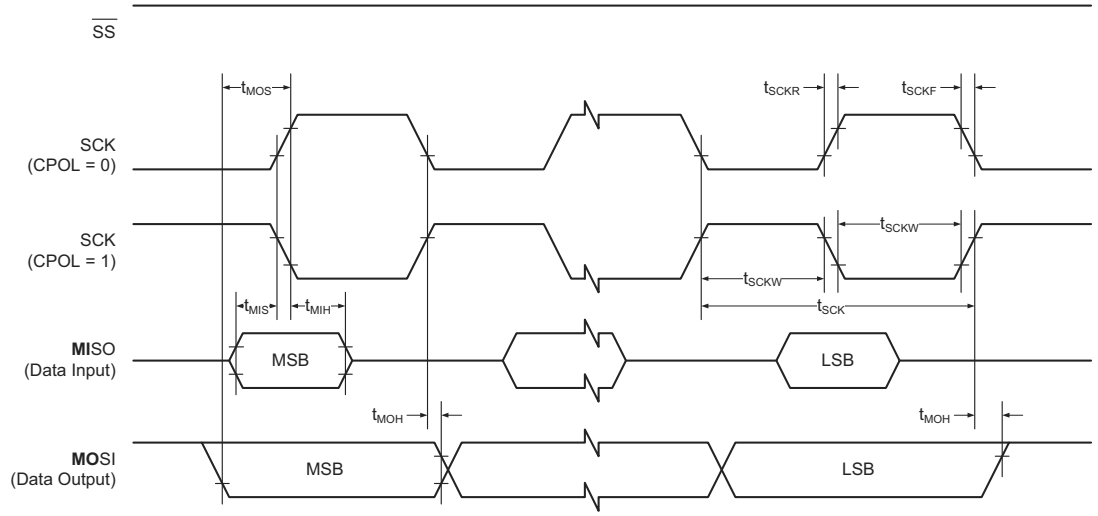


Figure 36-6. SPI Timing Requirements in Slave Mode

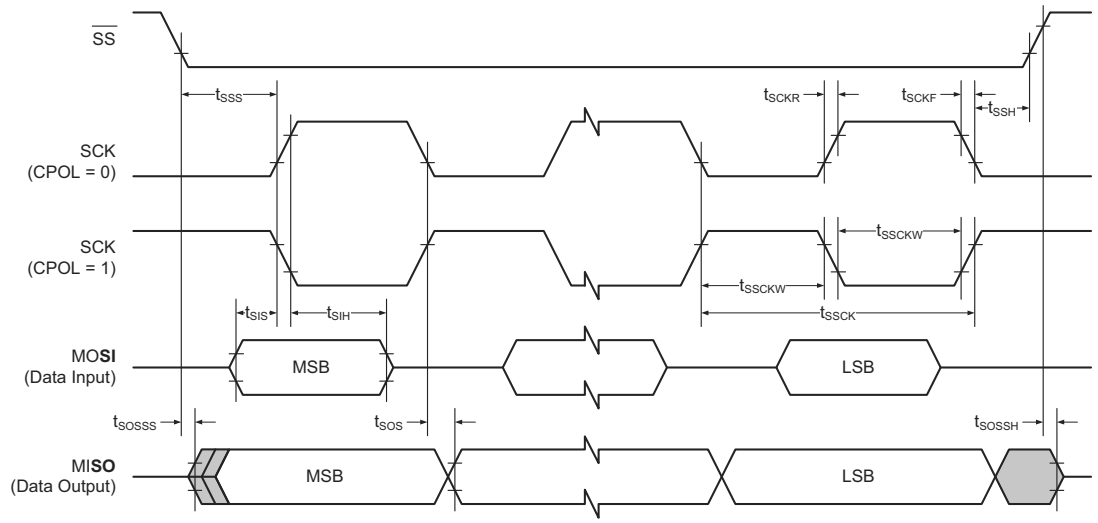


Table 36-29. SPI Timing Characteristics and Requirements

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 21-4 in XMEGA B Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		11		
t_{MIH}	MISO hold after SCK	Master		0		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

36.16 Two-wire Interface Characteristics

Table 36-30 describes the requirements for devices connected to the Two-wire Serial Bus. The Atmel AVR XMEGA Two-wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-7.

Figure 36-7. Two-wire Interface Bus Timing

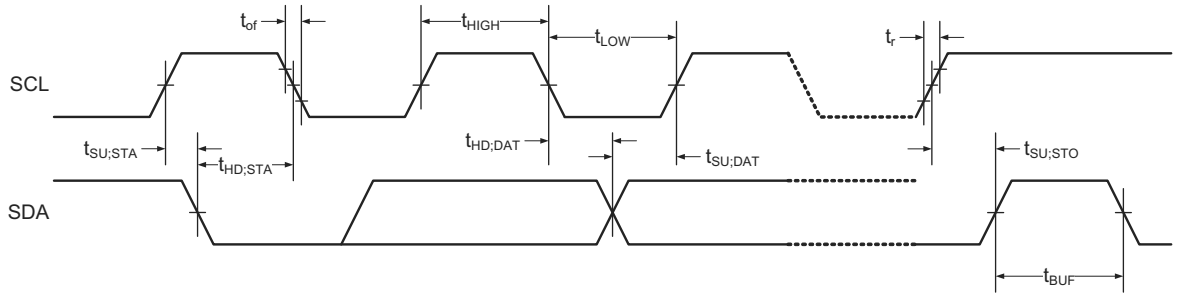


Table 36-30. Two-wire Serial Bus Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		0.7*V_{CC}		V_{CC}+0.5	V
V_{IL}	Input low voltage		-0.5		0.3*V_{CC}	
V_{hys}	Hysteresis of Schmitt trigger inputs		0.05V_{CC}[1]		0	
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		20+0.1C_b[1][2]		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	10pF < C_b < 400pF[2]	20+0.1C_b[1][2]		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	0.1V_{CC} < V_I < 0.9V_{CC}	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER}[3]>max(10f_{SCL}, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq$ 100kHz	$\frac{V_{CC}-0.4V}{3mA}$	$\frac{100ns}{C_b}$	$\frac{300ns}{C_b}$	Ω
		f_{SCL} > 100kHz				
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq$ 100kHz	4.0			µs
		f_{SCL} > 100kHz	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq$ 100kHz	4.0			
		f_{SCL} > 100kHz	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq$ 100kHz	4.7			
		f_{SCL} > 100kHz	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq$ 100kHz	0		3.5	
		f_{SCL} > 100kHz	0		0.9	

37.2 I/O Pin Characteristics

37.2.1 Pull-up

Figure 37-17. I/O Pin Pull-up Resistor Current vs. Input Voltage
V_{CC} = 1.8V.

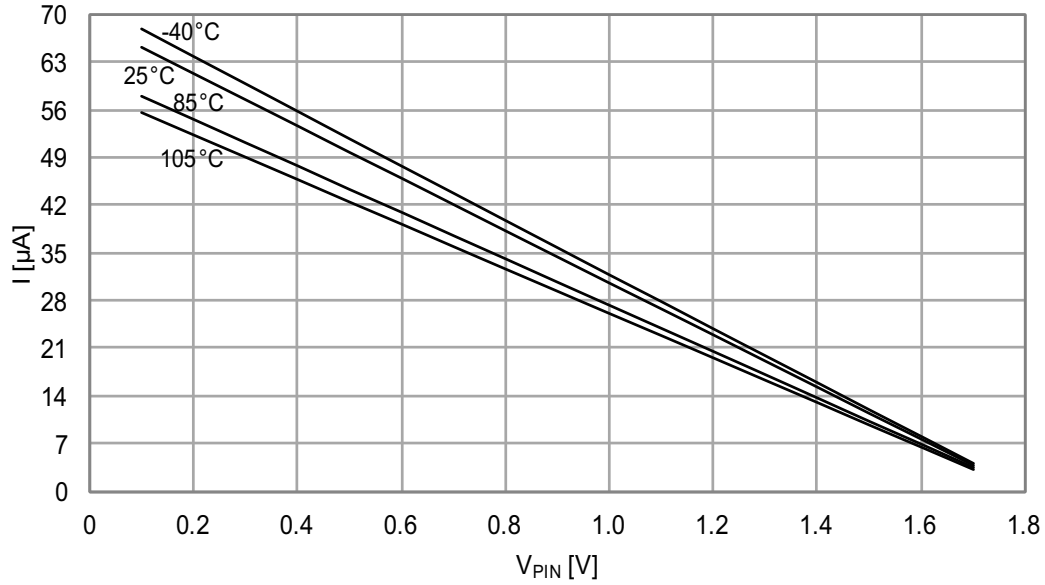


Figure 37-18. I/O Pin Pull-up Resistor Current vs. Input Voltage
V_{CC} = 3.0V.

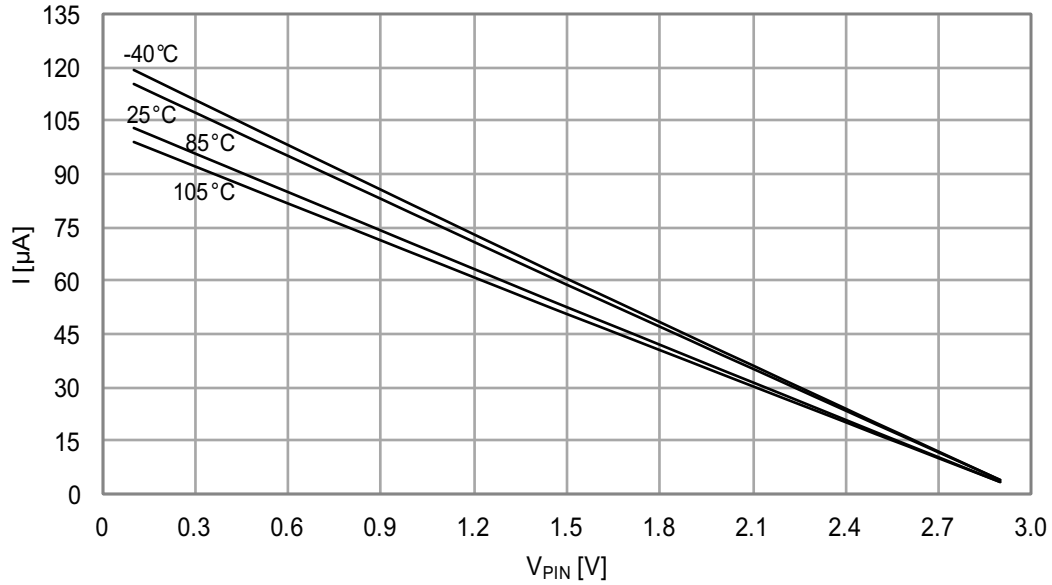


Figure 37-39. ADC Gain Error vs. V_{CC}.

Differential signed mode, external reference.

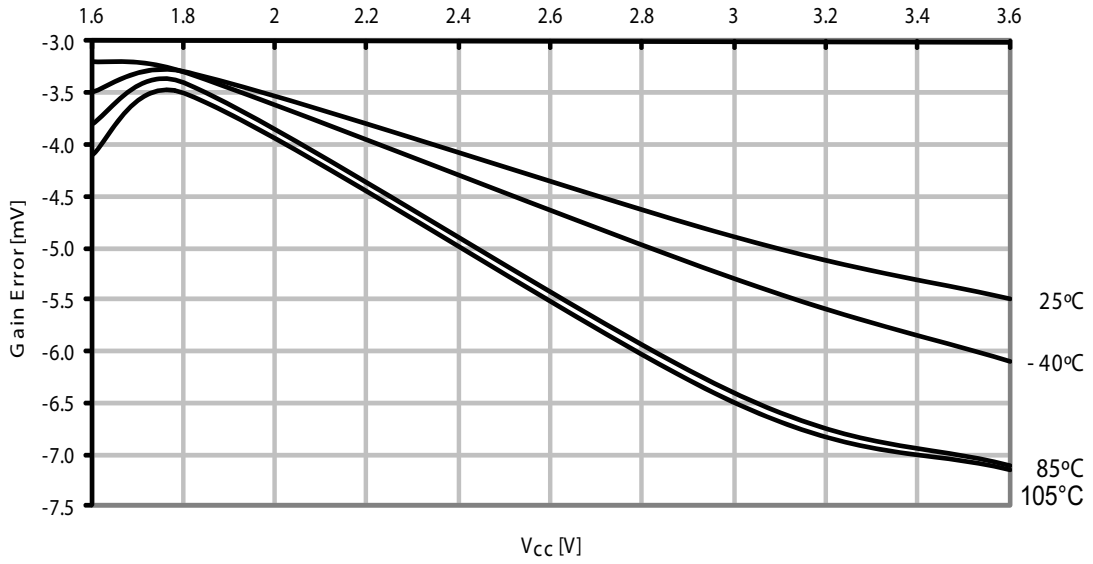


Figure 37-40. ADC Gain Error vs. V_{CC}.

SE Unsigned mode, external reference.

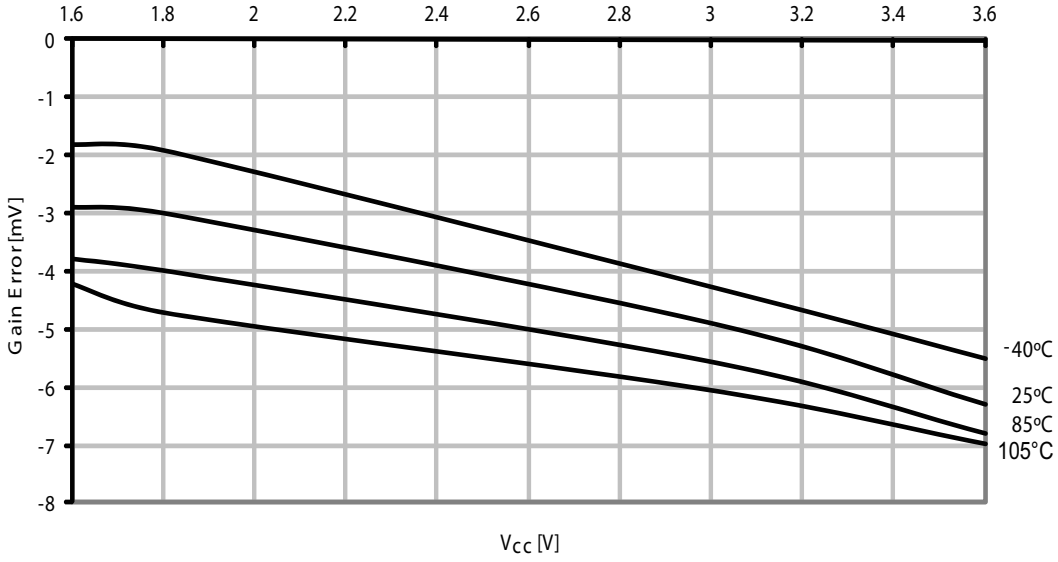
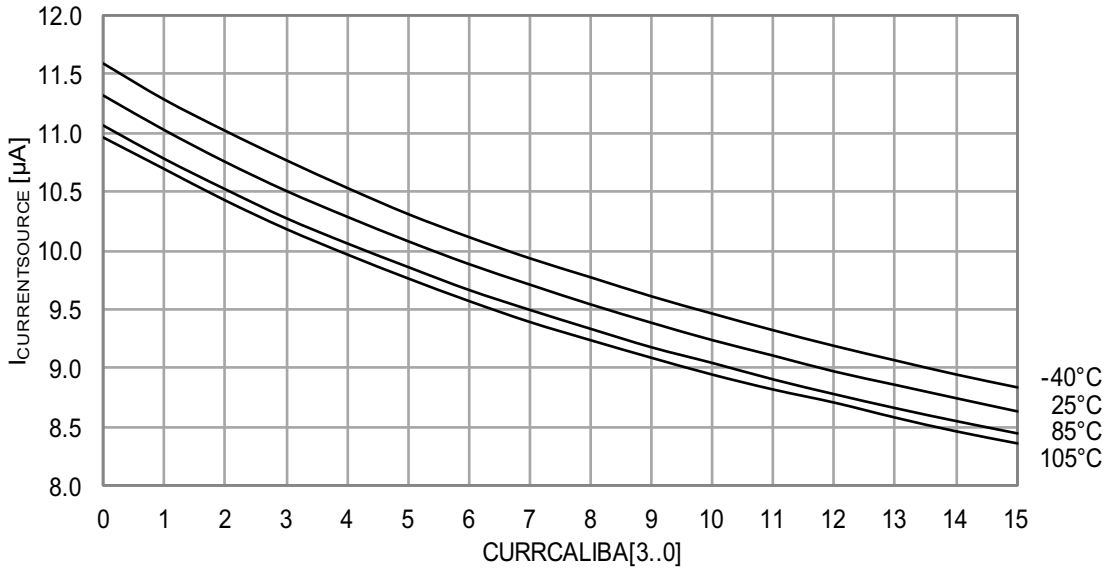


Figure 37-49. Analog Comparator Current Source vs. Calibration

***V_{CC} = 3.0V, double mode*.**



37.5 Internal 1.0V Reference Characteristics

Figure 37-50. ADC/DAC Internal 1.0V Reference vs. Temperature

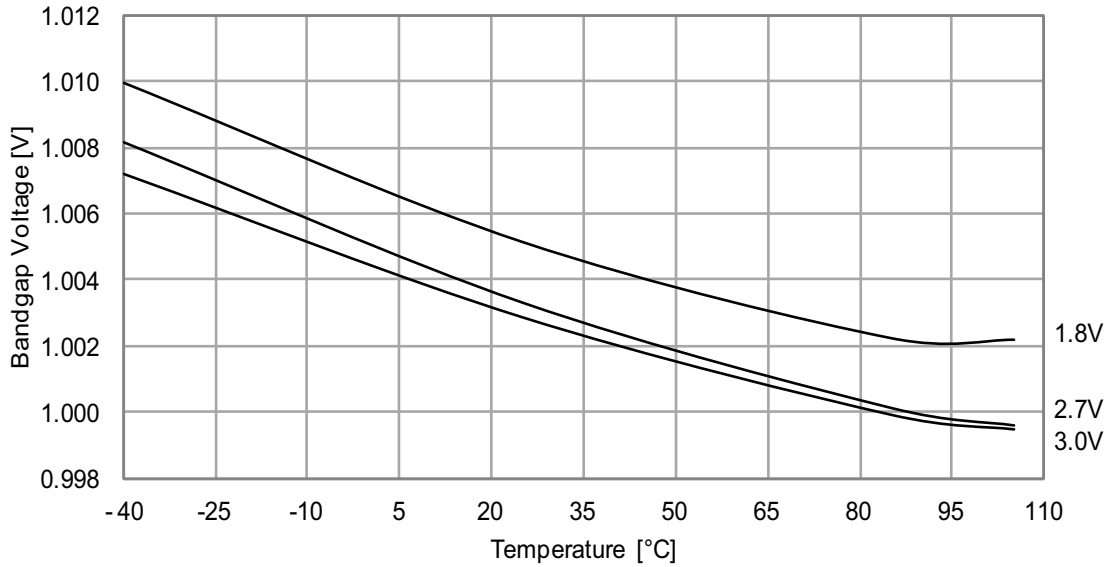
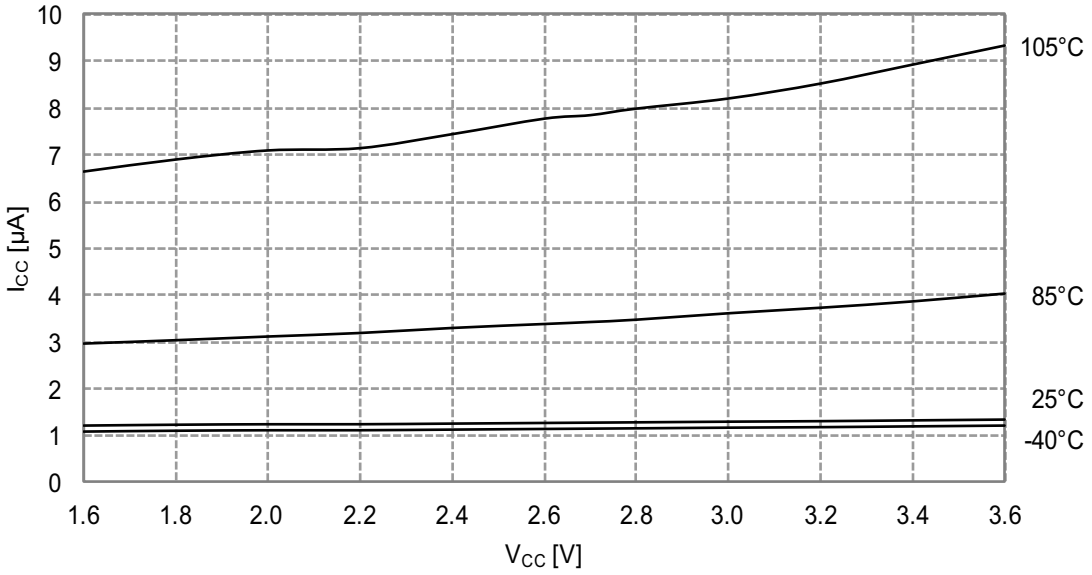


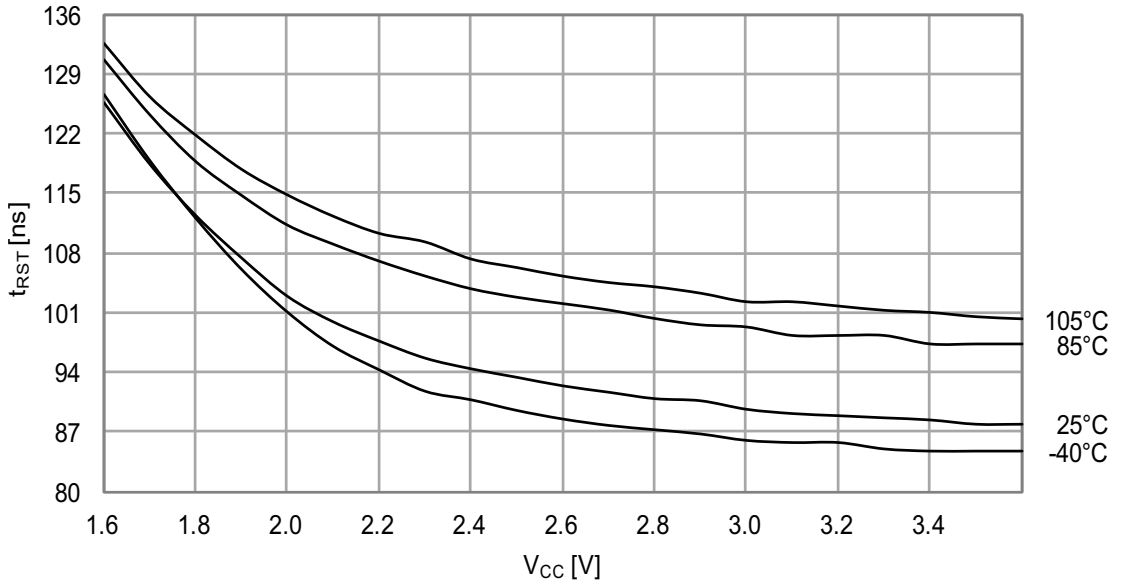
Figure 37-55. BOD Current Consumption vs. V_{CC}

***Sampled mode, BOD level = 1.6V*.**



37.7 External Reset Characteristics

Figure 37-56. Minimum Reset Pin Pulse Width vs. V_{CC}



37.10 LCD Characteristics

Figure 37-81. I_{CC} vs. Frame Rate

32Hz Low Power Frame Rate from 32.768kHz TOSC, w/ and w/o pixel load, V_{CC} = 1.8V, T = 25°C.

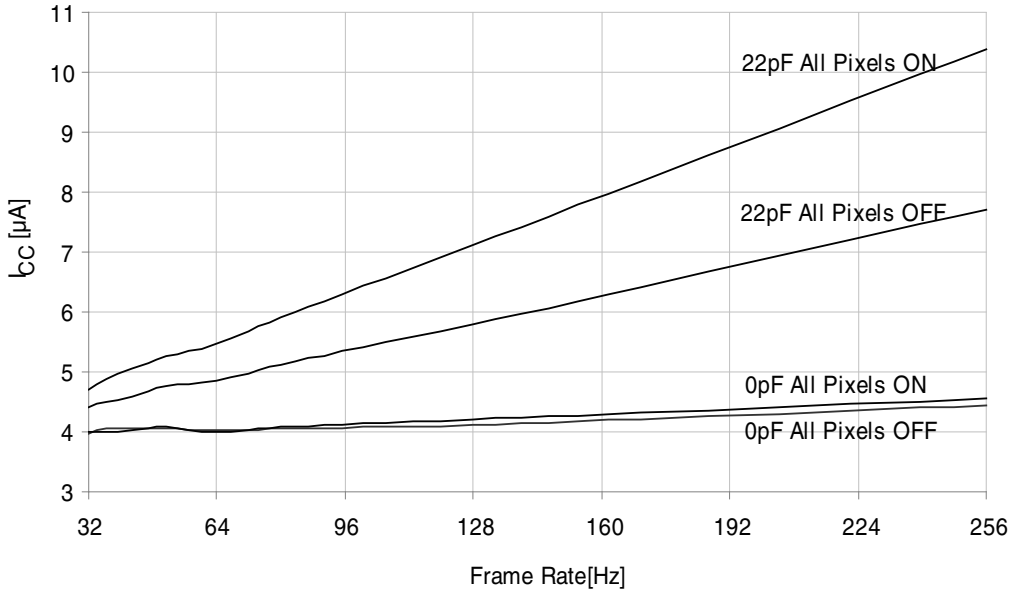


Figure 37-82. I_{CC} vs. Frame Rate

32Hz Low Power Frame Rate from 32.768kHz TOSC, w/ and w/o pixel load, V_{CC} = 3.0V, T = 25°C.

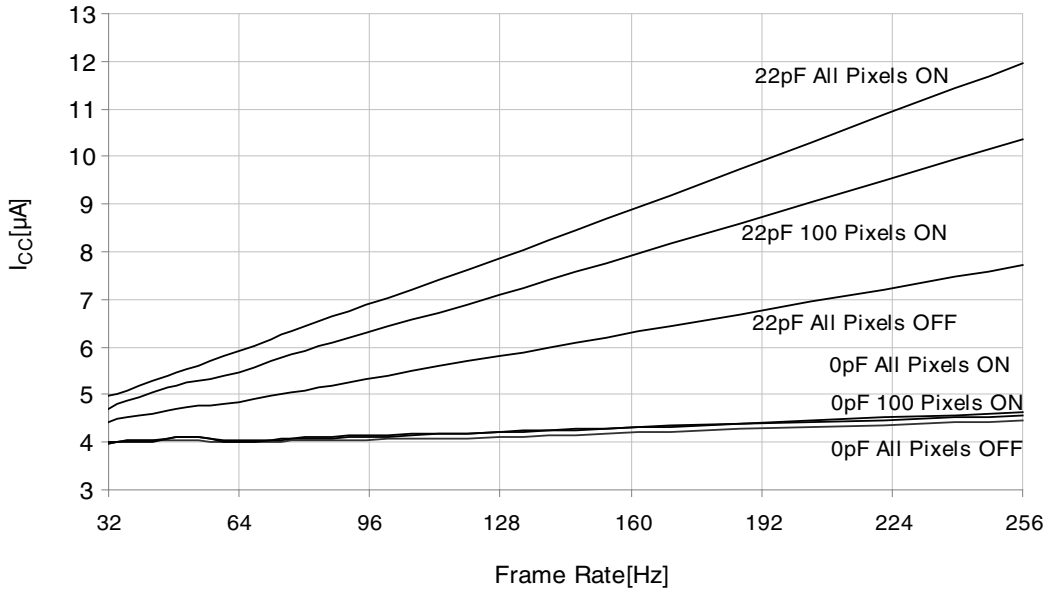


Figure 37-83. I_{CC} vs. Frame Rate
0pF load.

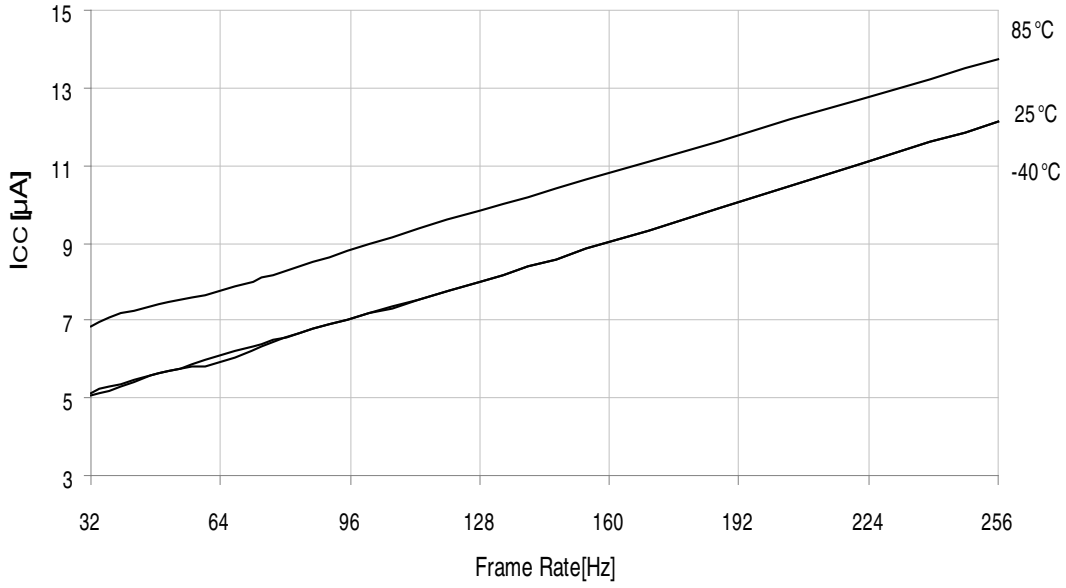


Figure 37-84. I_{CC} vs. Contrast
32Hz Low Power Frame Rate from 32.768kHz TOSC, w/o pixel load, V_{CC} = 1.8V.