Microchip Technology - ATXMEGA64B1-AU Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

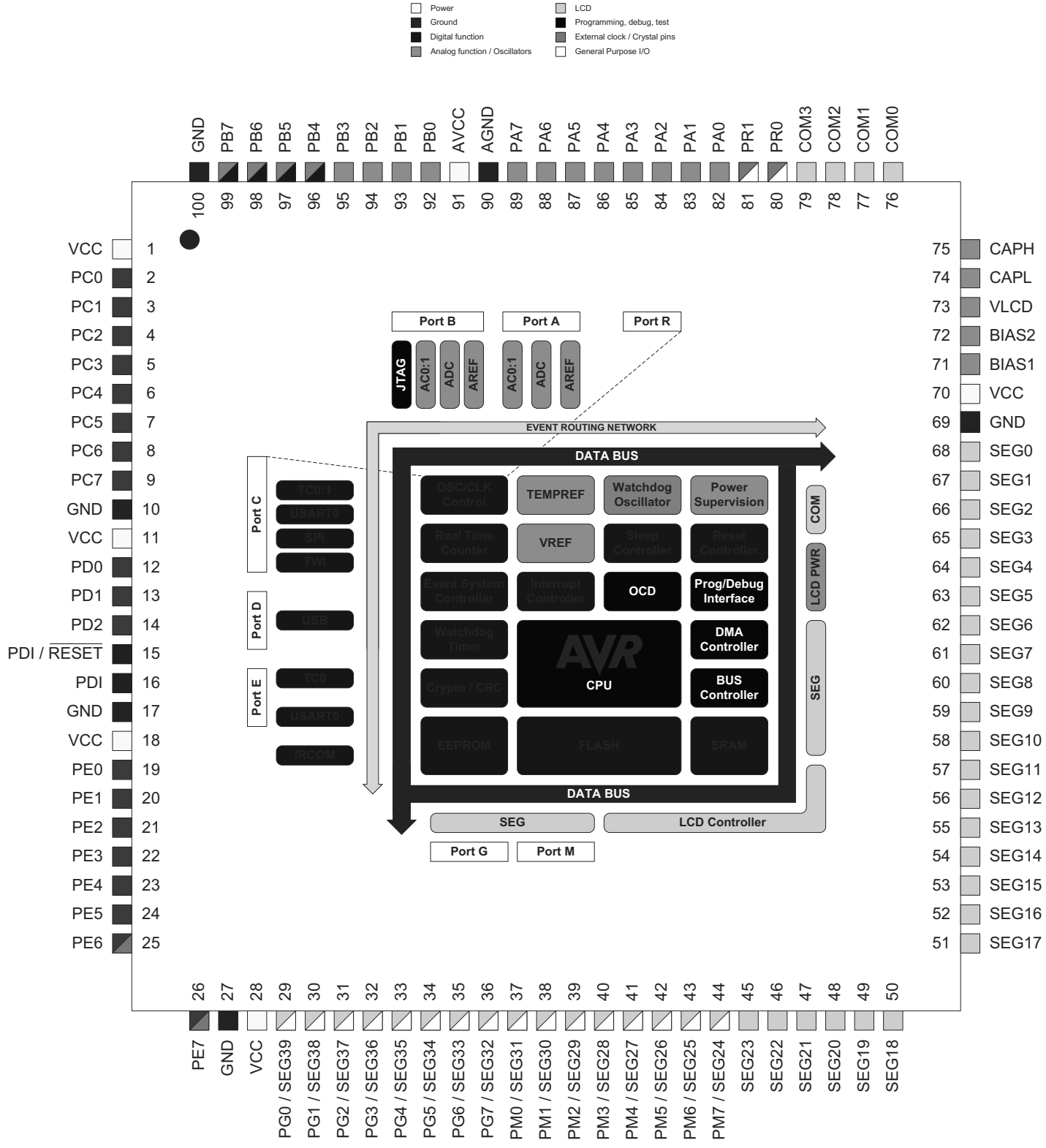
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64b1-au

2. Pinout/Block Diagram

Figure 2-1. Block Diagram and Pinout



Note: 1. For full details on pinout and alternate pin functions refer to “Pinout and Pin Functions” on page 54.

Figure 2-2. VFBGA Pinout

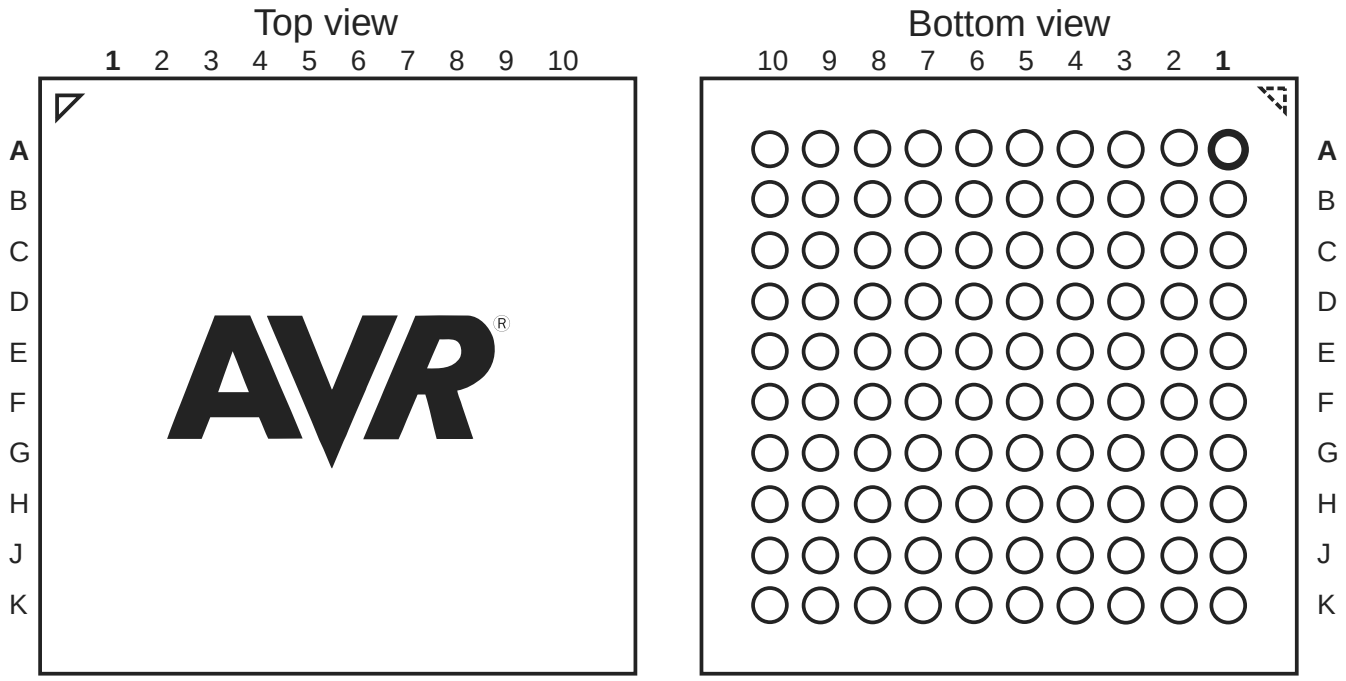


Table 2-1. VFBGA Pinout

	1	2	3	4	5	6	7	8	9	10
A	PC0	VCC	PB6	PB2	AVCC	PA5	PA1	PR1	COM2	CAPH
B	PC3	GND	PB7	PB4	AGND	PA4	PA0	PR0	COM1	CAPL
C	PC5	PC4	PC1	PB5	PA7	PA3	COM3	COM0	BIAS2	BIAS1
D	VCC	GND	PD0	PC2	PB0	PA6	SEG0	VLCD	GND	VCC
E	PD2	PDI/ RESET	PD1	PC6	PB1	PA2	SEG1	SEG4	SEG3	SEG2
F	VCC	GND	PDI	PC7	PB3	PM2/ SEG29	SEG10	SEG7	SEG6	SEG5
G	PE2	PE1	PE3	PE0	PE4	SEG23	SEG15	SEG13	SEG9	SEG8
H	PE5	PE6	PG1/ SEG38	PG4/ SEG35	PG7/ SEG32	PM5/ SEG26	SEG21	SEG18	SEG12	SEG11
J	PE7	PG0/ SEG39	PG3/ SEG36	PG6/ SEG33	PM1/ SEG30	PM4/ SEG27	PM7/ SEG24	SEG20	SEG16	SEG14
K	GND	VCC	PG2/ SEG37	PG5/ SEG34	PM0/ SEG31	PM3/ SEG28	PM6/ SEG25	SEG22	SEG19	SEG17

The Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers and SRAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for save storing of nonvolatile data in the program memory.

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic are supported, and the instruction set allows for efficient implementation of 32-bit arithmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

6.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

11.3.3 Power-save Mode

Power-save mode is identical to power down, with two exceptions:

1. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.
2. If the liquid crystal display controller (LCD) is enabled, it will keep running during sleep, and the device can wake up from LCD frame completed interrupt.

11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, RTC, and LCD clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

12.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

12.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

12.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see “WDT – Watchdog Timer” on page 27.

12.4.5 Software Reset

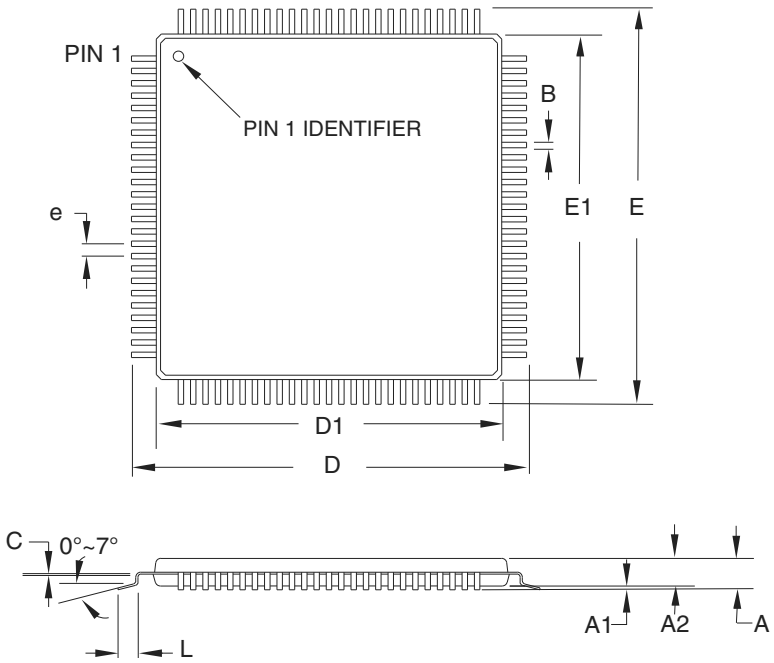
The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register.The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

12.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

35. Packaging Information

35.1 100A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08mm maximum.

2014-02-05

	TITLE	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**100A**, 100-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	E

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Power-save power consumption(2)	RTC on ULP clock, WDT, sampled BOD and LCD enabled, and all pixels ON, T = 25°C	V_{CC} = 1.8V		4.6		µA
			V_{CC} = 3.0V		5.2		
		RTC on 1.024kHz low power 32.768kHz TOSC, LCD enabled and all pixels ON T = 25°C	V_{CC} = 1.8V		3.9		
			V_{CC} = 3.0V		4.3		
		RTC from low power 32.768kHz TOSC, LCD enabled and all pixels ON, T = 25°C	V_{CC} = 1.8V		4.0		
			V_{CC} = 3.0V		4.5		
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		420		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization and not tested in production.

Figure 37-3. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator.

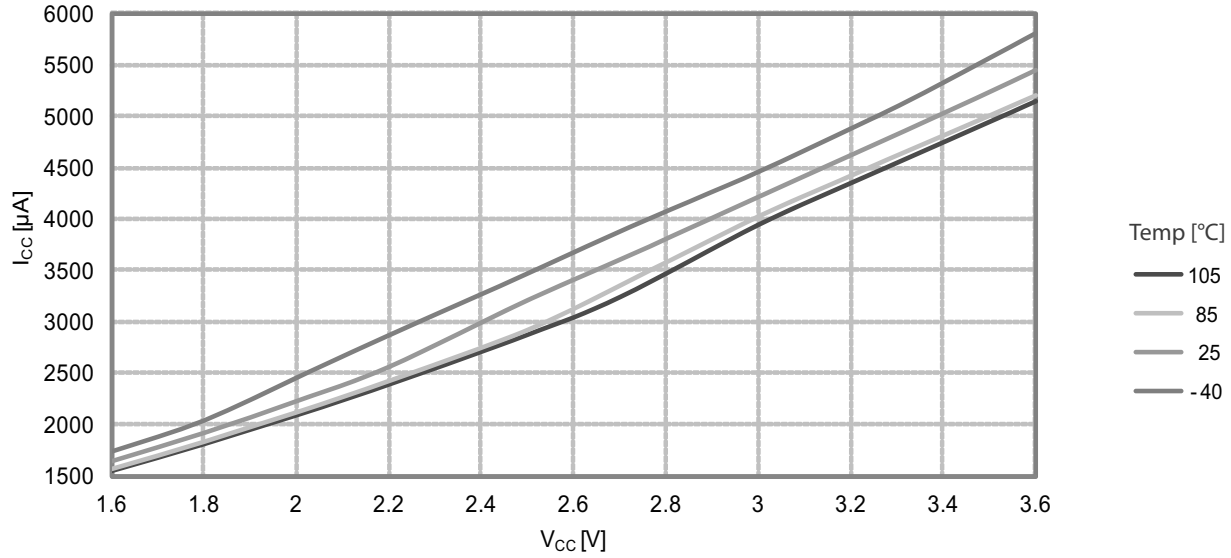


Figure 37-4. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator.

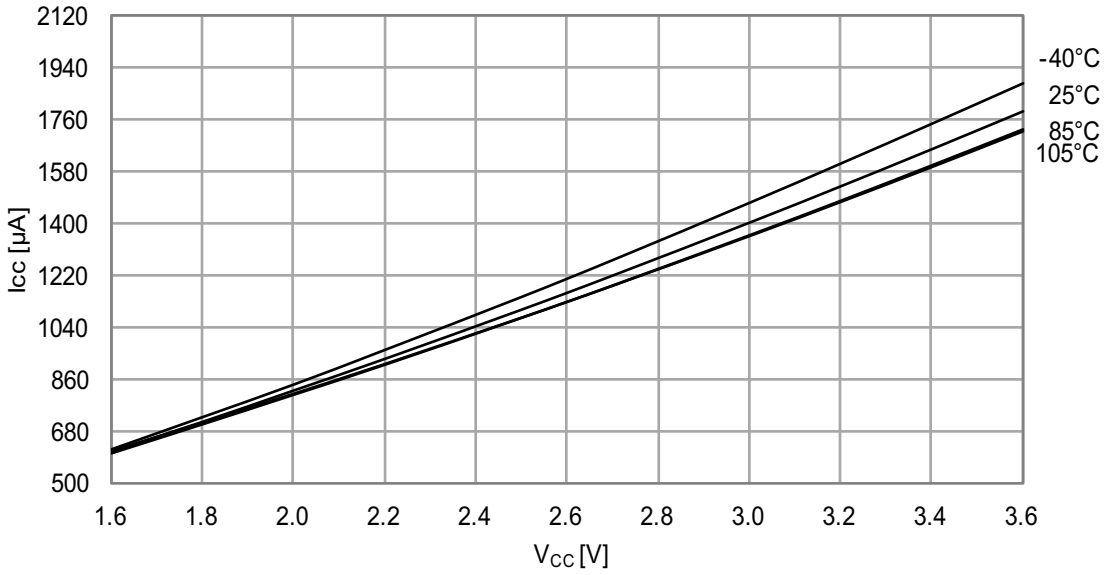


Figure 37-5. Active Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

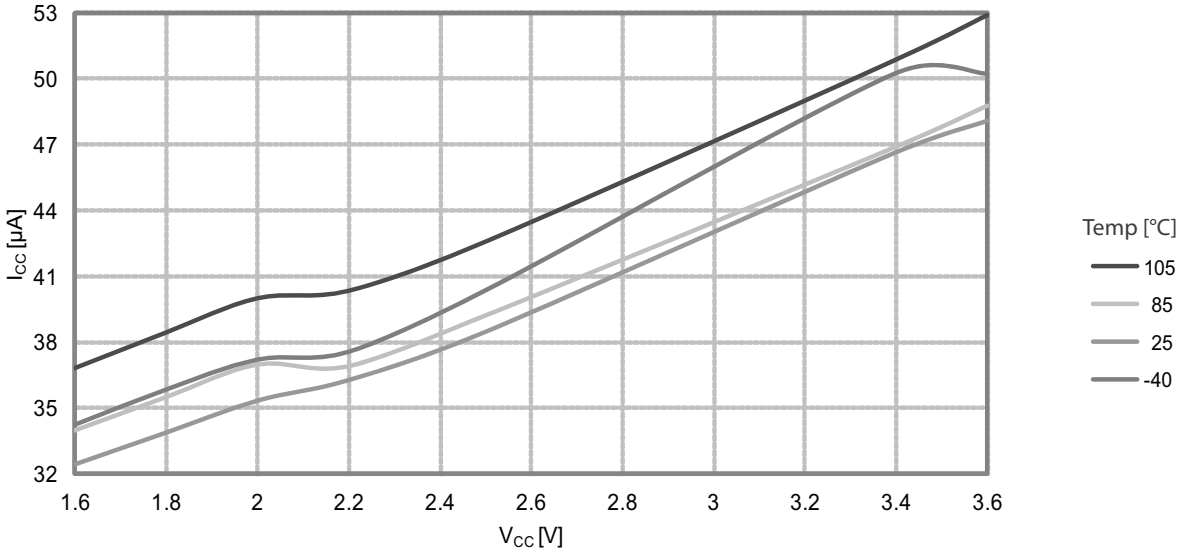


Figure 37-6. Active Mode Supply Current vs. V_{CC}

***f_{SYS} = 32MHz internal oscillator*.**

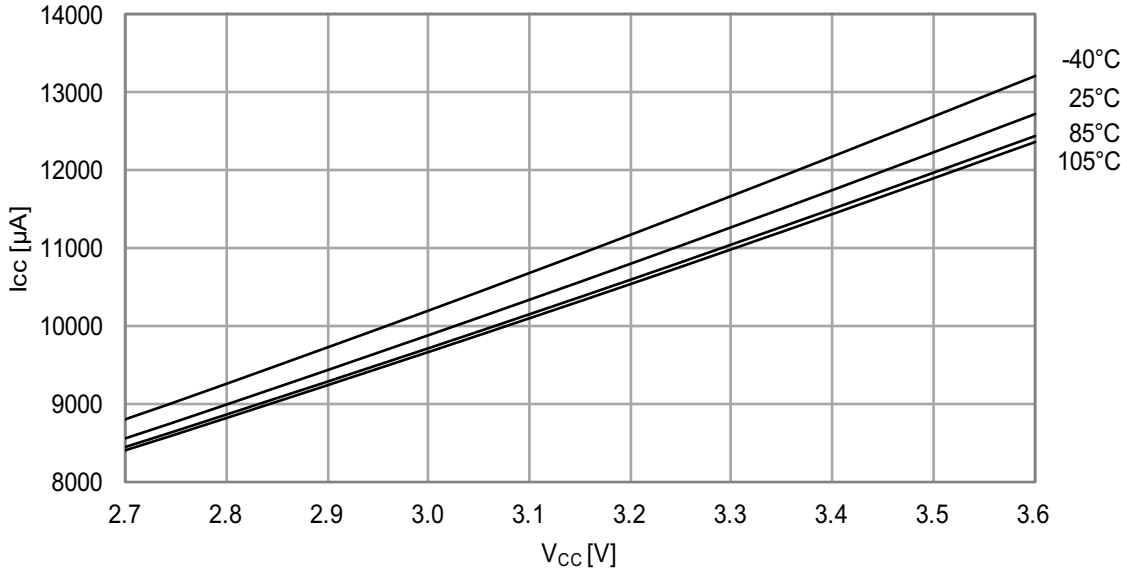
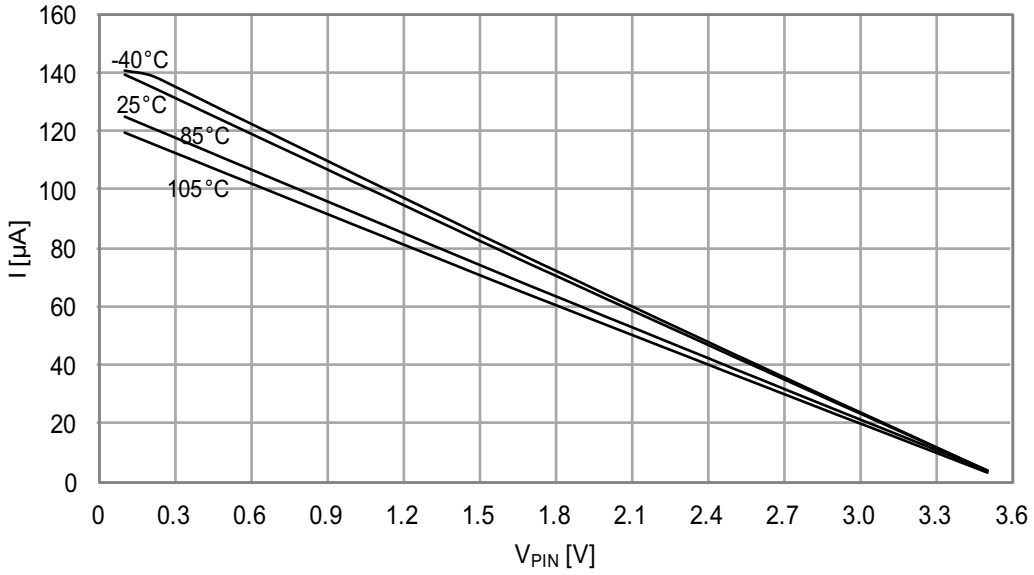


Figure 37-19. I/O Pin Pull-up Resistor Current vs. Pin Voltage

V_{CC} = 3.3V.



37.2.2 Output Voltage vs. Sink/Source Current

Figure 37-20. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V.

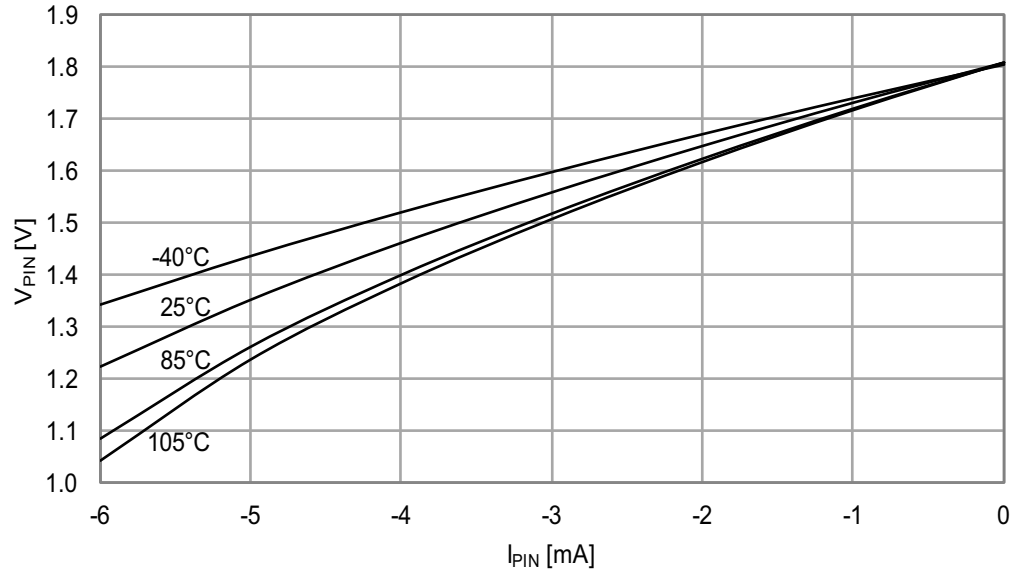


Figure 37-21. I/O Pin Output Voltage vs. Source Current
V_{CC} = 3.0V.

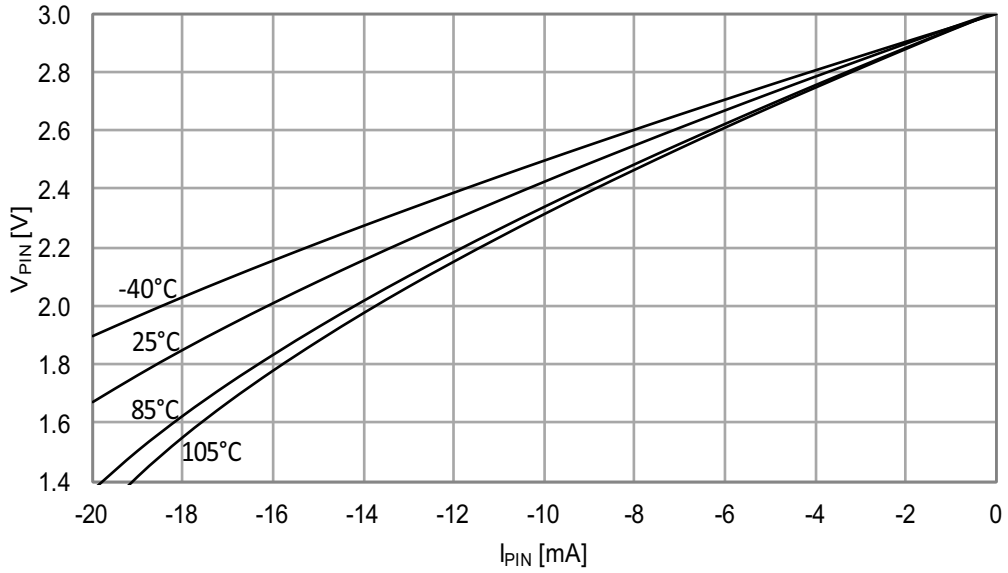
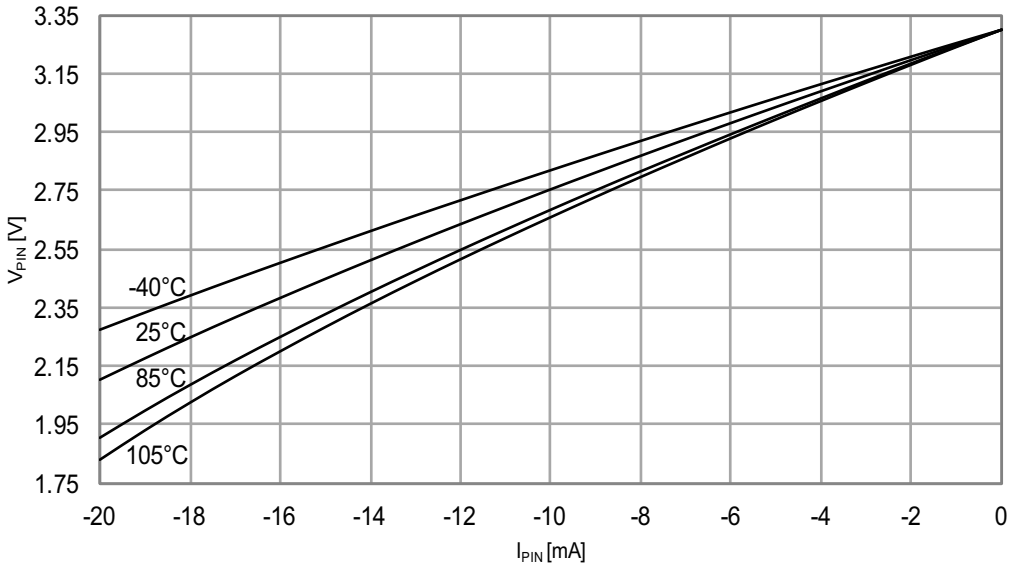


Figure 37-22. I/O Pin Output Voltage vs. Source Current
V_{CC} = 3.3V.



37.3 ADC Characteristics

Figure 37-29. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference.

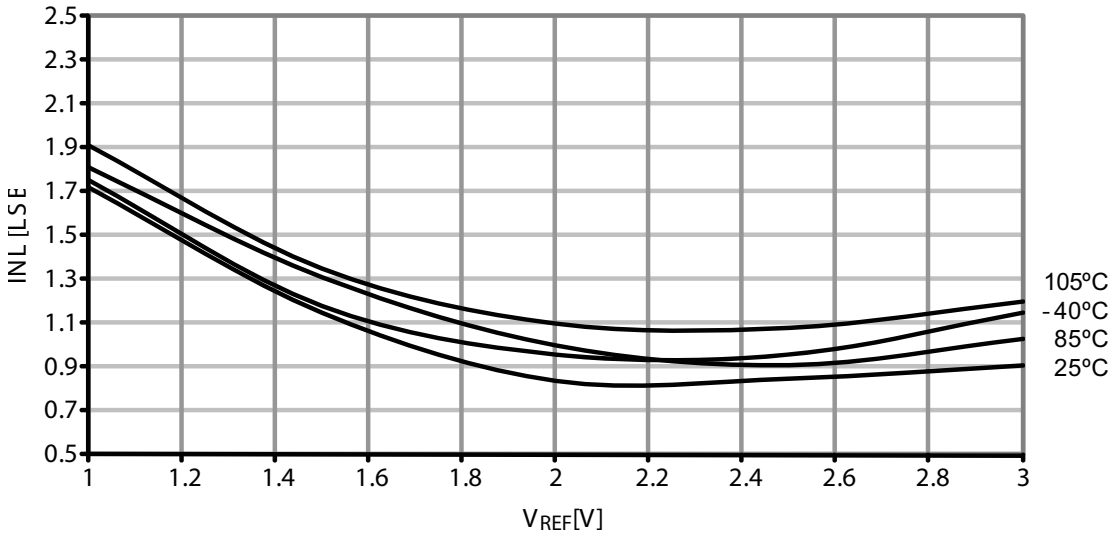


Figure 37-30. ADC INL vs. V_{REF}

SE Unsigned mode, V_{CC} = 3.6V external reference.

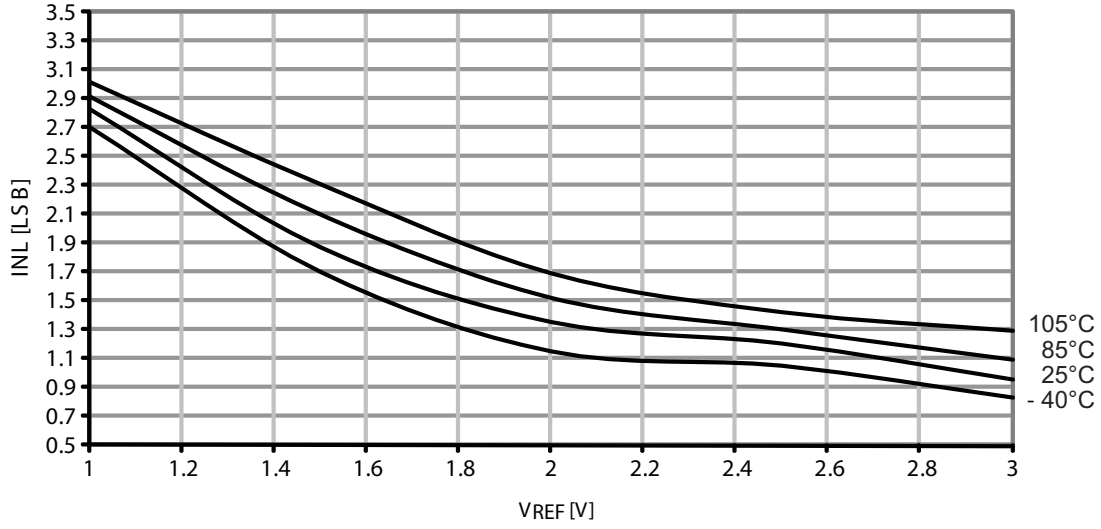


Figure 37-39. ADC Gain Error vs. V_{CC}.

Differential signed mode, external reference.

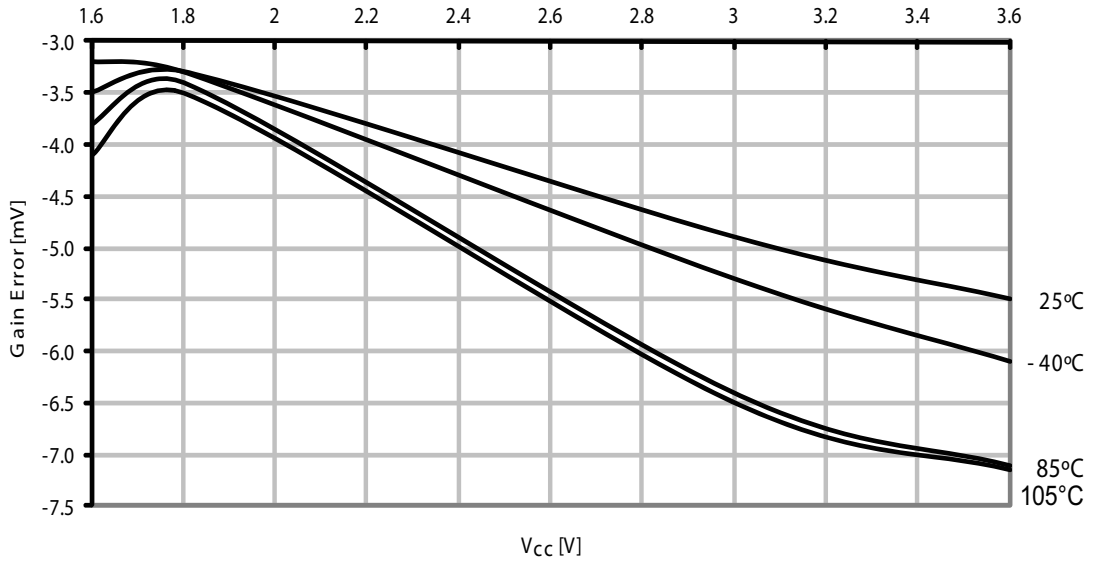


Figure 37-40. ADC Gain Error vs. V_{CC}.

SE Unsigned mode, external reference.

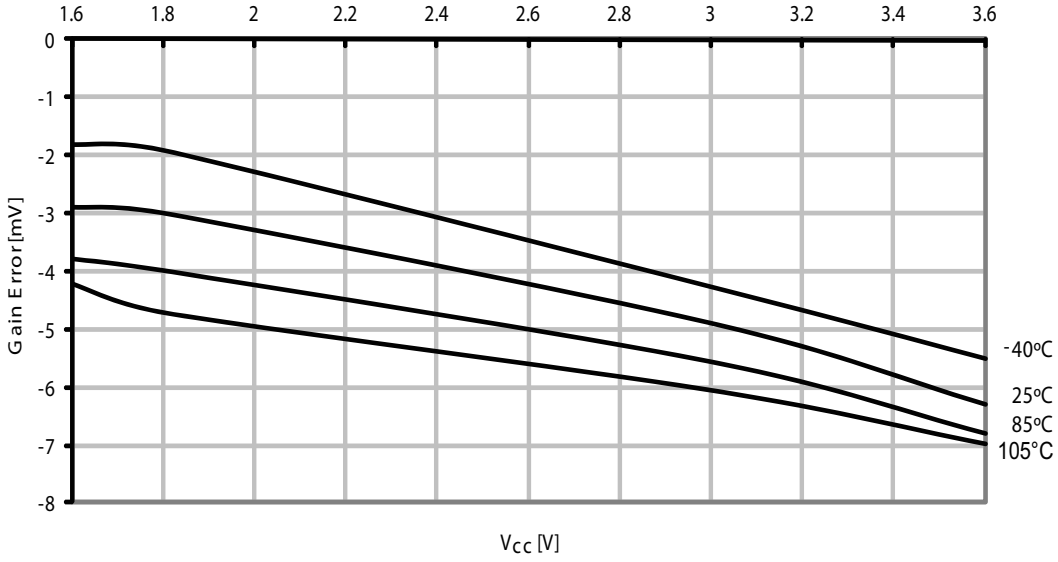


Figure 37-41. ADC Gain Error vs. Temperature

Differential signed mode, external reference.

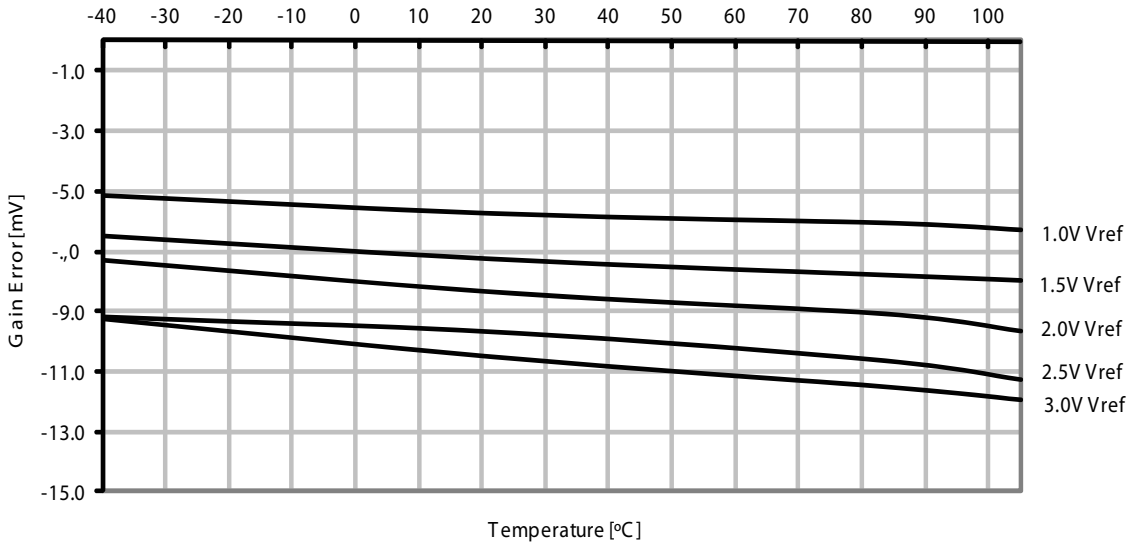


Figure 37-42. ADC Gain Error vs. Temperature

SE Unsigned mode, V_{CC} = 3.6V, external reference.

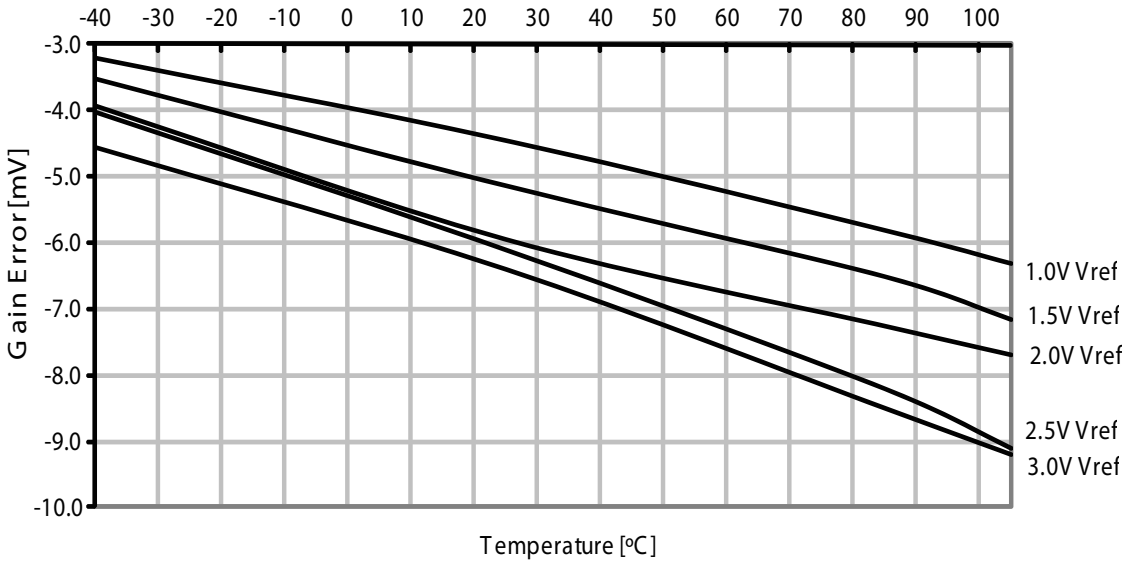


Figure 37-45. Analog Comparator Propagation Delay vs. V_{CC}

***High speed mode*.**

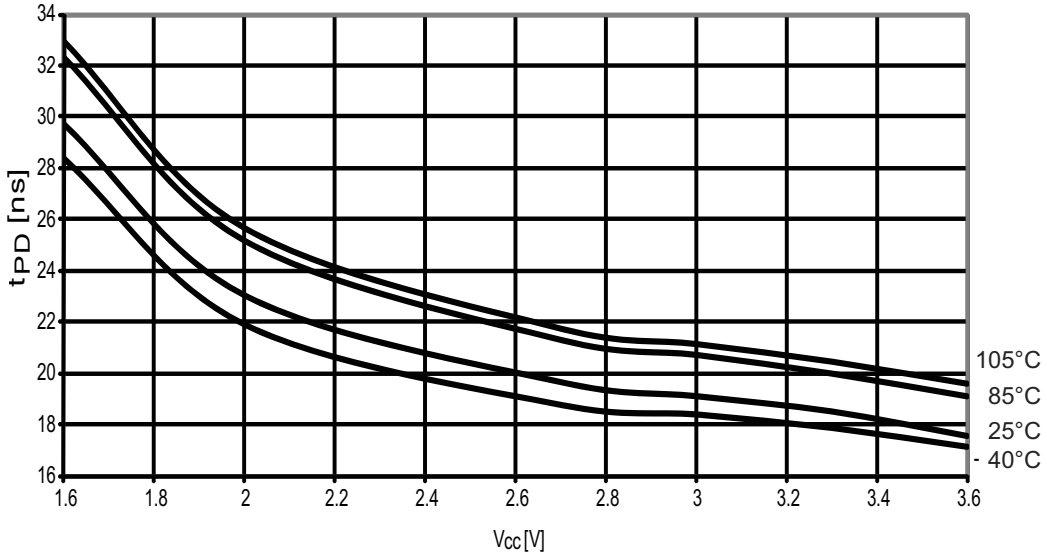


Figure 37-46. Analog Comparator Current Consumption vs. V_{CC}

High-speed mode.

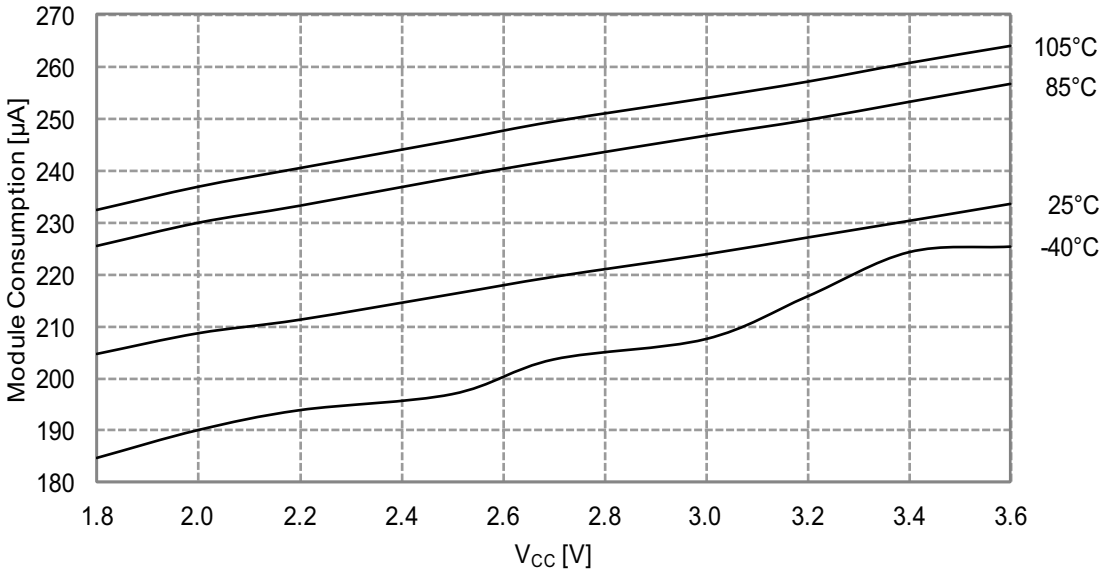


Figure 37-61. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - Reset pin read as "0".

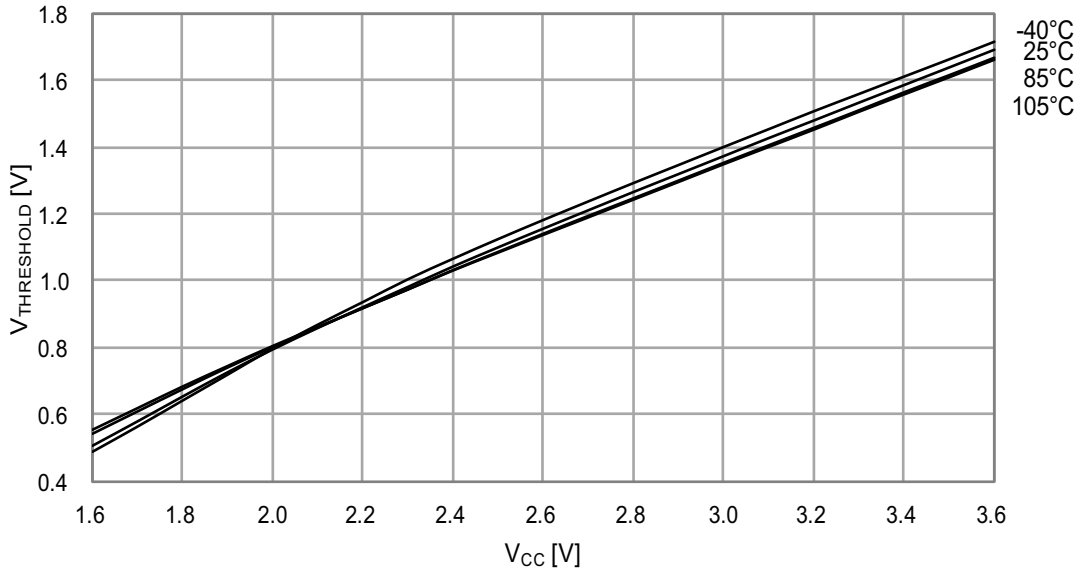


Figure 37-72. 32MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V.

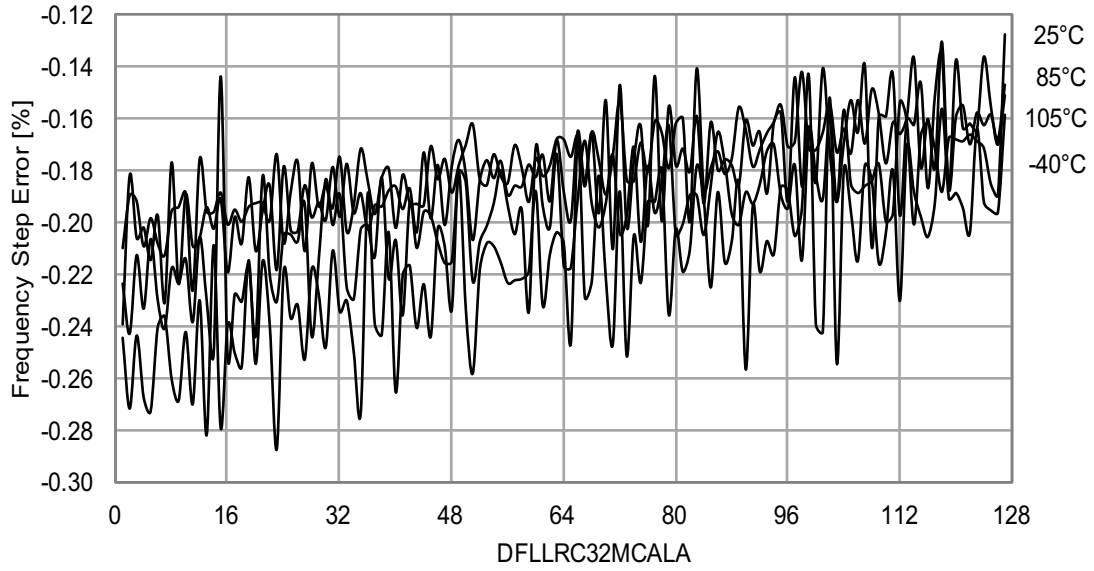
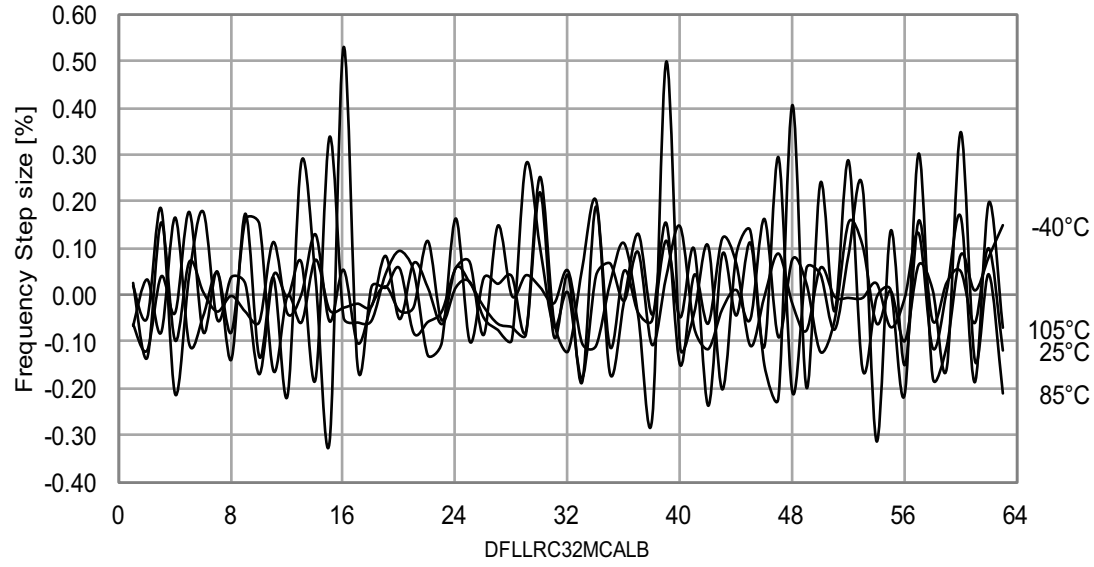


Figure 37-73. 32MHz Internal Oscillator CALB Calibration Step Size

V_{CC} = 3.0V, CALA = mid value.



39.5 8330D – 01/2013

1.	Updated “Ordering Information” on page 2: Added -AUR, -CU and -CUR options.
2.	Updated “Packaging Information” : Added package drawing for “7A1” on page 68.
3.	Updated Table 32-5 on page 57: PDI and RESET pins updated.
4.	Updated pin number for PR1 to pin 81 in Table 32-8 on page 59.
5.	Updated “External clock with prescaler for system clock” Table 36-26 on page 84.
6.	Added ESR parameter to the “External 16MHz crystal oscillator and XOSC characteristics.” Table 36-27 on page 84.

39.6 8330C – 07/2012

1.	Updated the Table 32-4 on page 57. PDI_CLOCK is on pin 16 and PDI_DATA on pin 15.
2.	Updated the datasheet using the Atmel new template.
3.	Updated “Errata” , “Rev. C” on page 136: “JTAG revision” replaced by “Device revision number”.

39.7 8330B – 02/2012

1.	Updated the Table 7-2 on page 16. The page size (words) for ATxmega128B1 changed from 256 to 128.
2.	Updated all “Electrical Characteristics” on page 69.
3.	Updated all “Typical Characteristics” on page 91.
4.	Updated “Errata” on page 136.

39.8 8330A – 10/2011

1.	Initial revision.