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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

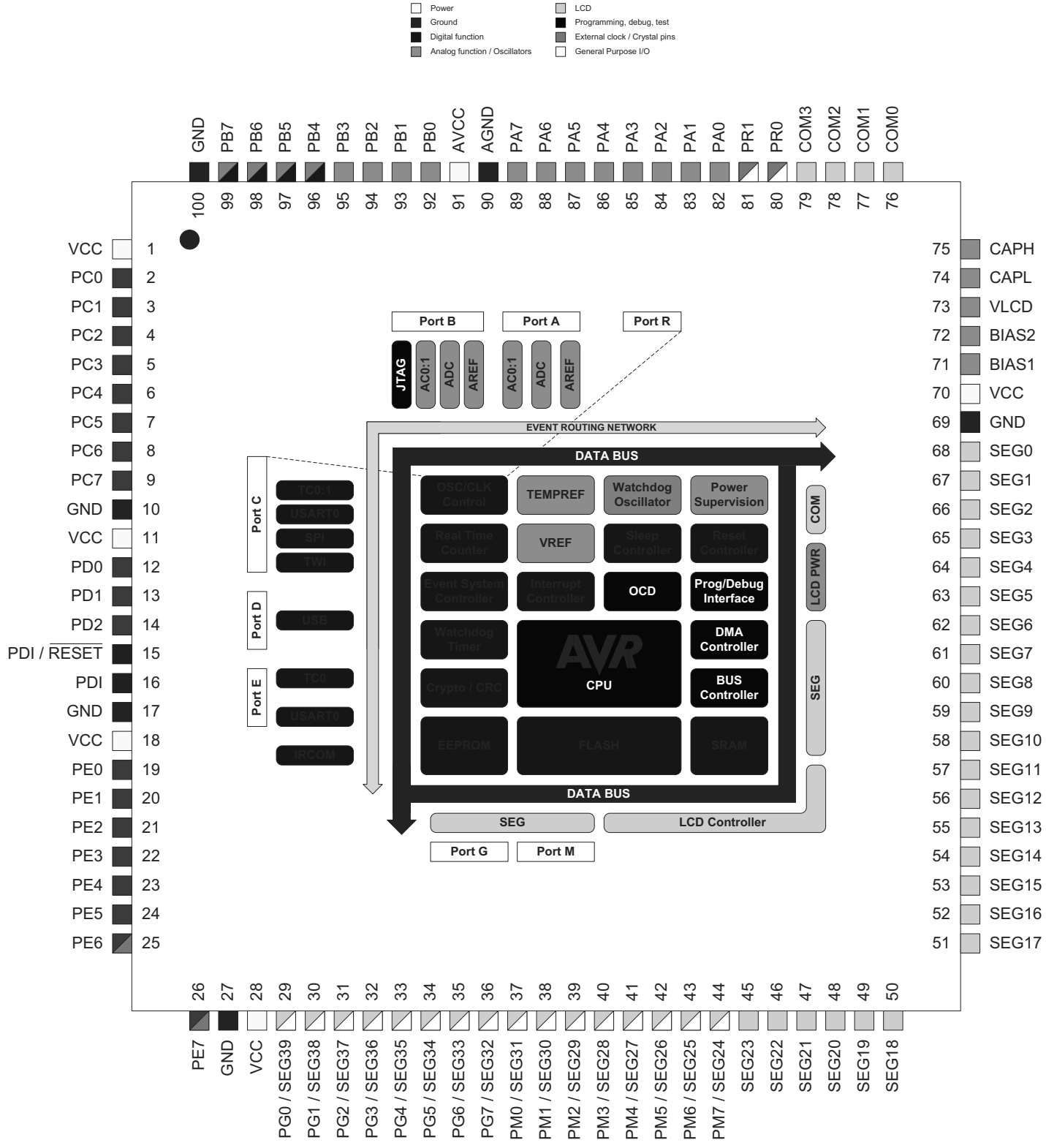
Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64b1-aur

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

2. Pinout/Block Diagram

Figure 2-1. Block Diagram and Pinout



Note: 1. For full details on pinout and alternate pin functions refer to “Pinout and Pin Functions” on page 54.

3. Overview

The Atmel® AVR® XMEGA® is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the Atmel AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The Atmel AVR XMEGA B1 devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; two-channel DMA controller, four-channel event system and programmable multilevel interrupt controller, 53 general purpose I/O lines, real-time counter (RTC); Liquid Crystal Display supporting up to 4x40 segment driver, ASCII character mapping and built-in contrast control (LCD); three flexible, 16-bit timer/counters with compare and PWM channels; two USARTs; one two-wire serial interface (TWI); one full speed USB 2.0 interface; one serial peripheral interface (SPI); AES and DES cryptographic engine; two 8-channel, 12-bit ADCs with programmable gain; four analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available. The devices also have an IEEE std. 1149.1 compliant JTAG interface, and this can also be used for on-chip debug and programming.

The ATx devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, DMA controller, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In power-save mode, the LCD controller is allowed to refresh data to the panel. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run, and the LCD controller is allowed to refresh data to the panel. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

Atmel offers a free QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI or JTAG interfaces. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the Atmel XMEGA B1 is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

The atmel AVR ATx devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended Reading

- XMEGA B Manual
- XMEGA Application Notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA B Manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentations are available from www.atmel.com/avr.

5. Capacitive Touch Sensing

The Atmel QTouch® library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

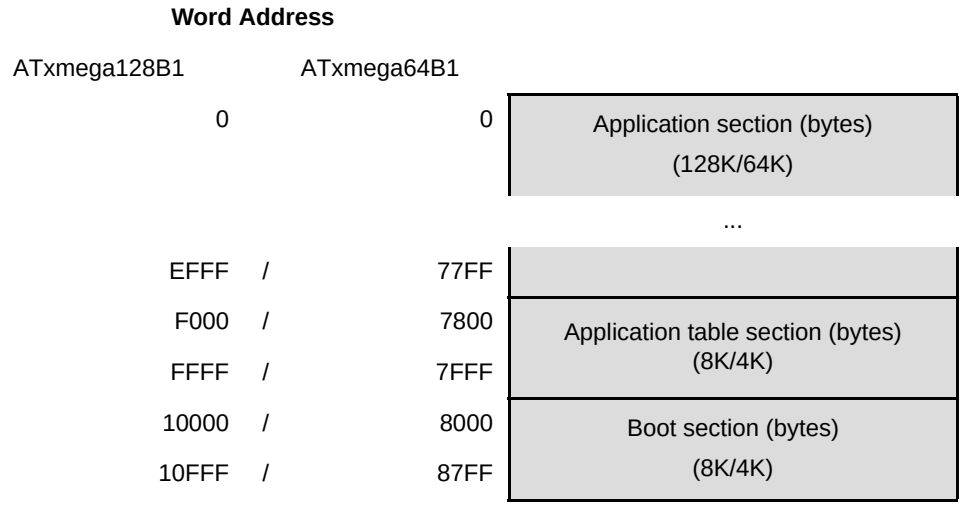
7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system re-programmable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16- or 32-bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash Program Memory (hexadecimal address)



7.3.1 Application Section

The application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 69.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1 on page 14.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes for XMEGA B1 Devices

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega64B1	52	96	1E
ATxmega128B1	4D	97	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (i.e., if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are re-programmable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM and optionally memory mapped EEPROM. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM, and SRAM will always have the same start addresses for all XMEGA devices.

7.11 JTAG Disable

It is possible to disable the JTAG interface from the application software. This will prevent all external JTAG access to the device until the next device reset or until JTAG is enabled again from the application software. As long as JTAG is disabled, the I/O pins required for JTAG can be used as normal I/O pins.

7.12 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.13 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-2 on page 16 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of Words and Pages in the Flash

Devices	PC size	Flash	Page size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No. of pages	Size	No. of pages
ATxmega64B1	16	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128B1	17	128K + 8K	128	Z[8:1]	Z[17:9]	128K	512	8K	32

Table 7-3 on page 16 shows EEPROM memory organization for the XMEGA B1 devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 7-3. Number of Bytes and Pages in the EEPROM

Devices	EEPROM	Page size	E2BYTE	E2PAGE	No. of pages
	Size	Bytes			
ATxmega64B1	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128B1	2K	32	ADDR[4:0]	ADDR[10:5]	64

12.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

12.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

12.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see “WDT – Watchdog Timer” on page 27.

12.4.5 Software Reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register.The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

12.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

28. LCD - Liquid Crystal Display Controller

28.1 Features

- Display capacity up to 40 segment and up to four common terminals
- Supports up to 16 GPIOs
- Shadow display memory gives full freedom in segment update
- ASCII character mapping
- Swap capability option on segment and/or common terminal buses
- Supports from static up to 1/4 duty
- Supports static and 1/3 bias
- LCD driver active in power save mode for low power operation
- Software selectable low power waveform
- Flexible selection of frame frequency
- Programmable blink mode and frequency on two segment terminals
- Uses Only 32kHz RTC clock source
- On-chip LCD power supply
- Software contrast adjustment control
- Equal source and sink capability to Increase glass life time
- Extended interrupt mode for display update or wake-up from sleep mode

28.2 Overview

The LCD controller is intended for monochrome passive liquid crystal display (LCD) with up to four common terminals and up to 40 Segments terminals. If the application does not need all the LCD segments available on the XMEGA, up to 16 of the unused LCD pins can be used as general purpose I/O pins.

The LCD controller can be clocked by an internal or an external asynchronous 32kHz clock source. This 32kHz oscillator source selection is the same as for the real time counter (RTC).

Dedicated Low Power Waveform, Contrast Control, Extended Interrupt Mode, Selectable Frame Frequency and Blink functionality are supported to off-load the CPU, reduce interrupts and reduce power consumption.

To reduce hardware design complexity, the LCD includes integrated LCD buffers, an integrated power supply voltage and an innovative SWAP mode. Using SWAP mode, the hardware designers have more flexibility during board layout as they can rearrange the pin sequence on Segment and/or Common Terminal Buses.

Figure 28-1. LCD Overview

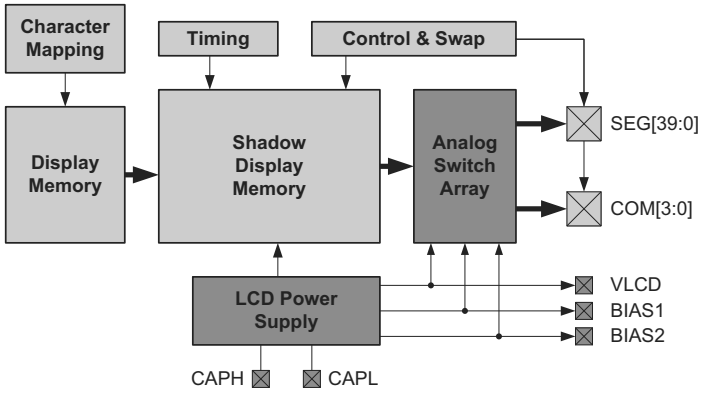
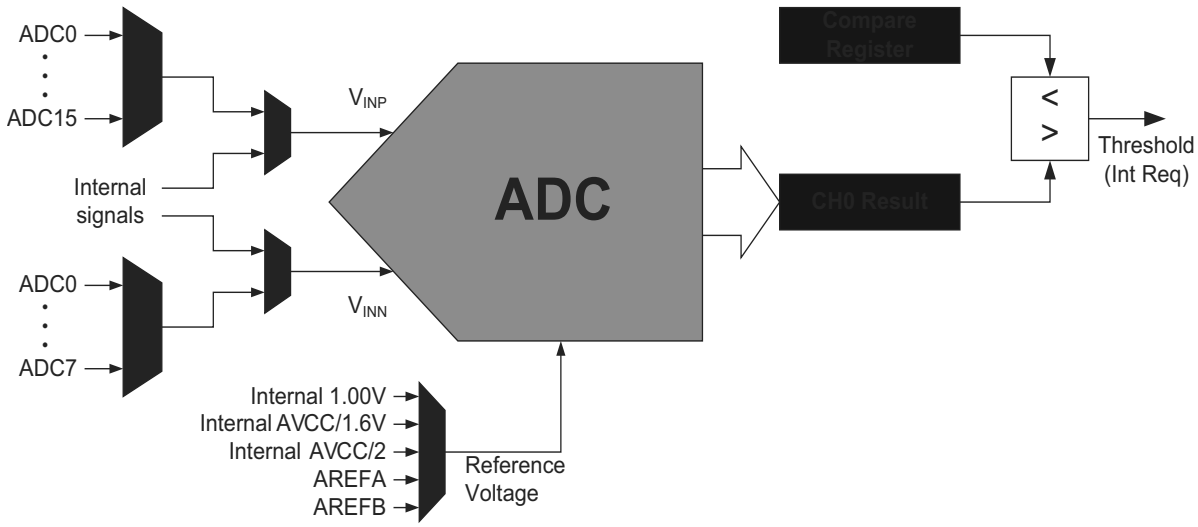


Figure 29-1. ADC Overview



The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.35µs for 12-bit to 2.3µs for 8-bit result.

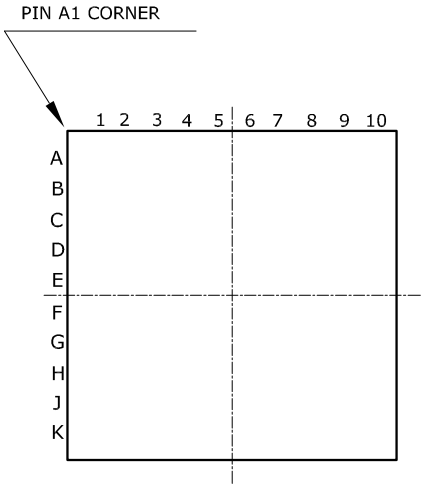
ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each has one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

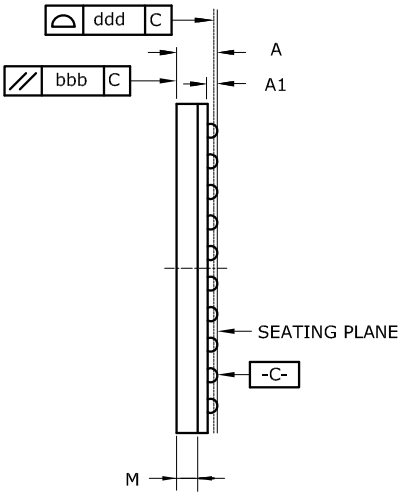
Base address	Name	Description
0x0800	TCC0	Timer/Counter 0 on port C
0x0840	TCC1	Timer/Counter 1 on port C
0x0880	AWEXC	Advanced Waveform Extension on port C
0x0890	HIRESC	High Resolution Extension on port C
0x08A0	USARTC0	USART 0 on port C
0x08C0	SPIC	Serial Peripheral Interface on port C
0x08F8	IRCOM	Infrared Communication Module
0x0A00	TCE0	Timer/Counter 0 on port E
0x0AA0	USARTE0	USART 0 on port E
0x0D00	LCD	Liquid Crystal Display

35.2 7A1

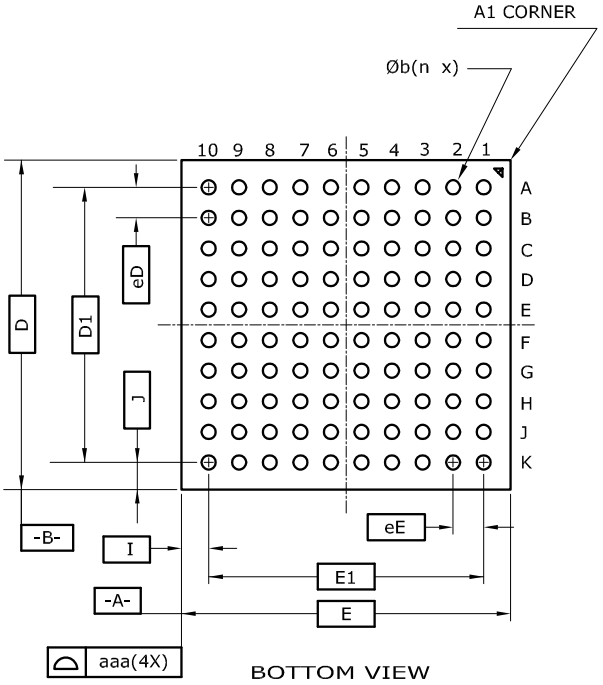
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.00	
A1	0.160	-----	0.260	
E/D	7.00 / 7.00			
E1/D1	5.85 / 5.85			
I/J	0.575			
eD/eE	Ball pitch : 0.650			
b	0.270	-----	0.370	
M	Mold thickness : 0.450 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Copla : 0.080			
ball diam	0.300			
n	100			

Notes : 1. No JEDEC Drawing Reference.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

12/21/2011

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	7A, 100-ball (10x10 array), 0.65mm pitch, 7x7x1mm Very Thin Fine-Pitch Ball Grid Array Package (VFBGA)	CAF	7A	B

36.13 Flash and EEPROM Memory Characteristics

Table 36-18. Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/erase cycles	25°C	10K			Cycle
			85°C	10K			
		Data retention	25°C	100			Year
			55°C	25			
	EEPROM	Write/erase cycles	25°C	100K			Cycle
			85°C	100K			
		Data retention	25°C	100			Year
			55°C	25			

Table 36-19. Programming Time

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
	Chip Erase	128KB flash, EEPROM(2)		75		ms
		64KB flash, EEPROM(2)		55		
	Flash	Page Erase		4		ms
		Page Write		4		
		Page Write Automatic Page Erase and Write		8		
	EEPROM	Page Erase		4		ms
		Page Write		4		
		Page Write Automatic Page Erase and Write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

36.14 Clock and Oscillator Characteristics

36.14.1 Calibrated 32.768kHz Internal Oscillator Characteristics

Table 36-20. Calibrated 32.768kHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibrated accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

36.14.2 Calibrated 2MHz RC Internal Oscillator Characteristics

Table 36-21. Calibrated 2MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.22		%

36.14.3 Calibrated and tunable 32MHz Internal Oscillator Characteristics

Table 36-22. Calibrated 32MHz Internal Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		35	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.23		%

36.14.4 32kHz Internal ULP Oscillator Characteristics

Table 36-23. 32kHz Internal ULP Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-12		12	%

36.14.5 Phase Locked Loop (PLL) Characteristics

Table 36-24. Internal PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency(1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			23	100	µs
	re-lock time			20	50	µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.14.6 External Clock Characteristics

Figure 36-3. External Clock Drive Waveform

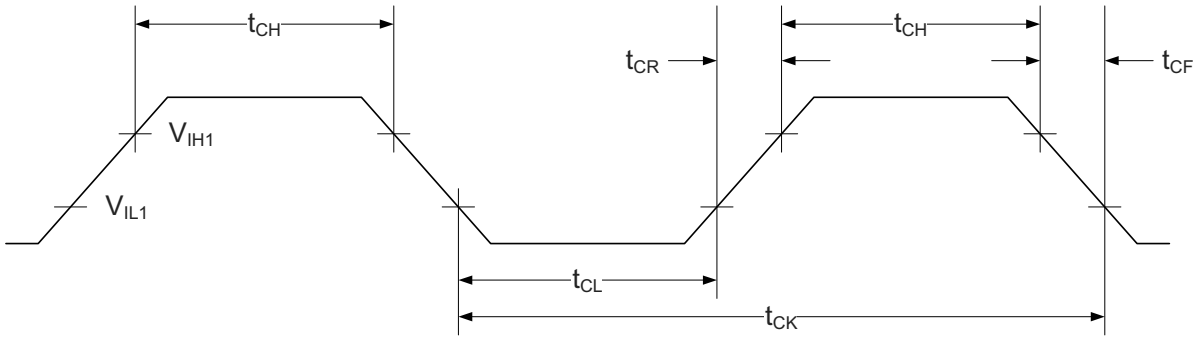


Table 36-25. External Clock used as System Clock without Prescaling

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock frequency(1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock high time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock low time	V_{CC} = 1.6 - 1.8V	30.0			
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.8V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		
	ESR	SF = Safety factor				min(RQ)/ SF	kΩ

37.1.3 Power-down Mode Supply Current

Figure 37-13. Power-down Mode Supply Current vs. Temperature

***All functions disabled*.**

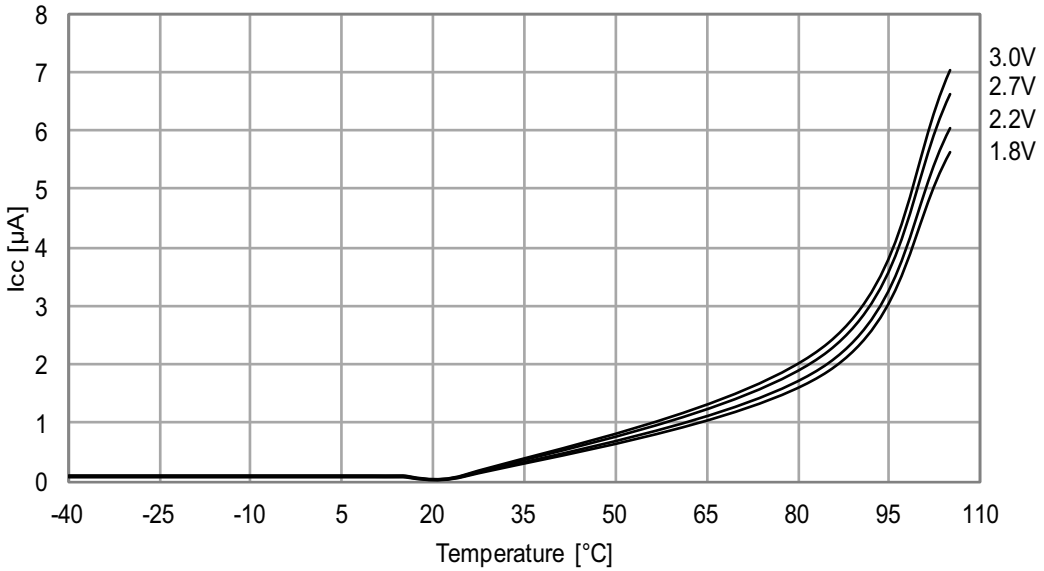


Figure 37-14. Power-down Mode Supply Current vs. Temperature

***Watchdog and sampled BOD enabled*.**

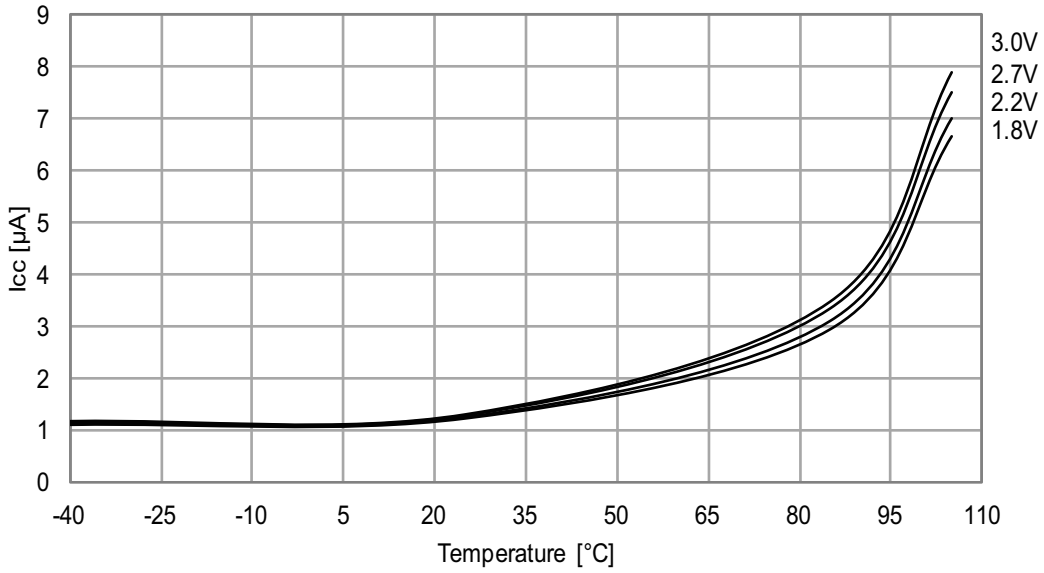
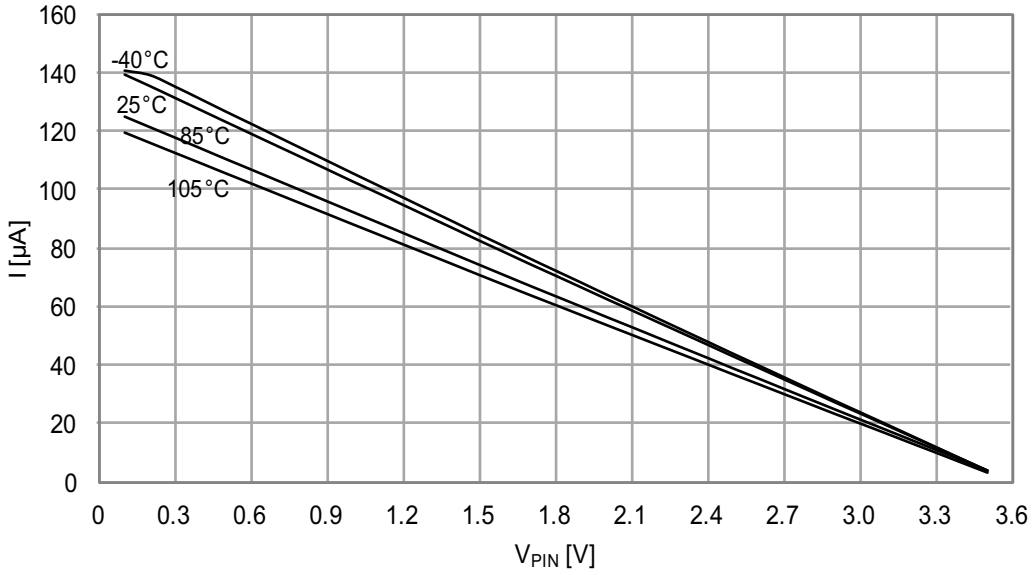


Figure 37-19. I/O Pin Pull-up Resistor Current vs. Pin Voltage

V_{CC} = 3.3V.



37.2.2 Output Voltage vs. Sink/Source Current

Figure 37-20. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V.

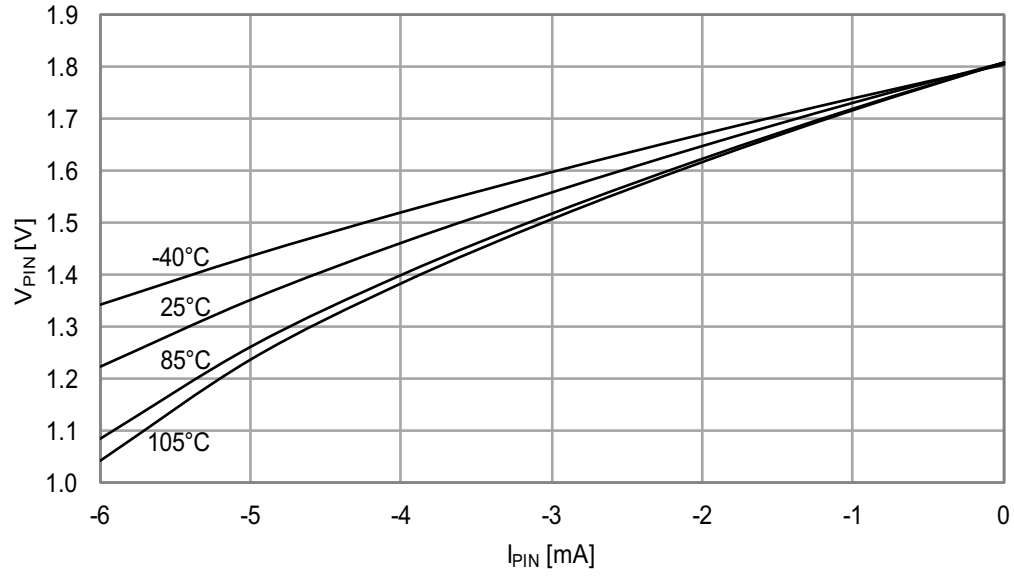


Figure 37-87. P_{SAVE} LCD LP 32Hz vs. Temperature
RTC, WDT, BOD sampled.

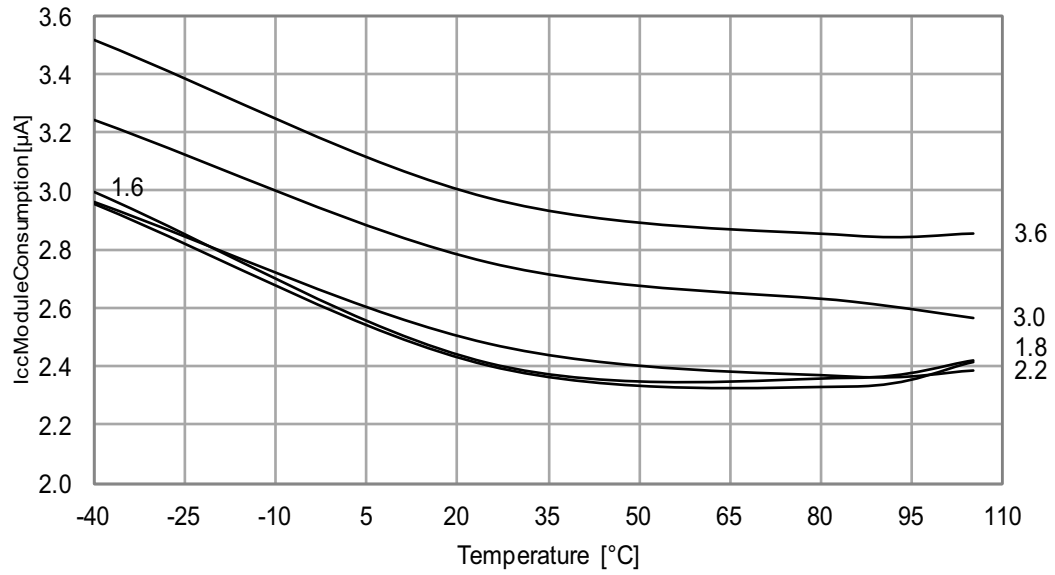
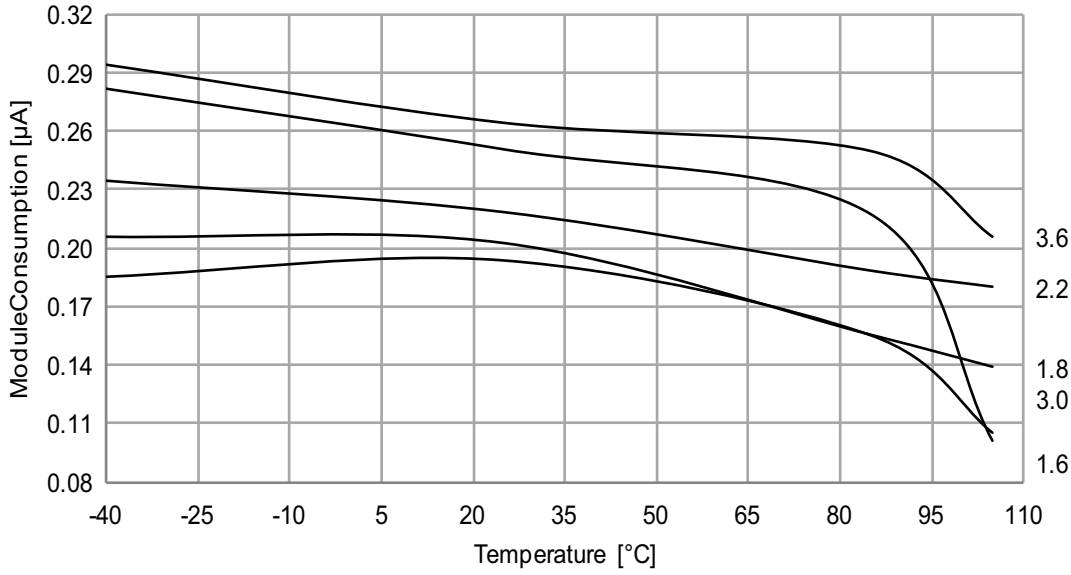


Figure 37-88. P_{SAVE} vs. Temperature
***RTC, WDT, BOD sampled*.**



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