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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1947-e-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC16(L)F1946/1947

4.2 Register Definitions: Configuration Words

R/P-1 **R/P-1** R/P-1 R/P-1 R/P-1 R/P-1 CPD **FCMEN IESO** CLKOUTEN BOREN<1:0> bit 13 bit 8 R/P-1 R/P-1 R/P-1 **R/P-1** R/P-1 R/P-1 R/P-1 R/P-1 CP PWRTE **MCLRE** WDTE<1:0> FOSC<2:0> bit 7 bit 0 Legend: R = Readable bit P = Programmable bit U = Unimplemented bit, read as '1' '0' = Bit is cleared -n = Value when blank or after Bulk Erase '1' = Bit is set bit 13 FCMEN: Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor is enabled 0 = Fail-Safe Clock Monitor is disabled IESO: Internal External Switchover bit bit 12 1 = Internal/External Switchover mode is enabled 0 = Internal/External Switchover mode is disabled **CLKOUTEN:** Clock Out Enable bit bit 11 If FOSC configuration bits are set to LP, XT, HS modes: This bit is ignored, CLKOUT function is disabled. Oscillator function on the CLKOUT pin. All other FOSC modes: 1 = CLKOUT function is disabled. I/O function on the CLKOUT pin. 0 = CLKOUT function is enabled on the CLKOUT pin BOREN<1:0>: Brown-out Reset Enable bits⁽¹⁾ bit 10-9 11 = BOR enabled 10 = BOR enabled during operation and disabled in Sleep 01 = BOR controlled by SBOREN bit of the BORCON register 00 = BOR disabled CPD: Data Code Protection bit⁽²⁾ bit 8 1 = Data memory code protection is disabled 0 = Data memory code protection is enabled **CP:** Code Protection bit⁽³⁾ bit 7 1 = Program memory code protection is disabled 0 = Program memory code protection is enabled bit 6 MCLRE: MCLR/VPP Pin Function Select bit If LVP bit = 1: This bit is ignored. If LVP bit = 0: 1 = \overline{MCLR}/VPP pin function is \overline{MCLR} ; Weak pull-up enabled. 0 = MCLR/VPP pin function is digital input; MCLR internally disabled; Weak pull-up under control of WPUG5 bit.

REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1

- **Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
 - 2: The entire data EEPROM will be erased when the code protection is turned off during an erase.
 - 3: The entire program memory will be erased when the code protection is turned off.

4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the \overline{CP} bit in Configuration Words. When $\overline{CP} = 0$, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.4** "Write **Protection**" for more information.

4.3.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the \overline{CPD} bit. When $\overline{CPD} = 0$, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 4.6 "Device ID and Revision ID**" for more information on accessing these memory locations. For more information on checksum calculation, see the "*PIC16F193X/LF193X/PIC16F194X/LF190X Memory Programming Specification*" (DS41397).

5.2.1.5 TIMER1 Oscillator

The Timer1 Oscillator is a separate crystal oscillator that is associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

The Timer1 Oscillator can be used as an alternate system clock source and can be selected during run-time using clock switching. Refer to **Section 5.3** "**Clock Switching**" for more information.

FIGURE 5-5: QUARTZ CRYSTAL OPERATION (TIMER1 OSCILLATOR)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
 - Always verify oscillator performance over the VDD and temperature range that is expected for the application.
 - **3:** For oscillator design assistance, reference the following Microchip Applications Notes:
 - AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC[®] and PIC[®] Devices (DS00826)
 - AN849, Basic PICmicro[®] Oscillator Design (DS00849)
 - AN943, Practical PICmicro[®] Oscillator Analysis and Design (DS00943)
 - AN949, Making Your Oscillator Work (DS00949)
 - TB097, Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS (DS91097)
 - AN1288, Design Practices for Low-Power External Oscillators (DS01288)

5.2.1.6 External RC Mode

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required.

The RC circuit connects to OSC1. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

Figure 5-6 shows the external RC mode connections.

FIGURE 5-6: EXTERNAL RC MODES



The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- · packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
				TUN	<5:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	1 as '0'	
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other						other Resets	
'1' = Bit is set '0' = Bit is cleared							
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5-0	TUN<5:0>: F	requency Tunir	ng bits				
	100000 = M	inimum frequer	псу				
	•						
	•						
	•						
	111111 = 0		io rupping of	the feater cali	aratad fraguas		
	000000 = 0	scinator module	e is running at	the factory-call	orated frequent	cy.	
	•						
	•						
	•						
	011110 =						
	011111 = M	aximum freque	ncy				

REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN		IRCI	=<3:0>		—	SCS	<1:0>	74
OSCSTAT	T10SCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	75
OSCTUNE	—	—			TUN	<5:0>			76
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	LCDIE	C3IE	CCP2IE ⁽¹⁾	92
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	LCDIF	C3IF	CCP2IF ⁽¹⁾	96
T1CON	TMR1C	S<1:0>	T1CKP	'S<1:0>	T1OSCEN	T1SYNC	_	TMR10N	197

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

Note 1: PIC16F1947 only.

TABLE 5-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
	13:8		—	FCMEN	IESO	CLKOUTEN	BORE	N<1:0>	CPD	54
CONFIGT	7:0	CP	MCLRE	PWRTE	WDTE	E<1:0>		FOSC<2:0>		54
CONFICE	13:8		_	LVP	DEBUG	—	BORV	STVREN	PLLEN	50
CONFIGZ	7:0		_		VCAPEN	_		WRT	<1:0>	50

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

Note 1: PIC16F1946/47 only.

REGISTER 12-18:	LATE: PORTE DATA LATCH REGISTER
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R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0
bit 7		·					bit 0
Legend:							
R = Readable b	oit	W = Writable b	oit	U = Unimplem	nented bit, read a	as '0'	
u = Bit is uncha	nged	x = Bit is unkn	own	-n/n = Value a	t POR and BOR	/Value at all oth	er Resets
'1' = Bit is set		'0' = Bit is clea	ared				

bit 7-0 LATE<7:0>: PORTE Output Latch Value bits⁽¹⁾

Note 1: Writes to PORTE are actually written to corresponding LATE register. Reads from PORTE register is return of actual I/O pin values.

REGISTER 12-19: ANSELE: PORTE ANALOG SELECT REGISTER

| R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| — | — | — | — | — | ANSE2 | ANSE1 | ANSE0 |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ANSE<7:0>**: Analog Select between Analog or Digital Function on Pins RE<7:0>, respectively 0 = Digital I/O. Pin is assigned to port or digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

TABLE 12-12: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON	P3CSEL	P3BSEL	P2DSEL	P2CSEL	P2BSEL	CCP2SEL	P1CSEL	P1BSEL	123
ANSELE	—	—	—	—	—	ANSE2	ANSE1	ANSE0	138
CCPxCON	PxM<	1:0> (1)	DCxB	<1:0>		CCPx	M<3:0>		227
LATE	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	138
LCDCON	LCDEN	SLPEN	WERR	—	CS<	:1:0>	LMUX	<1:0>	326
LCDREF	LCDIRE	LCDIRS	LCDIRI	—	VLCD3PE	VLCD2PE	VLCD1PE	—	328
LCDSE2	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	330
PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	137
TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	137

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTE.

Note 1: Applies to ECCP modules only.

- Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.
 - 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
 - **3:** The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.









17.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- · ADC input channel
- DACOUT pin
- Capacitive Sensing module (CPS)

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the DACCON0 register.

EQUATION 17-1: DAC OUTPUT VOLTAGE

<u>IF DACEN = 1</u>

 $VOUT = \left((VSOURCE + -VSOURCE -) \times \frac{DACR[4:0]}{2^5} \right) + VSOURCE -$

<u>IF DACEN = 0 & DACLPS = 1 & DACR[4:0] = 11111</u>

VOUT = VSOURCE +

<u>IF DACEN = 0 & DACLPS = 0 & DACR[4:0] = 00000</u>

VOUT = VSOURCE -

VSOURCE+ = VDD, VREF, or FVR BUFFER 2

VSOURCE- = VSS

17.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in **Section 30.0** "**Electrical Specifications**".

17.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DACR<4:0> bits of the DACCON1 register.

The DAC output voltage is determined by the following equations:

17.3 DAC Voltage Reference Output

The DAC can be output to the DACOUT pin by setting the DACOE bit of the DACCON0 register to '1'. Selecting the DAC reference voltage for output on the DACOUT pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACOUT pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to DACOUT. Figure 17-2 shows an example buffering technique.

PIC16(L)F1946/47



FIGURE 19-1: SR LATCH SIMPLIFIED BLOCK DIAGRAM

			-		- Period	
00	(Single Output)	PxA Modulated	= — <u>і́ </u>			
		PxA Modulated	- ' -		 Delav	
10	(Half-Bridge)	PxB Modulated		ay		
		PxA Active	_		· · · · · · · · · · · · · · · · · · ·	
01	(Full-Bridge,	PxB Inactive	- <u> </u>			
	i oiwaid)	PxC Inactive	_ <u>'</u> _ <u>'</u>			
		PxD Modulated	= — <u>_</u>			
		PxA Inactive	'		1 1 1	1 1 1
11	(Full-Bridge,	PxB Modulated	- 1_			<u>I</u>
	Reverse)	PxC Active	- ; - ;		· · ·	
		PxD Inactive	- :			,

FIGURE 23-7: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)

Pulse Width = Tosc * (CCPRxL<7:0>:CCPxCON<5:4>) * (TMRx Prescale Value)
Delay = 4 * Tosc * (PWMxCON<6:0>)

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24.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCLx line low effectively, pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and by the hardware that generates SCLx.

The CKP bit of the SSPxCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCLx line to go low and then hold it. Setting CKP will release SCLx and allow more communication.

24.5.6.1 Normal Clock Stretching

Following an \overline{ACK} , if the R/W bit of SSPxSTAT is set, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit of SSPxCON2 is set, the slave hardware will always stretch the clock after the \overline{ACK} sequence. Once the slave is ready, CKP is set by software and communication resumes.

- Note 1: The BF bit has no effect if the clock will be stretched or not. The previous version of the module did not stretch the clock if SSPxBUF was read before the 9th falling edge of SCLx.
 - 2: The previous versions of the module did not stretch the clock for a transmission if SSPxBUF was loaded before the 9th falling edge of SCLx. It is now always cleared for read requests.

24.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCLx is stretched without CKP being cleared. SCLx is released immediately after a write to SSPxADD.

Note:	Previous versions of the module did not
	stretch the clock if the second address byte
	did not match.

24.5.6.3 Byte NACKing

When AHEN bit of SSPxCON3 is set, CKP is cleared by hardware after the eighth falling edge of SCLx for a received matching address byte. When the DHEN bit of SSPxCON3 is set, CKP is cleared after the eighth falling edge of SCLx for received data.

Stretching after the eighth falling edge of SCLx allows the slave to look at the received address or data and decide if it wants to ACK the received data.

24.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCLx line to go low and then hold it. However, clearing the CKP bit will not assert the SCLx output low until the SCLx output is already sampled low. Therefore, the CKP bit will not assert the SCLx line until an external I^2C master device has already asserted the SCLx line. The SCLx output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCLx. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCLx (see Figure 24-23).



FIGURE 24-23: CLOCK SYNCHRONIZATION TIMING

27.7 LCD Multiplex Types

The LCD driver module can be configured into one of four multiplex types:

- Static (only COM0 is used)
- 1/2 multiplex (COM<1:0> are used)
- 1/3 multiplex (COM<2:0> are used)
- 1/4 multiplex (COM<3:0> are used)

The LMUX<1:0> bit setting of the LCDCON register decides which of the LCD common pins are used (see Table 27-4 for details).

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. If the pin is a COM drive, then the TRIS setting of that pin is overridden.

Multiplex	LMUX <1:0>	СОМЗ	COM2	COM1	COM0
Static	00	Unused	Unused	Unused	Active
1/2	01	Unused	Unused	Active	Active
1/3	10	Unused	Active	Active	Active
1/4	11	Active	Active	Active	Active

TABLE 27-4: COMMON PIN USAGE

27.8 Segment Enables

The LCDSEn registers are used to select the pin function for each segment pin. The selection allows each pin to operate as either an LCD segment driver or as one of the pin's alternate functions. To configure the pin as a segment pin, the corresponding bits in the LCDSEn registers must be set to '1'.

If the pin is a digital I/O, the corresponding TRIS bit controls the data direction. Any bit set in the LCDSEn registers overrides any bit settings in the corresponding TRIS register.

Note: On a Power-on Reset, these pins are configured as normal I/O, not LCD pins.

27.9 Pixel Control

The LCDDATAx registers contain bits which define the state of each pixel. Each bit defines one unique pixel.

Register 27-6 shows the correlation of each bit in the LCDDATAx registers to the respective common and segment signals.

Any LCD pixel location not being used for display can be used as general purpose RAM.

27.10 LCD Frame Frequency

The rate at which the COM and SEG outputs change is called the LCD frame frequency.

TABLE 27-5:	FRAME FREQUENCY
	FORMULAS

Multiplex	Frame Frequency ⁽²⁾ =					
Static	Clock source/(4 x (LCD Prescaler) x 32 x 1))					
1/2	Clock source/(2 x (LCD Prescaler) x 32 x 2))					
1/3	Clock source/(1 x (LCD Prescaler) x 32 x 3))					
1/4	Clock source/(1 x (LCD Prescaler) x 32 x 4))					
Note 1:	Clock source is Easc/256 T10SC or					

Note 1: Clock source is Fosc/256, T1OSC or LFINTOSC.

TABLE 27-6: APPROXIMATE FRAME FREQUENCY (IN Hz) USING Fosc @ 8 MHz, TIMER1 @ 32.768 kHz OR LFINTOSC

LP<3:0>	Static	1/2	1/3	1/4
2	122	122	162	122
3	81	81	108	81
4	61	61	81	61
5	49	49	65	49
6	41	41	54	41
7	35	35	47	35

^{2:} See Figure 27-2.

27.13 Operation During Sleep

The LCD module can operate during Sleep. The selection is controlled by bit SLPEN of the LCDCON register. Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

If a SLEEP instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very low-current Consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 27-20 shows this operation.

The LCD module can be configured to operate during Sleep. The selection is controlled by bit SLPEN of the LCDCON register. Clearing SLPEN and correctly configuring the LCD module clock will allow the LCD module to operate during Sleep. Setting SLPEN and correctly executing the LCD module shutdown will disable the LCD module during Sleep and save power.

If a SLEEP instruction is executed and SLPEN = 1, the LCD module will immediately cease all functions, drive the outputs to Vss and go into a very low-current mode. The SLEEP instruction should only be executed after the LCD module has been disabled and the current cycle completed, thus ensuring that there are no DC voltages on the glass. To disable the LCD module, clear the LCDEN bit. The LCD module will complete the disabling process after the current frame, clear the LCDA bit and optionally cause an interrupt.

The steps required to properly enter Sleep with the LCD disabled are:

- Clear LCDEN
- Wait for LCDA = 0 either by polling or by interrupt
- Execute SLEEP

If SLPEN = 0 and SLEEP is executed while the LCD module clock source is FOSC/4, then the LCD module will halt with the pin driving the last LCD voltage pattern. Prolonged exposure to a fixed LCD voltage pattern will cause damage to the LCD glass. To prevent LCD glass damage, either perform the proper LCD module shutdown prior to Sleep, or change the LCD module clock to allow the LCD module to continue operation during Sleep.

If a SLEEP instruction is executed and SLPEN = 0 and the LCD module clock is either T1OSC or LFINTOSC, the module will continue to display the current contents of the LCDDATA registers. While in Sleep, the LCD data cannot be changed. If the LCDIE bit is set, the device will wake from Sleep on the next LCD frame boundary. The LCD module current consumption will not decrease in this mode; however, the overall device power consumption will be lower due to the shutdown of the CPU and other peripherals. Table 27-8 shows the status of the LCD module during a Sleep while using each of the three available clock sources.

Note:	When the LCDEN bit is cleared, the LCD
	module will be disabled at the completion
	of frame. At this time, the port pins will
	revert to digital functionality. To minimize
	power consumption due to floating digital
	inputs, the LCD pins should be driven low
	using the PORT and TRIS registers.

If a SLEEP instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATA registers. To allow the module to continue operation while in Sleep, the clock source must be either the LFINTOSC or T1OSC external oscillator. While in Sleep, the LCD data cannot be changed. The LCD module current consumption will not decrease in this mode; however, the overall consumption of the device will be lower due to shut down of the core and other peripheral functions.

Table 27-8 below shows the status of the LCD module during Sleep, using each of the three available clock sources.

TABLE 27-8: LCD MODULE STATUS DURING SLEEP

Clock Source	SLPEN	Operational During Sleep
T1080	0	Yes
11030	1	No
	0	Yes
LFINTOSC	1	No
Eccc/4	0	No
FUSC/4	1	No

Note:	The LFINTOSC or external T1OS	T10SC					
	oscillator must be used to operate th	е					
	LCD module during Sleep.						

If LCD interrupts are being generated (Type-B waveform with a multiplex mode not static) and LCDIE = 1, the device will awaken from Sleep on the next frame boundary.

Mnemonic, Operands				14-Bit Opcode				Status	
		Description Cycles		MSb		LSb		Affected	Notes
	BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	2
ADDWFC	f, d	Add with Carry W and f	1	11	1101	dfff	ffff	C, DC, Z	2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	2
ASRF	f, d	Arithmetic Right Shift	1	11	0111	dfff	ffff	C, Z	2
LSLF	f, d	Logical Left Shift	1	11	0101	dfff	ffff	C, Z	2
LSRF	f, d	Logical Right Shift	1	11	0110	dfff	ffff	C, Z	2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	_	Clear W	1	00	0001	0000	00xx	Z	
COMF	f. d	Complement f	1	00	1001	dfff	ffff	z	2
DECF	f. d	Decrement f	1	00	0011	dfff	ffff	z	2
INCF	f. d	Increment f	1	0.0	1010	dfff	ffff	z	2
IORWE	f. d	Inclusive OR W with f	1	0.0	0100	dfff	ffff	z	2
MOVE	f. d	Move f	1	0.0	1000	dfff	ffff	z	2
MOVWE	f	Move W to f	1	0.0	0000	1fff	ffff	_	2
RIF	fd	Rotate Left f through Carry	1	0.0	1101	dfff	ffff	C	2
RRF	f d	Rotate Right f through Carry	1	00	1100	dfff	ffff	c	2
SUBWE	f d	Subtract W from f	1	00	0010	dfff	ffff		2
SUBWEB	f d	Subtract with Borrow W from f	1	11	1011	dfff	ffff	C DC Z	2
SWAPE	f d	Swap nibbles in f	1	00	1110	dfff	ffff	0, 00, 2	2
XORWE	f d	Exclusive OR W with f	1	00	0110	dfff	ffff	7	2
	., a	BYTE ORIENTED SKIP) PFRATIO	ONS	0110	4111		-	
550507	fd	Decrement f. Skin if 0	1(2)		1011	aff.	<i>f f f f f f f f f f </i>		1 2
DECFSZ	f d	Increment f. Skip if 0	1(2)	00	1111	dfff	LLLL FFFF		1, 2
INCF52	1, U		1(2)	00		ulli			1, 2
		BIT-ORIENTED FILE REGIST	ER OPER	ATION	IS	1			
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		2
		BIT-ORIENTED SKIP O	PERATIO	NS					
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		1, 2
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		1, 2
LITERAL (OPERATIO	NS							
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	k	Move literal to BSR	1	00	0000	001k	kkkk		
MOVLP	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk		
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

TABLE 29-3: PIC16(L)F1946/47 INSTRUCTION SET

Note 1:If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

RETFIE	Return from Interrupt
Syntax:	[label] RETFIE
Operands:	None
Operation:	$\begin{array}{l} TOS \to PC, \\ 1 \to GIE \end{array}$
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words:	1
Cycles:	2
Example:	RETFIE
	After Interrupt PC = TOS GIE = 1

RETURN	Return from Subroutine			
Syntax:	[label] RETURN			
Operands:	None			
Operation:	$TOS \rightarrow PC$			
Status Affected:	None			
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.			

RETLW	Return with literal in W	DIE	Pototo Loft f through Corry			
Syntax:	[<i>label</i>] RETLW k		Rotate Left I through Carry			
Operands:	$0 \le k \le 255$	Syntax:	[<i>label</i>] RLF f,d			
Operation:	$k \rightarrow (W);$ TOS $\rightarrow PC$	Operands:	$0 \le f \le 127$ $d \in [0,1]$			
Status Affected	None	Operation:	See description below			
Description:	The W register is leaded with the 8 bit	Status Affected:	С			
Description: The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.		Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is			
Words:	1		stored back in register T.			
Cycles:	2					
Example:	CALL TABLE;W contains table	Words:	1			
	<pre>;offset value . ;W now has table value</pre>	Cycles:	1			
TABLE	•	Example:	RLF REG1,0			
	• ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • RETLW kn ; End of table		Before Instruction REG1 = 1110 0110 C = 0 After Instruction REG1 = 1110 0110 W = 1100 1100 C = 1			
	Before Instruction W = 0x07 After Instruction W = value of k8					









Param No.	Symbol	Characteristic		Min.	Тур†	Max.	Units	Conditions
SP70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK \downarrow or SCK \uparrow input		2.25 TCY		—	ns	
SP71*	TscH	SCK input high time (Slave mode)		Tcy + 20		—	ns	
SP72*	TscL	SCK input low time (Slave mode	e)	Tcy + 20		—	ns	
SP73*	TDIV2scH, TDIV2scL	Setup time of SDI data input to S	SCK edge	100		_	ns	
SP74*	TscH2dlL, TscL2dlL	Hold time of SDI data input to SO	CK edge	100		_	ns	
SP75*	TDOR	SDO data output rise time	3.0-5.5V	—	10	25	ns	
			1.8-5.5V	—	25	50	ns	
SP76*	TDOF	SDO data output fall time		—	10	25	ns	
SP77*	TssH2doZ	SS↑ to SDO output high-impedance		10	—	50	ns	
SP78*	TscR	SCK output rise time	3.0-5.5V	—	10	25	ns	
		(Master mode)	1.8-5.5V	—	25	50	ns	
SP79*	TscF	SCK output fall time (Master mo	de)	—	10	25	ns	
SP80*	TSCH2DOV,	SDO data output valid after	3.0-5.5V	—	_	50	ns	
	TscL2doV	SCK edge	1.8-5.5V	—	—	145	ns	
SP81*	TDOV2scH	SDO data output setup to SCK edge		TCY	—	—	ns	
	, TDOV2scL							
SP82*	TssL2DoV	SDO data output valid after $\overline{\text{SS}}\downarrow$ edge			_	50	ns	
SP83*	TscH2ssH, TscL2ssH	SS ↑ after SCK edge		1.5 Tcy + 40	_	_	ns	

TABLE 30-14: SPI MODE REQUIREMENTS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 30-20: I²C BUS START/STOP BITS TIMING









FIGURE 31-6: IDD MAXIMUM, XT AND EXTRC OSCILLATOR, PIC16F1946/47 ONLY













PIC16(L)F1946/47





FIGURE 31-62: COMPARATOR HYSTERESIS, LOW-POWER MODE

