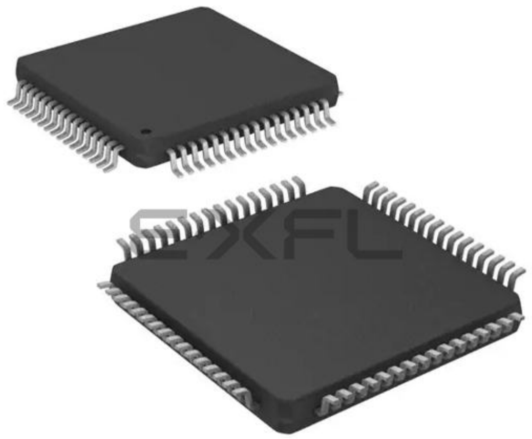

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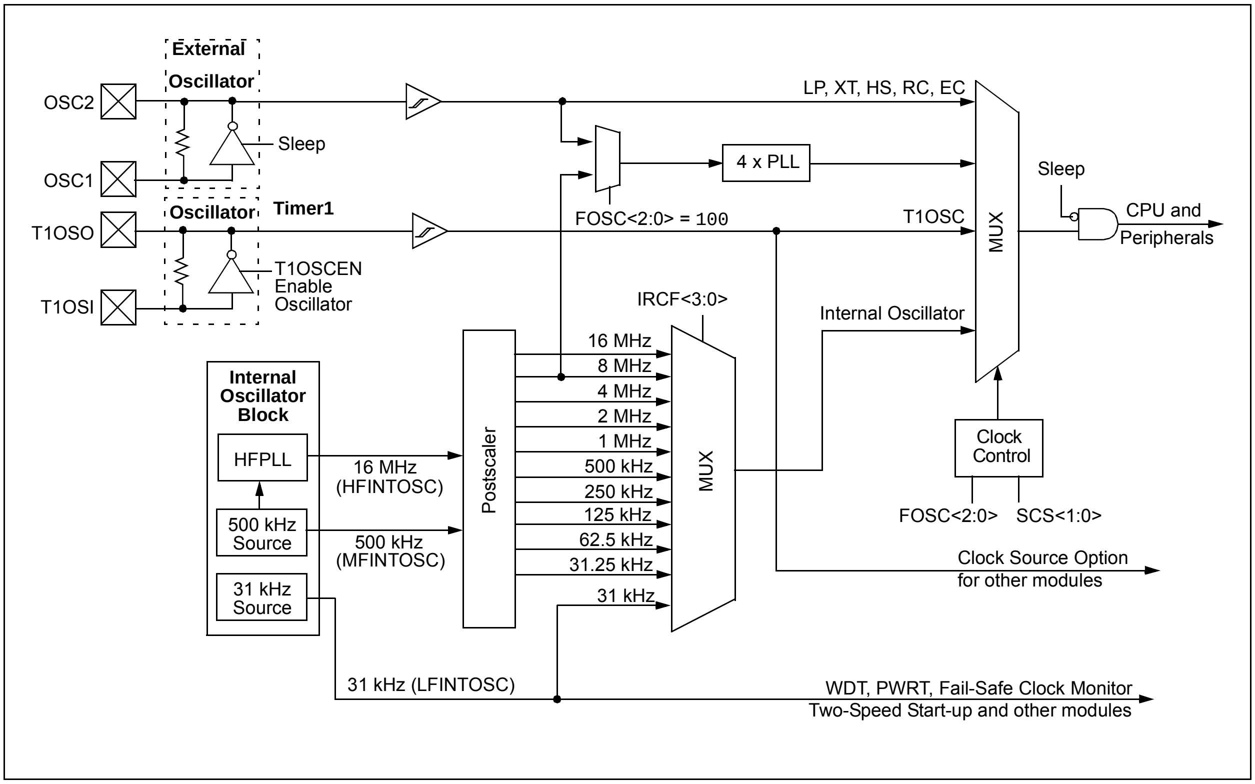
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1947t-i-pt

FIGURE 5-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



6.12 Power Control (PCON) Register

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset ($\overline{\text{POR}}$)
- Brown-out Reset ($\overline{\text{BOR}}$)
- Reset Instruction Reset ($\overline{\text{RI}}$)
- Stack Overflow Reset (STKOVF)
- Stack Underflow Reset (STKUNF)
- $\overline{\text{MCLR}}$ Reset ($\overline{\text{RMCLR}}$)

The PCON register bits are shown in Register 6-2.

6.13 Register Definitions: Power Control

REGISTER 6-2: PCON: POWER CONTROL REGISTER

R/W/HS-0/q	R/W/HS-0/q	U-0	U-0	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	—	—	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-m/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **STKOVF:** Stack Overflow Flag bit
1 = A Stack Overflow occurred
0 = A Stack Overflow has not occurred or set to ‘0’ by firmware

bit 6 **STKUNF:** Stack Underflow Flag bit
1 = A Stack Underflow occurred
0 = A Stack Underflow has not occurred or set to ‘0’ by firmware

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3 **$\overline{\text{RMCLR}}$:** $\overline{\text{MCLR}}$ Reset Flag bit
1 = A $\overline{\text{MCLR}}$ Reset has not occurred or set to ‘1’ by firmware
0 = A $\overline{\text{MCLR}}$ Reset has occurred (set to ‘0’ in hardware when a $\overline{\text{MCLR}}$ Reset occurs)

bit 2 **$\overline{\text{RI}}$:** RESET Instruction Flag bit
1 = A RESET instruction has not been executed or set to ‘1’ by firmware
0 = A RESET instruction has been executed (set to ‘0’ in hardware upon executing a RESET instruction)

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

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EXAMPLE 11-4: ERASING ONE ROW OF PROGRAM MEMORY -

```
; This row erase routine assumes the following:
; 1. A valid address within the erase block is loaded in ADDRH:ADDRL
; 2. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)


        BCF         INTCON,GIE      ; Disable ints so required sequences will execute properly
        BANKSEL     EEADRL
        MOVF        ADDRL,W         ; Load lower 8 bits of erase address boundary
        MOVWF       EEADRL
        MOVF        ADDRH,W         ; Load upper 6 bits of erase address boundary
        MOVWF       EEADRH
        BSF         EECON1,EEPGD    ; Point to program memory
        BCF         EECON1,CFGS     ; Not configuration space
        BSF         EECON1,FREE     ; Specify an erase operation
        BSF         EECON1,WREN     ; Enable writes

Required Sequence
        MOVLW       55h             ; Start of required sequence to initiate erase
        MOVWF       EECON2          ; Write 55h
        MOVLW       0AAh            ;
        MOVWF       EECON2          ; Write AAh
        BSF         EECON1,WR       ; Set WR bit to begin erase
        NOP                         ; Any instructions here are ignored as processor
                                    ; halts to begin erase sequence
        NOP                         ; Processor will stop here and wait for erase complete.

                                    ; after erase processor continues with 3rd instruction

        BCF         EECON1,WREN     ; Disable writes
        BSF         INTCON,GIE      ; Enable interrupts
```

12.5 PORTB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 12-7). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 12-1 shows how to initialize an I/O port.

Reading the PORTB register (Register 12-6) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATB).

The TRISB register (Register 12-7) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read ‘0’.

12.5.1 WEAK PULL-UPS

Each of the PORTB pins has an individually configurable internal weak pull-up. Control bits WPUB<7:0> enable or disable each pull-up (see Register 12-9). Each weak pull-up is automatically turned off when the port pin is configured as an output. All pull-ups are disabled on a Power-on Reset by the $\overline{\text{WPUEN}}$ bit of the OPTION_REG register.

12.5.2 INTERRUPT-ON-CHANGE

All of the PORTB pins are individually configurable as an interrupt-on-change pin. Control bits IOCB<7:0> enable or disable the interrupt function for each pin. The interrupt-on-change feature is disabled on a Power-on Reset. Reference **Section 13.0 “Interrupt-On-Change”** for more information.

12.5.3 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 12-5.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions, such as the EUSART RX signal, override other port functions and are included in the priority list.

TABLE 12-5: PORTB OUTPUT PRIORITY

Pin Name	Function Priority[1]
RB0	SEG30 (LED) SRI (SR Latch) RB0
RB1	SEG8 (LCD) RB1
RB2	SEG9 (LCD) RB2
RB3	SEG10 (LCD) RB3
RB4	SEG11 (LCD) RB4
RB5	SEG29 (LCD) RB5
RB6	ICSPCLK (Programming) ICDCLK (enabled by Configuration Word) SEG38 (LCD) RB6
RB7	ICSPDAT (Programming) ICDDAT (enabled by Configuration Word) SEG39 (LCD) RB7

Note 1: Priority listed from highest to lowest.

12.15 PORTG Registers

PORTG is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISG (Register 12-25). Setting a TRISG bit (= 1) will make the corresponding PORTG pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISG bit (= 0) will make the corresponding PORTG pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). The exception is RG5, which is input only and its TRIS bit will always read as '1'. Example 12-1 shows how to initialize an I/O port.

Reading the PORTG register (Register 12-24) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATG). RG5 reads '0' when MCLRE = 1.

The TRISG register (Register 12-25) controls the PORTG pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISG register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

12.15.1 ANSELG REGISTER

The ANSELG register (Register 12-27) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELG bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELG bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELG register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

12.15.2 PORTG FUNCTIONS AND OUTPUT PRIORITIES

Each PORTG pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 12-16.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

TABLE 12-16: PORTG OUTPUT PRIORITY

Pin Name	Function Priority(1)
RG0	CCP3 (CCP) P3A (CCP) SEG42 (LCD) RG0
RG1	TX2 (EUSART) CK2 (EUSART) C3OUT (Comparator) SEG43 (LCD) RG1
RG2	DT2 SEG44 (LCD) RG2
RG3	CCP4 (CCP) P3D (CCP) SEG45 (LCD) RG3
RG4	CCP5 (CCP) P1D (CCP) SEG26 (LCD) RG4
RG5	Input-only pin

Note 1: Priority listed from highest to lowest.

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19.0 SR LATCH

The module consists of a single SR Latch with multiple Set and Reset inputs as well as separate latch outputs. The SR Latch module includes the following features:

- Programmable input selection
- SR Latch output is available externally
- Separate Q and $\overline{Q}$ outputs
- Firmware Set and Reset

The SR Latch can be used in a variety of analog applications, including oscillator circuits, one-shot circuit, hysteretic controllers, and analog timing applications.

19.1 Latch Operation

The latch is a Set-Reset Latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. The latch can be set or reset by:

- Software control (SRPS and SRPR bits)
- Comparator C1 output (sync_C1OUT)
- Comparator C2 output (sync_C2OUT)
- SRI pin
- Programmable clock (SRCLK)

The SRPS and the SRPR bits of the SRCON0 register may be used to set or reset the SR Latch, respectively. The latch is Reset-dominant. Therefore, if both Set and Reset inputs are high, the latch will go to the Reset state. Both the SRPS and SRPR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

The output from Comparator C1 or C2 can be used as the Set or Reset inputs of the SR Latch. The output of either comparator can be synchronized to the Timer1 clock source. See **Section 18.0 “Comparator Module”** and **Section 21.0 “Timer1 Module with Gate Control”** for more information.

An external source on the SRI pin can be used as the Set or Reset inputs of the SR Latch.

An internal clock source is available that can periodically set or reset the SR Latch. The SRCLK<2:0> bits in the SRCON0 register are used to select the clock source period. The SRSCKE and SRRCKE bits of the SRCON1 register enable the clock source to set or reset the SR Latch, respectively.

19.2 Latch Output

The SRQEN and SRNQEN bits of the SRCON0 register control the Q and $\overline{Q}$ latch outputs. Both of the SR Latch outputs may be directly output to an I/O pin at the same time.

The applicable TRIS bit of the corresponding port must be cleared to enable the port pin output driver.

19.3 Effects of a Reset

Upon any device Reset, the SR Latch output is not initialized to a known state. The user’s firmware is responsible for initializing the latch output before enabling the output pins.

REGISTER 19-3: SRCON1: SR LATCH CONTROL 1 REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **SRSPE:** SR Latch Peripheral Set Enable bit
1 = SR Latch is set when the SRI pin is high
0 = SRI pin has no effect on the set input of the SR Latch

bit 6 **SRSCKE:** SR Latch Set Clock Enable bit
1 = Set input of SR Latch is pulsed with SRCLK
0 = SRCLK has no effect on the set input of the SR Latch

bit 5 **SRSC2E:** SR Latch C2 Set Enable bit
1 = SR Latch is set when the C2 Comparator output is high
0 = C2 Comparator output has no effect on the set input of the SR Latch

bit 4 **SRSC1E:** SR Latch C1 Set Enable bit
1 = SR Latch is set when the C1 Comparator output is high
0 = C1 Comparator output has no effect on the set input of the SR Latch

bit 3 **SRRPE:** SR Latch Peripheral Reset Enable bit
1 = SR Latch is reset when the SRI pin is high
0 = SRI pin has no effect on the Reset input of the SR Latch

bit 2 **SRRCKE:** SR Latch Reset Clock Enable bit
1 = Reset input of SR Latch is pulsed with SRCLK
0 = SRCLK has no effect on the Reset input of the SR Latch

bit 1 **SRRC2E:** SR Latch C2 Reset Enable bit
1 = SR Latch is reset when the C2 Comparator output is high
0 = C2 Comparator output has no effect on the Reset input of the SR Latch

bit 0 **SRRC1E:** SR Latch C1 Reset Enable bit
1 = SR Latch is reset when the C1 Comparator output is high
0 = C1 Comparator output has no effect on the Reset input of the SR Latch

TABLE 19-2: SUMMARY OF REGISTERS ASSOCIATED WITH SR LATCH MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELF	ANSELF7	ANSELF6	ANSELF5	ANSELF4	ANSELF3	ANSELF2	ANSELF1	ANSELF0	126
SRCON0	SRLEN	SRCLK<2:0>			SRQEN	SRNQEN	SRPS	SRPR	184
SRCON1	SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E	185
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	125
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	125

Legend: — = unimplemented location, read as ‘0’. Shaded cells are unused by the SR Latch module.

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23.4.8 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a reset, see **Section 12.1 "Alternate Pin Function"** for more information.

TABLE 23-10: SUMMARY OF REGISTERS ASSOCIATED WITH ENHANCED PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON	P3CSEL	P3BSEL	P2DSEL	P2CSEL	P2BSEL	CCP2SEL	P1CSEL	P1BSEL	123
CCPxCON	PxM<1:0>(1)		DCxB<1:0>		CCPxM<3:0>				227
CCPxAS	CCPxASE	CCPxAS<2:0>			PSSxAC<1:0>		PSSxBD<1:0>		229
CCPTMRS0	C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		228
CCPTMRS1	—	—	—	—	—	—	C5TSEL<1:0>		228
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	90
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	91
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	LCDIE	C3IE	CCP2IE	92
PIE3	—	CCP5IE	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—	93
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	95
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	LCDIF	C3IF	CCP2IF	96
PIR3	—	CCP5IF	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—	97
PR2	Timer2 Period Register								200*
PR4	Timer4 Period Register								200*
PR6	Timer6 Period Register								200*
PSTRxCON	—	—	—	STRx-SYNC	STRxD	STRxC	STRxB	STRxA	231
PWMxCON	PxRSEN	PxDC<6:0>							230
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<:0>1		202
T4CON	—	T4OUTPS<3:0>				TMR4ON	T4CKPS<:0>1		202
T6CON	—	T6OUTPS<3:0>				TMR6ON	T6CKPS<:0>1		202
TMR2	Timer2 Module Register								200*
TMR4	Timer4 Module Register								200*
TMR6	Timer6 Module Register								200*
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	128
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	131
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	134
TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	137
TRISG	TRISG7	TRISG6	TRISG5	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	143

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the PWM.
Note 1: Applies to ECCP modules only.
* Page provides register information.

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23.5 Register Definitions: ECCP Control

REGISTER 23-1: CCPxCON: CCPx CONTROL REGISTER

R/W-00	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PxM<1:0>(1)		DCxB<1:0>		CCPxM<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **PxM<1:0>:** Enhanced PWM Output Configuration bits(1)

Capture mode:
Unused

Compare mode:
Unused

If CCPxM<3:2> = `00`, `01`, `10`:
`xx` = PxA assigned as Capture/Compare input; PxB, PxC, PxD assigned as port pins

If CCPxM<3:2> = `11`:
`11` = Full-Bridge output reverse; PxB modulated; PxC active; PxA, PxD inactive
`10` = Half-Bridge output; PxA, PxB modulated with dead-band control; PxC, PxD assigned as port pins
`01` = Full-Bridge output forward; PxD modulated; PxA active; PxB, PxC inactive
`00` = Single output; PxA modulated; PxB, PxC, PxD assigned as port pins

bit 5-4 **DCxB<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0 **CCPxM<3:0>:** ECCPx Mode Select bits

`1011` = Compare mode: Special Event Trigger (ECCPx resets Timer, sets CCPxIF bit, starts A/D conversion if A/D module is enabled)(2)
`1010` = Compare mode: generate software interrupt only; ECCPx pin reverts to I/O state
`1001` = Compare mode: initialize ECCPx pin high; clear output on compare match (set CCPxIF)
`1000` = Compare mode: initialize ECCPx pin low; set output on compare match (set CCPxIF)

`0111` = Capture mode: every 16th rising edge
`0110` = Capture mode: every 4th rising edge
`0101` = Capture mode: every rising edge
`0100` = Capture mode: every falling edge

`0011` = Reserved
`0010` = Compare mode: toggle output on match
`0001` = Reserved
`0000` = Capture/Compare/PWM off (resets ECCPx module)

CCP4/CCP5 only:
`11xx` = PWM mode

ECCP1/ECCP2/ECCP3 only:
`1111` = PWM mode: PxA, PxC active-low; PxB, PxD active-low
`1110` = PWM mode: PxA, PxC active-low; PxB, PxD active-high
`1101` = PWM mode: PxA, PxC active-high; PxB, PxD active-low
`1100` = PWM mode: PxA, PxC active-high; PxB, PxD active-high

Note 1: These bits are not implemented on CCP<5:4>.
2: A/D conversion start applies to CCP5 only.

FIGURE 24-14: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)

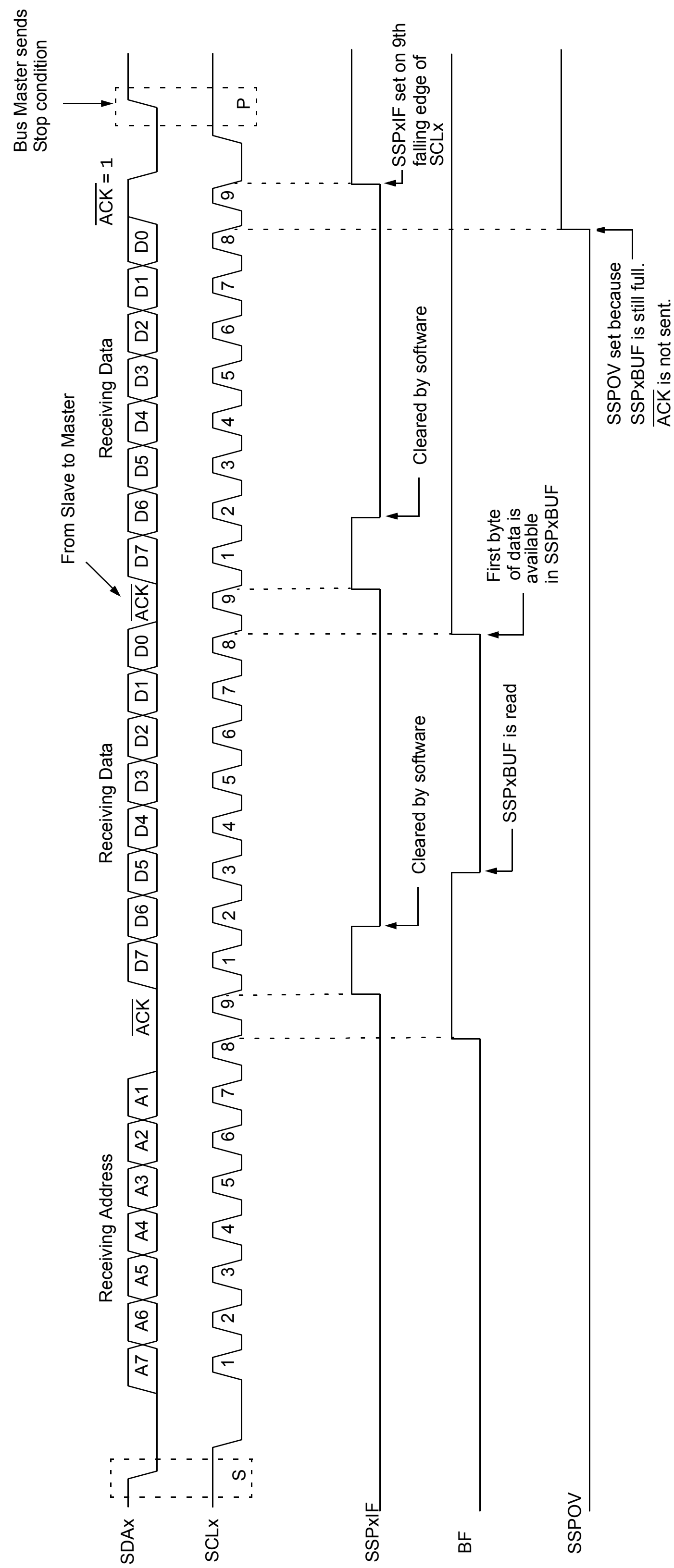

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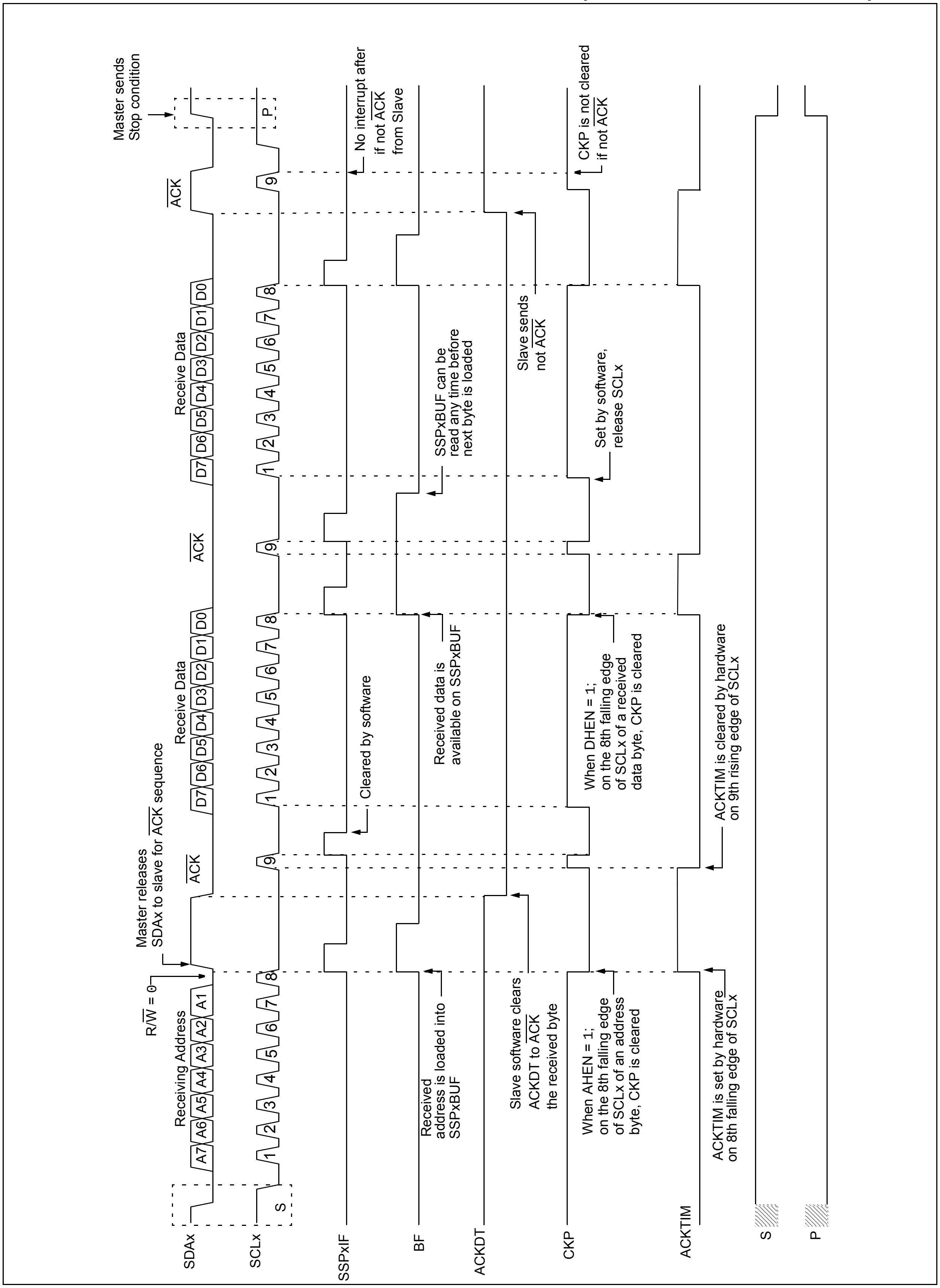
FIGURE 24-17: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)



24.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDAx or SCLx are sampled low at the beginning of the Start condition (Figure 24-32).
b) SCLx is sampled low before SDAx is asserted low (Figure 24-33).

During a Start condition, both the SDAx and the SCLx pins are monitored.

If the SDAx pin is already low, or the SCLx pin is already low, then all of the following occur:

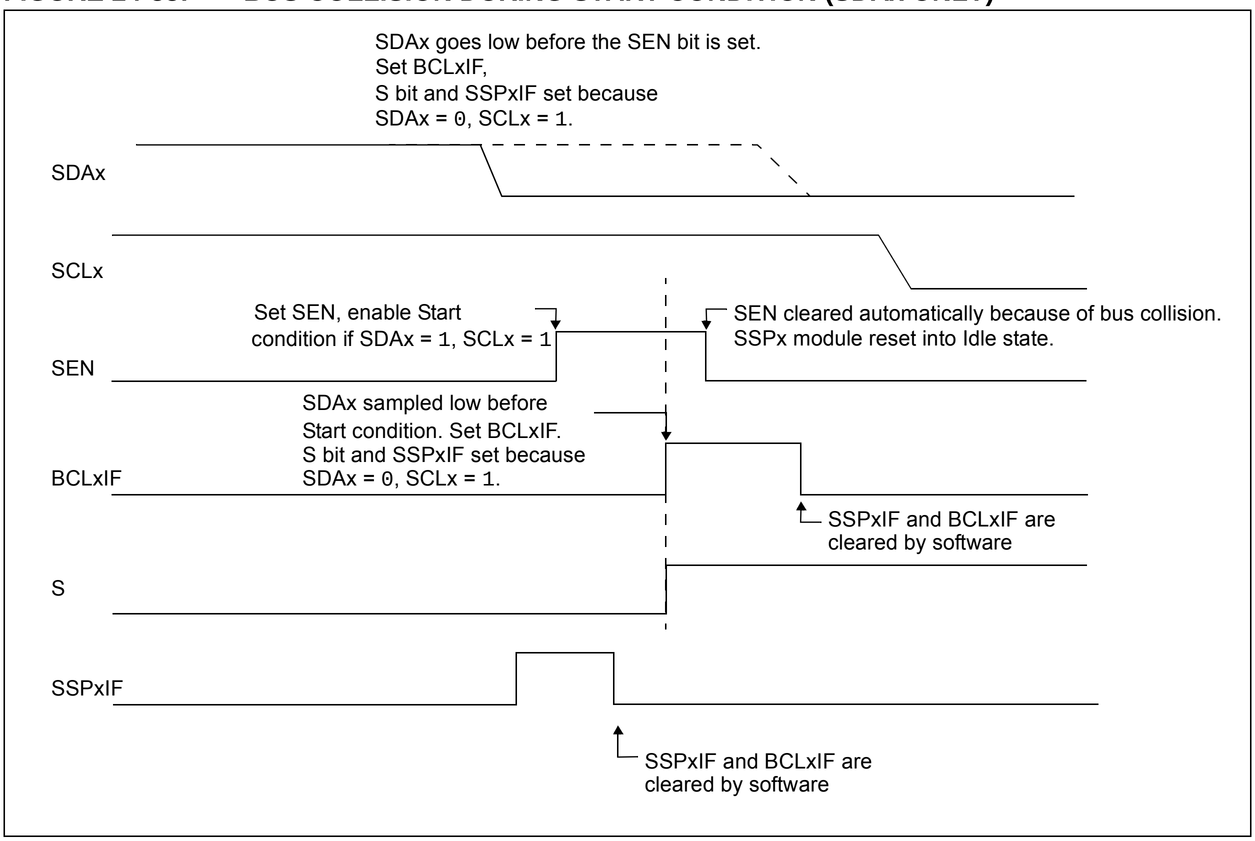
- the Start condition is aborted
- the BCLxIF flag is set and
- the MSSPx module is reset to its Idle state (Figure 24-32).

The Start condition begins with the SDAx and SCLx pins deasserted. When the SDAx pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCLx pin is sampled low while SDAx is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDAx pin is sampled low during this count, the BRG is reset and the SDAx line is asserted early (Figure 24-34). If, however, a '1' is sampled on the SDAx pin, the SDAx pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCLx pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCLx pin is asserted low.

Note:	The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDAx before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 24-33: BUS COLLISION DURING START CONDITION (SDAx ONLY)



24.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDAx when SCLx goes from low level to high level.
b) SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user releases SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled.

If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 24-35). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 24-36.

If, at the end of the BRG timeout, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

FIGURE 24-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

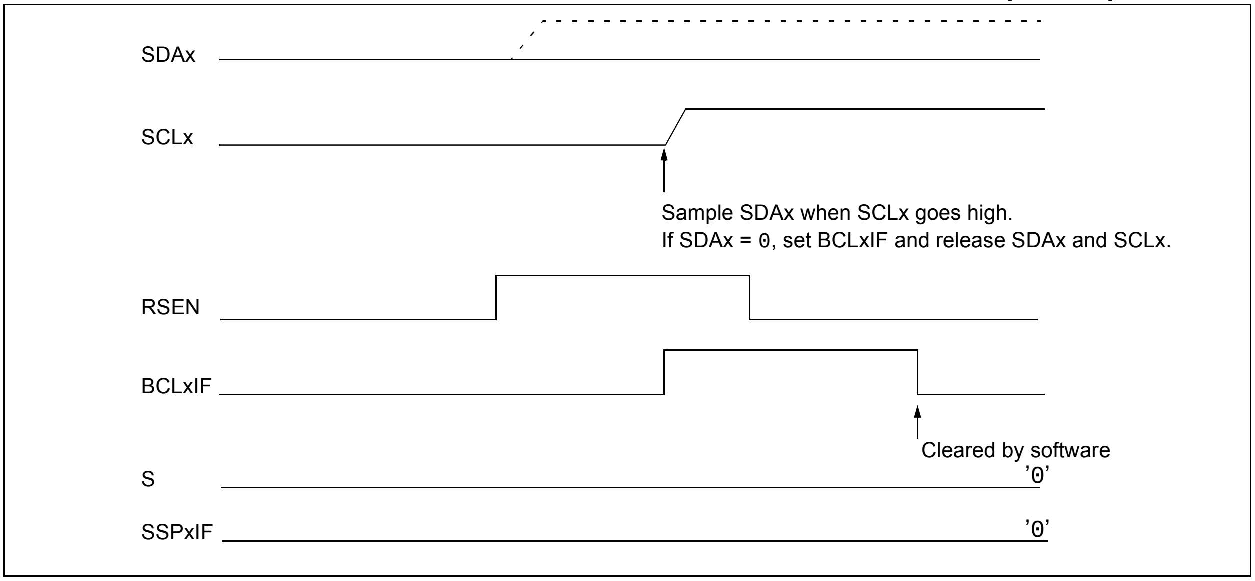


FIGURE 24-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

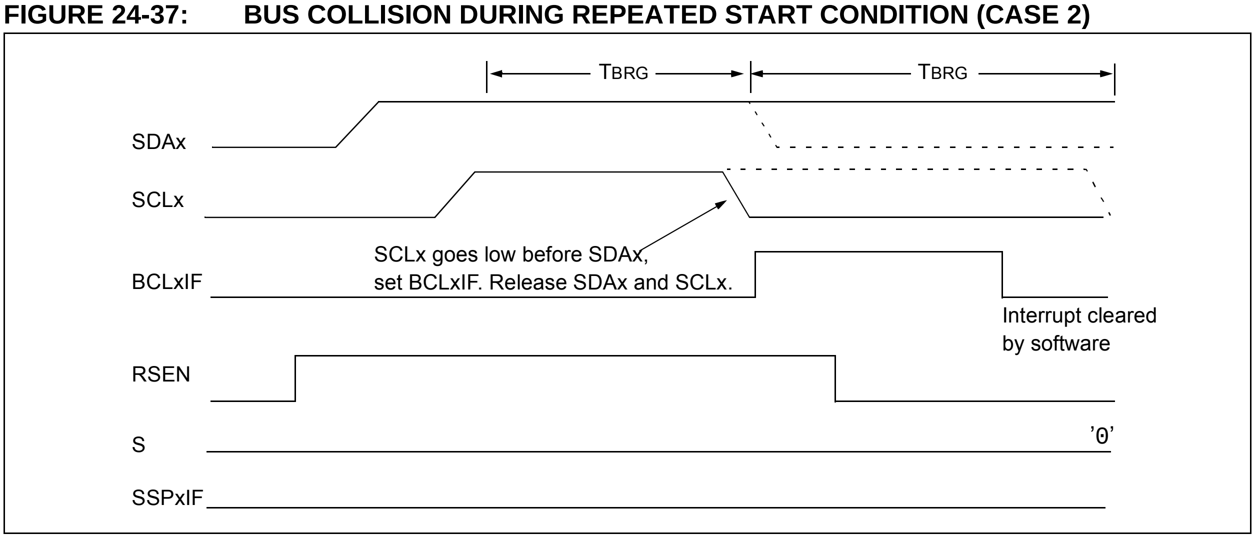


TABLE 25-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	FOSC = 8.000 MHz			FOSC = 4.000 MHz			FOSC = 3.6864 MHz			FOSC = 1.000 MHz		
	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	—
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	—	—	—
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	—
115.2k	—	—	—	—	—	—	115.2k	0.00	1	—	—	—

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	FOSC = 32.000 MHz			FOSC = 18.432 MHz			FOSC = 16.000 MHz			FOSC = 11.0592 MHz		
	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)
300	300	0.00	26666	300.0	0.00	15359	300.0	0.00	13332	300.0	0.00	9215
1200	1200	0.00	6666	1200	0.00	3839	1200.1	0.01	3332	1200	0.00	2303
2400	2400	0.01	3332	2400	0.00	1919	2399.5	-0.02	1666	2400	0.00	1151
9600	9604	0.04	832	9600	0.00	479	9592	-0.08	416	9600	0.00	287
10417	10417	0.00	767	10425	0.08	441	10417	0.00	383	10433	0.16	264
19.2k	19.18k	-0.08	416	19.20k	0.00	239	19.23k	0.16	207	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.60k	0.00	79	57.97k	0.64	68	57.60k	0.00	47
115.2k	115.9	0.64	68	115.2k	0.00	39	114.29k	-0.79	34	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	FOSC = 8.000 MHz			FOSC = 4.000 MHz			FOSC = 3.6864 MHz			FOSC = 1.000 MHz		
	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)	Actual Rate	% Error	SPxBRGH:SPxBRGL (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0.00	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—

25.4.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDxCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPxBRGH:SPxBRGL register pair. After the ABDOVF bit has been set, the counter continues to count until the fifth rising edge is detected on the RXx/DTx pin. Upon detecting the fifth RXx/DTx edge, the hardware will set the RCxIF interrupt flag and clear the ABDEN bit of the BAUDxCON register. The RCxIF flag can be subsequently cleared by reading the RCxREG. The ABDOVF flag can be cleared by software directly.

To terminate the auto-baud process before the RCxIF flag is set, clear the ABDEN bit then clear the ABDOVF bit. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

25.4.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RXx/DTx line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDxCON register. Once set, the normal receive sequence on RXx/DTx is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RXx/DTx line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCxIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 25-7), and asynchronously if the device is in Sleep mode (Figure 25-8). The interrupt condition is cleared by reading the RCxREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RXx line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

25.4.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be ten or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Startup Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

WUE Bit

The wake-up event causes a receive interrupt by setting the RCxIF bit. The WUE bit is cleared by hardware by a rising edge on RXx/DTx. The interrupt condition is then cleared by software by reading the RCxREG register and discarding its contents.

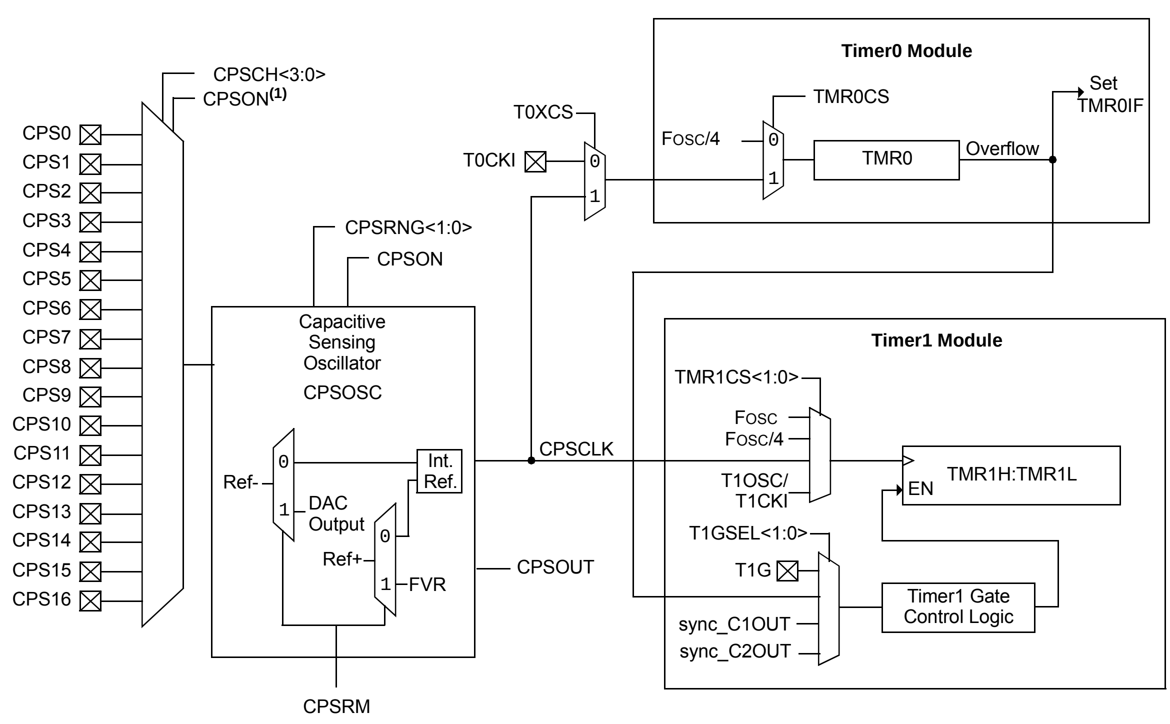
To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

26.0 CAPACITIVE SENSING (CPS) MODULE

The Capacitive Sensing (CPS) module allows for an interaction with an end user without a mechanical interface. In a typical application, the CPS module is attached to a pad on a Printed Circuit Board (PCB), which is electrically isolated from the end user. When the end user places their finger over the PCB pad, a capacitive load is added, causing a frequency shift in the CPS module. The CPS module requires software and at least one timer resource to determine the change in frequency. Key features of this module include:

- Analog MUX for monitoring multiple inputs
- Capacitive sensing oscillator
- Multiple power modes
- Multiple current ranges
- Multiple voltage reference modes
- Software control
- Operation during Sleep

FIGURE 26-1: CAPACITIVE SENSING BLOCK DIAGRAM



Note 1: If CPSON = 0, disabling capacitive sensing, no channel is selected.

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26.4 Register Definitions: Capacitive Sensing Control

REGISTER 26-2: CPSCON0: CAPACITIVE SENSING CONTROL REGISTER 0

R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R-0/0	R/W-0/0
CPSON	CPSRM	—	—	CPSRNG<1:0>		CPSOUT	T0XCS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **CPSON:** CPS Module Enable bit
1 = CPS module is enabled
0 = CPS module is disabled

bit 6 **CPSRM:** Capacitive Sensing Reference Mode bit
1 = CPS module is in high range. DAC and FVR provide oscillator voltage references.
0 = CPS module is in the low range. Internal oscillator voltage references are used.

bit 5-4 **Unimplemented:** Read as ‘0’

bit 3-2 **CPSRNG<1:0>:** Capacitive Sensing Current Range bits
If CPSRM = 0 (low range):
11 = Oscillator is in High Range. Charge/Discharge Current is nominally 18 µA
10 = Oscillator is in Medium Range. Charge/Discharge Current is nominally 1.2 µA
01 = Oscillator is in Low Range. Charge/Discharge Current is nominally 0.1 µA
00 = Oscillator is off

If CPSRM = 1 (high range):
11 = Oscillator is in High Range. Charge/Discharge Current is nominally 100 µA
10 = Oscillator is in Medium Range. Charge/Discharge Current is nominally 30 µA
01 = Oscillator is in Low Range. Charge/Discharge Current is nominally 9 µA
00 = Oscillator is on. Noise Detection mode. No Charge/Discharge current is supplied.

bit 1 **CPSOUT:** Capacitive Sensing Oscillator Status bit
1 = Oscillator is sourcing current (Current flowing out of the pin)
0 = Oscillator is sinking current (Current flowing into the pin)

bit 0 **T0XCS:** Timer0 External Clock Source Select bit
If TMR0CS = 1:
The T0XCS bit controls which clock external to the core/Timer0 module supplies Timer0:
1 = Timer0 clock source is the capacitive sensing oscillator
0 = Timer0 clock source is the T0CKI pin
If TMR0CS = 0:
Timer0 clock source is controlled by the core/Timer0 module and is FOSC/4

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REGISTER 26-3: CPSCON1: CAPACITIVE SENSING CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	CPSCH<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **CPSCH<4:0>:** Capacitive Sensing Channel Select bits
If CPSON = 0:
These bits are ignored. No channel is selected.
If CPSON = 1:
00000 = channel 0, (CPS0)
00001 = channel 1, (CPS1)
00010 = channel 2, (CPS2)
00011 = channel 3, (CPS3)
00100 = channel 4, (CPS4)
00101 = channel 5, (CPS5)
00110 = channel 6, (CPS6)
00111 = channel 7, (CPS7)
01000 = channel 8, (CPS8)
01001 = channel 9, (CPS9)
01010 = channel 10, (CPS10)
01011 = channel 11, (CPS11)
01100 = channel 12, (CPS12)
01101 = channel 13, (CPS13)
01110 = channel 14, (CPS14)
01111 = channel 15, (CPS15)
10000 = channel 16, (CPS16)
10001 = Reserved. Do not use.
.
.
.
11111 = Reserved. Do not use.

TABLE 26-1: SUMMARY OF REGISTERS ASSOCIATED WITH CAPACITIVE SENSING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	126
CPSCON0	CPSON	CPSRM	—	—	CPSRNG<1:0>		CPSOUT	T0XCS	322
CPSCON1	—	—	—	CPSCH<4:0>					323
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS2	PS1	PS0	188
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	197
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	125
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	128
TRISD	TRISD<7:0>								134

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are not used by the CPS module.

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FIGURE 31-9: IDD, EC OSCILLATOR, LOW-POWER MODE, FOSC = 500 kHz, PIC16LF1946/47 ONLY

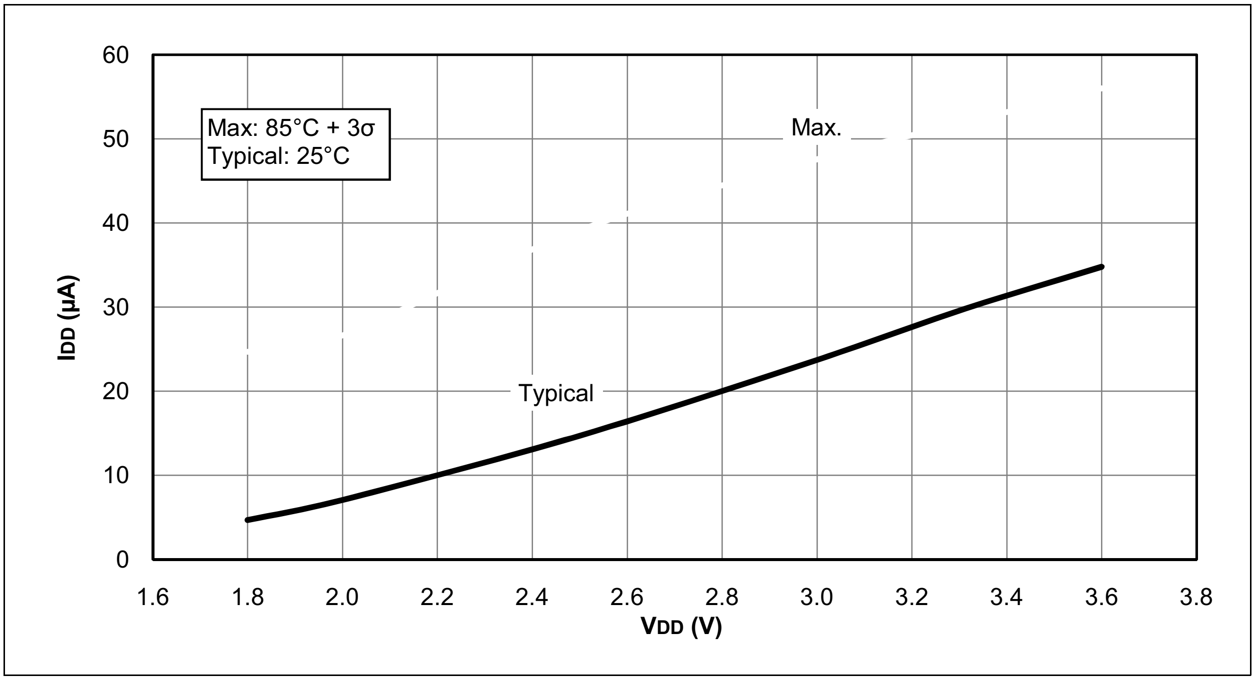

FIGURE 31-10: IDD, EC OSCILLATOR, LOW-POWER MODE, FOSC = 500 kHz, PIC16F1946/47 ONLY

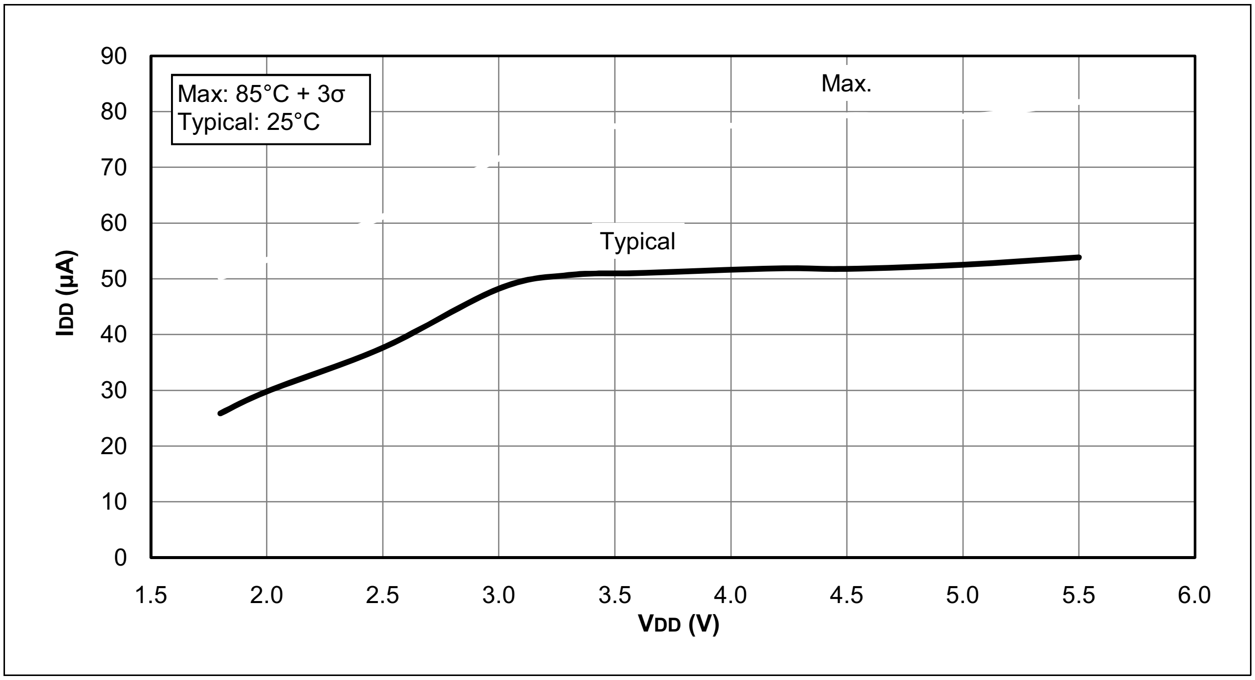

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FIGURE 31-33: IPD, WATCHDOG TIMER (WDT), PIC16LF1946/47 ONLY

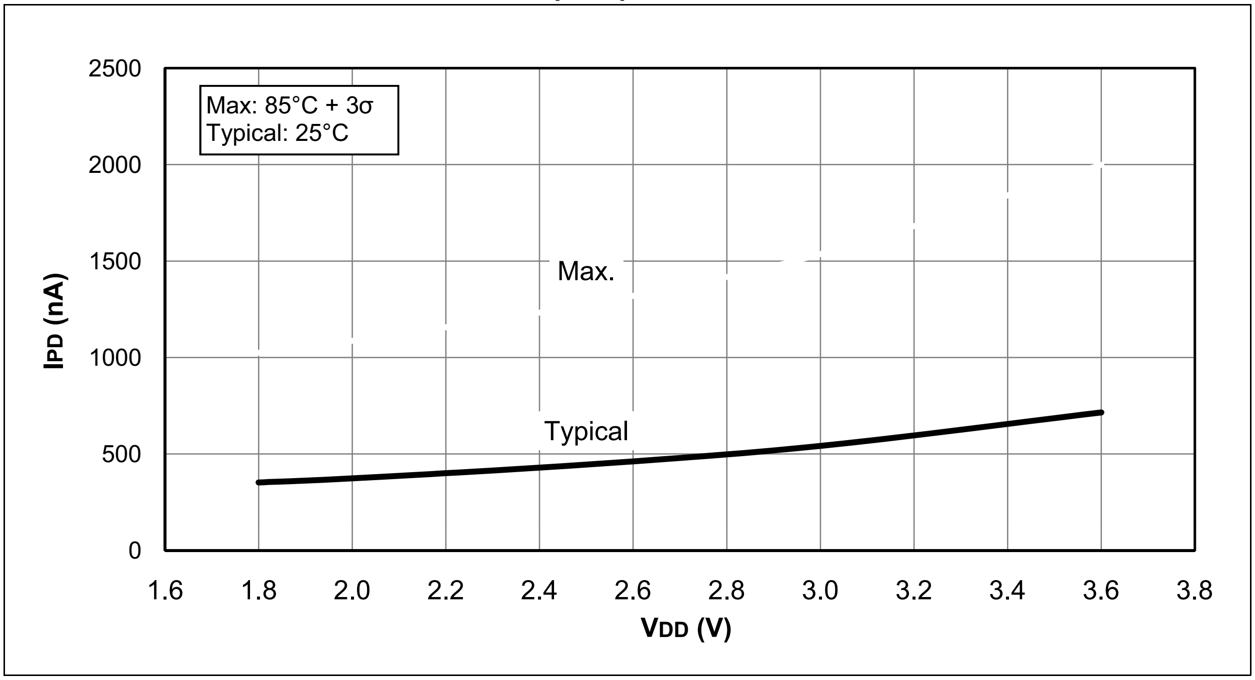
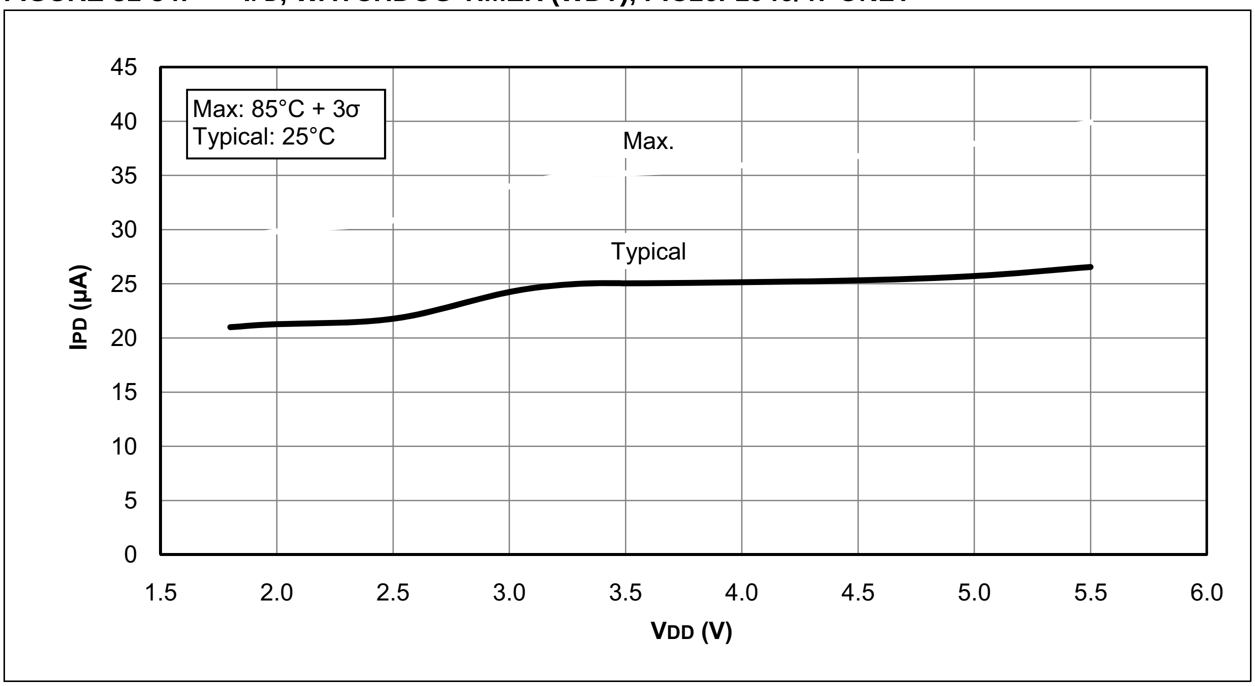


FIGURE 31-34: IPD, WATCHDOG TIMER (WDT), PIC16F1946/47 ONLY



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