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What is "<ins>Embedded - Microcontrollers</ins>"?

"<ins>Embedded - Microcontrollers</ins>" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<ins>Embedded - Microcontrollers</ins>"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f301c6t6tr

List of figures

1   Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F301x6/8 microcontrollers.

This datasheet should be read in conjunction with the STM32F301x6/8 and STM32F318x8 advanced ARM®-based 32-bit MCUs reference manual (RM0366). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M4 core, please refer to the Cortex®-M4 Technical Reference Manual, available from ARM website www.arm.com.

3   Functional overview

3.1   ARM® Cortex®-M4 core with FPU, embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single-precision FPU speeds up software development by using metalanguage development tools while avoiding saturation.

With its embedded ARM core, the STM32F301x6/8 family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F301x6/8 family devices.

3.2   Memories

3.2.1   Embedded Flash memory

All STM32F301x6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2   Embedded SRAM

STM32F301x6/8 devices feature 16 Kbytes of embedded SRAM.

3.3   Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

*   Boot from user Flash
*   Boot from system memory
*   Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10) and USART2 (PA2/PA3).

Table 4. STM32F301x6/8 peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADC1 DAC1	Conversion triggers
	DMA	Memory to memory transfer trigger
	Compx	Comparator output blanking
COMPx	TIMx	Timer input: OCREF_CLR input, input capture
ADC1	TIM1	Timer triggered by analog watchdog
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx PVD GPIO	TIM1 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADC1 DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: *For more details about the interconnect actions, please refer to the corresponding sections in the* STM32F301x6/8 and STM32F318x8 *reference manual RM0366.*

3.17 Inter-integrated circuit interfaces (I^{2}C)

The devices feature three I^{2}C bus interfaces which can operate in multimaster and slave mode. Each I2C interface can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

All I^{2}C interfaces support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	**Digital filter**
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, it provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. It also has a clock domain independent from the CPU clock, allowing the I2Cx (x=1,3) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 7* for the features available in I2C1, I2C2 and I2C3.

Table 7. STM32F301x6/8 I^{2}C implementation

I2C features[1]	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Independent clock	X	X	X
SMBus	X	X	X
Wakeup from STOP	X	X	X

1. X = supported.

Figure 7. STM32F301x6/8 WLCSP49 ballout
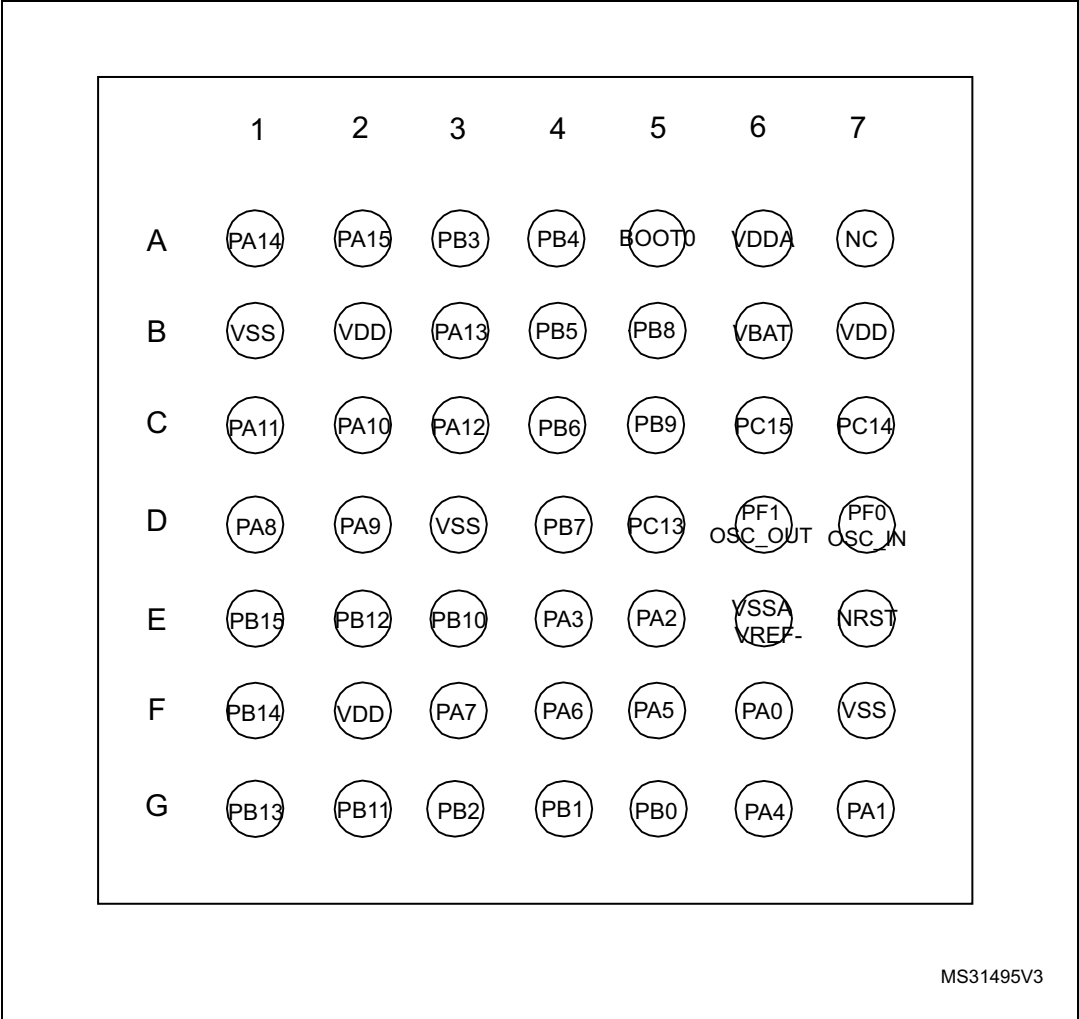
1. The above figure shows the package top view.

2. NC: Not connected.

5   Memory mapping

Figure 8. STM32F301x6/8 memory mapping

MSv30355V3
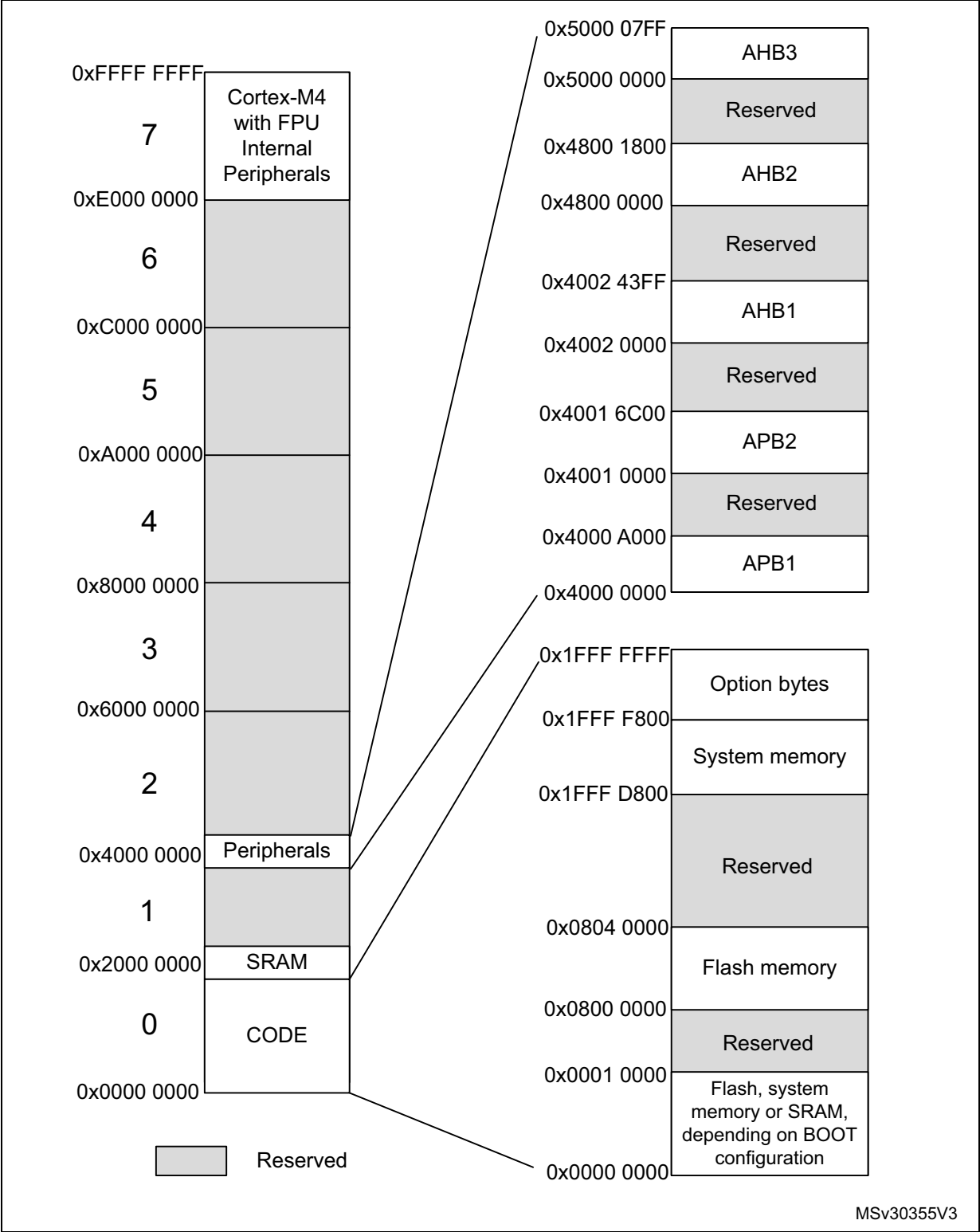
6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme
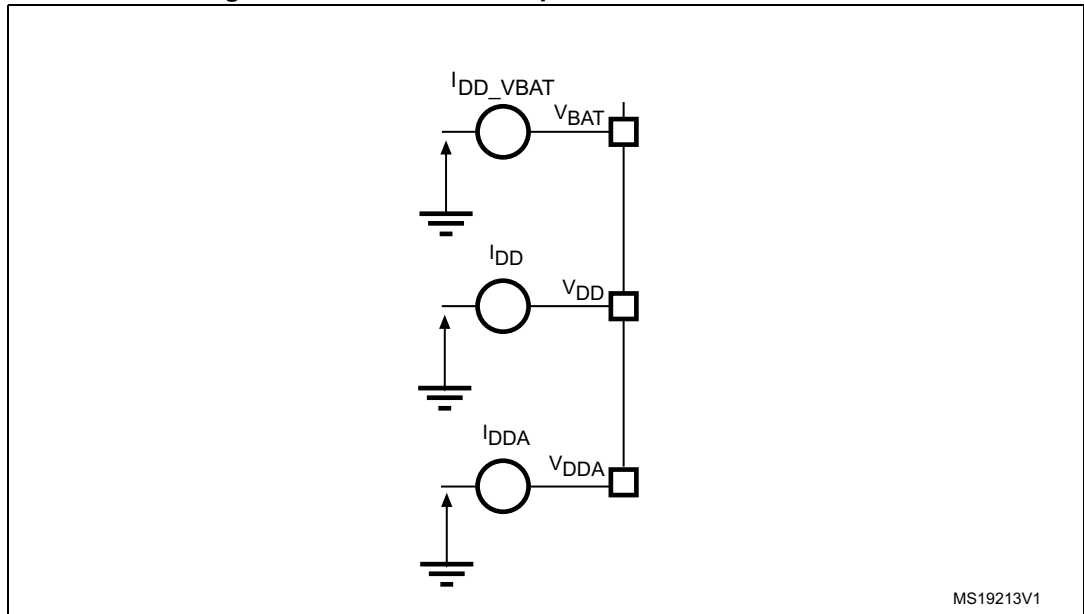
6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics*, and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 20. Voltage characteristics[1]

| Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{BAT} and V_{DD})	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for V_{DD} > V_{DDA}	-	0.4	V
V_{IN}[2]	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	V
	Input voltage on TTa and TT pins	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
	Input voltage on Boot0 pin	0	9	
$|\Delta V_{DDx}|$	Variations between different V_{DD} power pins	-	50	mV
$|V_{SSX}$ –$V_{SS}|$	Variations between all the different ground pins[3]	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		V

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
   V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
   V_{DDA} must be greater than or equal to V_{DD}.

2. V_{IN} maximum must always be respected. Refer to *Table 21: Current characteristics* for the maximum allowed injected current values.

3. Include V_{REF-} pin.

6.3.4 Embedded reference voltage

The parameters given in *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23*.

Table 27. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\ °C < T_A < +105\ °C$	1.20	1.23	1.25	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	2.2	-	-	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10[1]	mV
T_{Coeff}	Temperature coefficient	-	-	-	100 [1]	ppm/°C

1. Guaranteed by design.

Table 28. Internal reference voltage calibration values

Calibration value name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: *The total current consumption is the sum of I_{DD} and I_{DDA}.*

Table 29. Typical and maximum current consumption from VDD supply at VDD = 3.6V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A[1]			Typ	Max @ T_A[1]			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	45.8	49.1[2]	50.1	51.4[2]	25.1	27.3[2]	28.0	28.6[2]	mA
			64 MHz	40.8	43.6	44.9	46.9	22.3	24.1	25.0	25.5	
			48 MHz	30.2	32.9	33.5	34.8	17.0	18.7	19.1	19.6	
			32 MHz	20.5	23.1	24.1	25.4	11.1	12.2	13.2	13.3	
			24 MHz	15.4	17.1	18.3	19.5	8.5	9.7	10.1	10.2	
			8 MHz	5.0	5.9	6.3	6.9	3.1	3.7	4.1	4.7	
			1 MHz	0.8	1.1	1.9	2.6	0.5	0.8	1.2	1.4	
		Internal clock (HSI)	64 MHz	37.3	41.1	41.8	43.3	22.0	23.8	24.4	24.9	
			48 MHz	28.0	31.1	31.6	33.2	16.4	18.0	18.3	18.6	
			32 MHz	18.8	21.3	22.1	23.1	10.9	11.9	12.8	13.1	mA
			24 MHz	14.2	15.9	16.8	17.9	5.5	6.4	6.7	7.3	
			8 MHz	4.8	5.1	6.0	6.5	2.9	3.5	4.1	4.2	
I_{DD}	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	30.0	32.8[2]	33.1	34.1[2]	5.9	6.8[2]	6.9	7.4[2]	
			64 MHz	26.7	29.2	29.6	30.5	5.3	5.9	6.2	6.7	
			48 MHz	16.7	18.5	19.0	19.7	3.6	4.5	4.5	5.3	
			32 MHz	13.3	14.9	15.3	15.4	2.9	3.7	3.8	4.3	
			24 MHz	10.2	11.4	12.0	12.3	2.2	2.7	2.9	3.2	
			8 MHz	3.6	4.4	4.8	5.3	0.9	1.2	1.5	2.1	
			1 MHz	0.5	0.8	1.1	1.3	0.1	0.4	0.8	0.8	
		Internal clock (HSI)	64 MHz	23.2	25.3	25.6	26.2	5.0	5.7	6.1	6.2	
			48 MHz	17.5	19.2	19.4	19.9	3.9	4.7	4.8	5.3	
			32 MHz	11.7	12.9	13.2	13.3	2.6	3.4	3.6	4.2	mA
			24 MHz	8.9	10.2	10.6	10.8	1.4	2.1	2.4	2.7	
			8 MHz	3.4	4.0	4.6	5.1	0.7	1.1	1.4	1.9	

1. Guaranteed by characterization results.

2. Data based on characterization results and tested in production with code executing from RAM.

Low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$[2]	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$[2]	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 46* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23*.

Table 46. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock[1]	1[2]	-	24[2]	MHz
	PLL input clock duty cycle	40[2]	-	60[2]	%
f_{PLL_OUT}	PLL multiplier output clock	16[2]	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200[2]	µs
Jitter	Cycle-to-cycle jitter	-	-	300[2]	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

2. Guaranteed by design.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under the conditions summarized in *Table 23*. All I/Os are CMOS and TTL compliant.

Table 54. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TTa and TT I/O	-	-	$0.3\ V_{DD} + 0.07$ [1]	V
		FT and FTf I/O	-	-	$0.475\ V_{DD}$ -0.2 [1]	
		BOOT0 I/O	-	-	$0.3\ V_{DD} - 0.3$ [1]	
		All I/Os except BOOT0	-	-	$0.3\ V_{DD}$ [2]	
V_{IH}	High level input voltage	TTa and TT I/O	$0.445\ V_{DD} + 0.398$ [1]	-	-	V
		FT and FTf I/O	$0.5\ V_{DD} + 0.2$ [1]	-	-	
		BOOT0	$0.2\ V_{DD} + 0.95$ [1]	-	-	
		All I/Os except BOOT0	$0.7\ V_{DD}$ [2]	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200 [1]	-	mV
		FT and FTf I/O	-	100 [1]	-	
		BOOT0	-	300 [1]	-	
I_{lkg}	Input leakage current [3]	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O [4] $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor [5]	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor [5]	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation

2. Tested in production.

3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to *Table 53: I/O current injection susceptibility*.

4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.

5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

6.3.17 Communications interfaces

I^{2}C interface characteristics

The I2C interface meets the timings requirements of the I^{2}C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 61. I2C analog filter characteristics[1]

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50[2]	260[3]	ns

1. Guaranteed by design.

2. Spikes with widths below $t_{AF(min)}$ are filtered.

3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 63. I2S characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(WS)}$	WS valid time	Master mode	-	20	ns
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	0	-	
$t_{h(WS)}$	WS hold time	Slave mode	4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	8	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	50	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	22	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1	-	

1. Guaranteed by characterization results.

2. 256xFs maximum is 36 MHz (APB1 Maximum frequency)

Note: *Refer to RM0366 Reference Manual I2S Section for more details about the sampling frequency (Fs), fMCK, fCK, DCK values reflect only the digital peripheral behavior, source clock precision might slightly change the values DCK depends mainly on ODD bit value. Digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max (I2SDIV+ODD)/(2*I2SDIV+ODD) and Fs max supported for each mode/condition.*

7   Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 75. WLCSP49 - 49-pin, 3.417 x 3.151 mm, 0.4 mm pitch wafer level chip scale package mechanical data

| Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	3.382	3.417	3.452	0.1331	0.1345	0.1359
E	3.116	3.151	3.186	0.1227	0.1241	0.1254
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.5085	-	-	0.0200	-
G	-	0.3755	-	-	0.0148	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 37. WLCSP49 - 49-pin, 3.417 x 3.151 mm, 0.4 mm pitch wafer level chip scale package recommended footprint
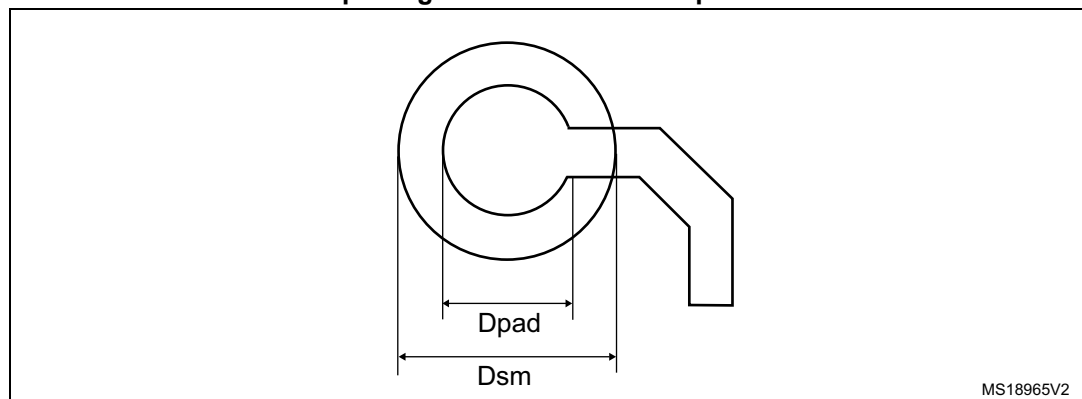
Figure 43. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint
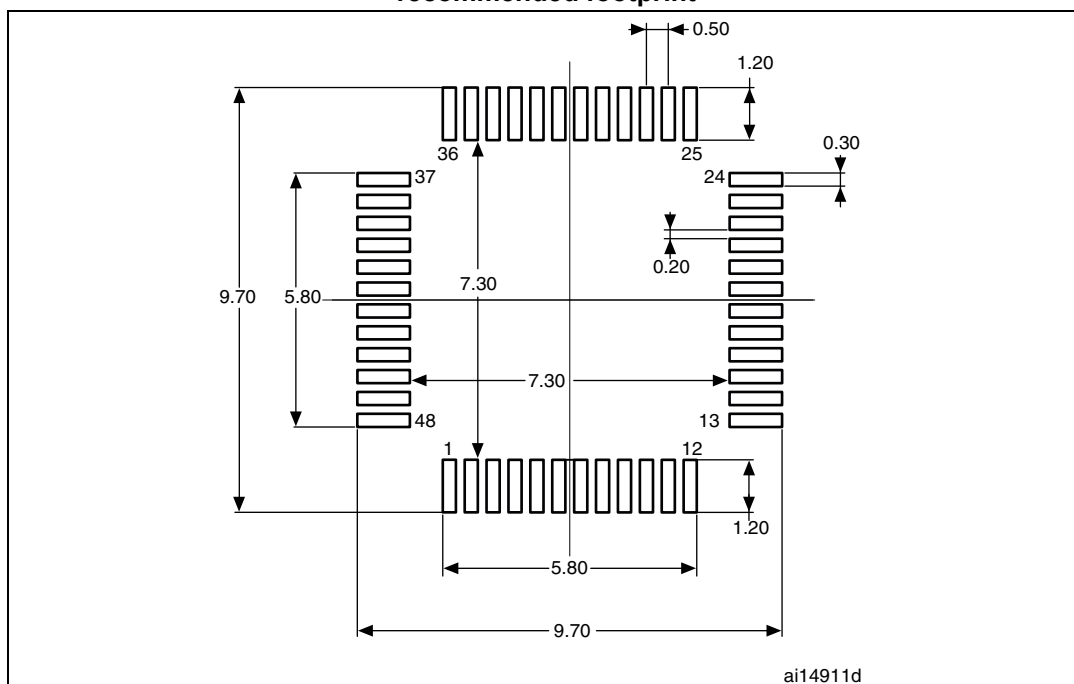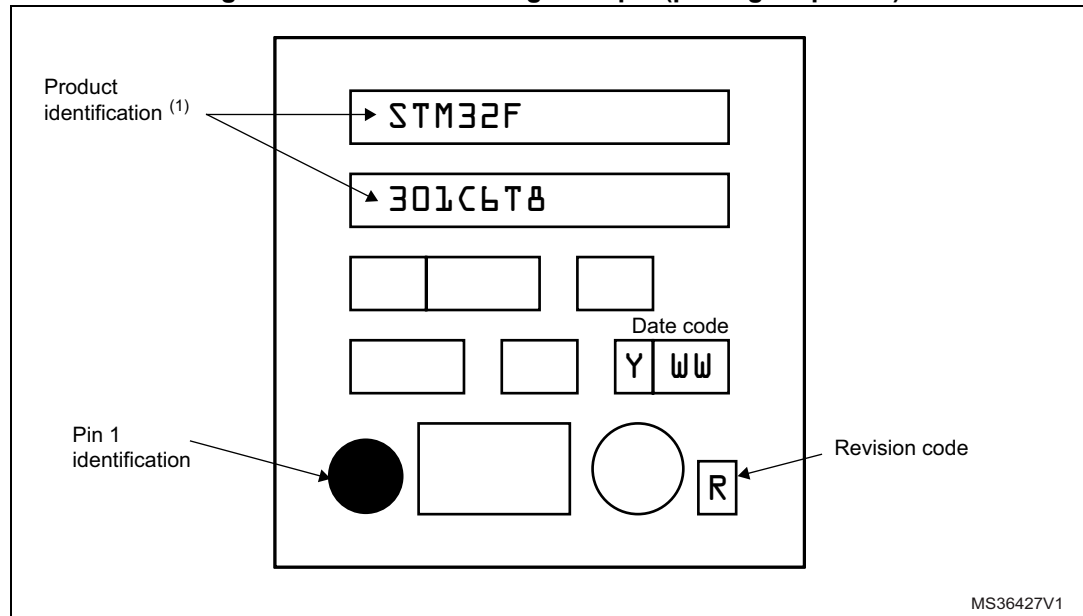

1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. LQFP48 marking example (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F301x6 STM32F301x8 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL} = 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL} = 1.3 V

P_{INTmax} = 50 mA × 3.5 V = 175 mW

P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 61.6 mW:

P_{Dmax} = 175 + 61.6 = 236.6 mW

Thus: P_{Dmax} = 236.6 mW

Using the values obtained in *Table 80* T_{Jmax} is calculated as follows:

– For LQFP64, 45°C/W

T_{Jmax} = 82 °C + (45°C/W × 236.6 mW) = 82°C + 10.65 °C = 92.65°C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Ordering information*).