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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f301k6u6

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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3 Functional overview

3.1 ARM[®] Cortex[®]-M4 core with FPU, embedded Flash and SRAM

The ARM[®] Cortex[®]-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 32-bit RISC processor with FPU features exceptional codeefficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single-precision FPU speeds up software development by using metalanguage development tools while avoiding saturation.

With its embedded ARM core, the STM32F301x6/8 family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F301x6/8 family devices.

3.2 Memories

3.2.1 Embedded Flash memory

All STM32F301x6/8 devices feature up to 64 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.2.2 Embedded SRAM

STM32F301x6/8 devices feature 16 Kbytes of embedded SRAM.

3.3 Boot modes

At startup, BOOT0 pin and BOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10) and USART2 (PA2/PA3).





Figure 2. Clock tree



4 Pinouts and pin description



1. The above figure shows the package top view.





1. The above figure shows the package top view.

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				-	Table	14. Altern	ate functio	ons for P	Ort A (C	ontinue	a)				-	
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port & pin name	SYS_AF	TIM2/TIM15/TIM16 /TIM17/EVENT	I2C3/TIM1/TIM2/TIM15	I2C3/TIM15/TSC	I2C1/I2C2/TIM1/ TIM16/TIM17	SPI2/I2S2/ SPI3/I2S3/Infrared	SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared	USART1/USART2/USART3/ GPCOMP6	I2C3/GPCOMP2 /GPCOMP4/GPCOMP6	TIM1/TIM15	TIM2/TIM17	TIM1	TIM1			EVENT
PA9	-	-	I2C3 _SMBAL	TSC _G4_IO1	I2C2 _SCL	I2S3 _MCK	TIM1_CH2	USART1 _ ^{TX}	-	TIM15 _BKIN	TIM2 _CH3	-	-	-	-	EVENT OUT
PA10	-	TIM17 _BKIN		TSC _G4_IO2	I2C2 _SDA	SPI2_MIS O/I2S2ext _SD	TIM1_CH3	USART1 _RX	COMP6 _OUT	-	TIM2 _CH4	-	-	-	-	EVENT OUT
PA11	-	-	-	-	-	SPI2_MO SI/I2S2 _SD	TIM1 _CH1N	USART1 _CTS	-	-	-	TIM1 _CH4	TIM1 _BKIN2	-	-	EVENT OUT
PA12	-	TIM16 _CH1	-	-	-	I2SCKIN	TIM1 _CH2N	USART1 _RTS_D E	COMP2 _OUT	-	-	TIM1 _ETR	-	-	-	EVENT OUT
PA13	SWDAT- JTMS	TIM16 _CH1N	-	TSC _G4_IO3	-	IR-OUT	-	USART3 _CTS	-	-	-	-	-	-	-	EVENT OUT
PA14	SWCLK- JTCK		-	TSC _G4_IO4	I2C1 _SDA	-	TIM1_BKIN	USART2 _TX	-	-	-	-	-	-	-	EVENT OUT
PA15	JTDI	TIM2_C H1/ TIM2_E TR	-	TSC _SYNC	I2C1 _SCL	-	SPI3_NSS/ I2S3_WS	USART2 _RX	-	TIM1 _BKIN	-	-	-	-	-	EVENT OUT

Pinouts and pin description

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6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20: Voltage characteristics*, *Table 21: Current characteristics*, and *Table 22: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Min	Мах	Unit
V _{DD} -V _{SS}	External main supply voltage (including $V_{DDA,}$ V_{BAT} and $V_{DD})$	-0.3	4.0	V
V _{DD} -V _{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
	Input voltage on FT and FTf pins	V _{SS} –0.3	V _{DD} + 4.0	
	Input voltage on TTa and TT pins	V _{SS} –0.3	4.0	
$V_{IN}^{(2)}$	Input voltage on any other pin	V _{SS} -0.3	4.0	V
	Input voltage on Boot0 pin	0	9	
$ \Delta V_{DDx} $	Variations between different V _{DD} power pins	-	50	m\/
V _{SSX} –V _{SS}	Variations between all the different ground $pins^{(3)}$	-	50	111V
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	see Section 6.3. sensitivity charac	12: Electrical cteristics	V

Table 20	. Voltage	characteristics ⁽¹⁾
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All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}: V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence. V_{DDA} must be greater than or equal to V_{DD}.

2. V_{IN} maximum must always be respected. Refer to *Table 21: Current characteristics* for the maximum allowed injected current values.

3. Include V_{REF-} pin.



				All peripherals enabled				All peripherals disabled				
Symbol	Parameter	Conditions	f _{HCLK}	Ŧ	М	ax @ T,	4 ⁽¹⁾	-	Max @ T _A ⁽¹⁾			Unit
				тур	25 °C	85 °C	105 °C	тур	25 °C	85 °C	105 °C	
			72 MHz	45.8	49.1 ⁽²⁾	50.1	51.4 ⁽²⁾	25.1	27.3 ⁽²⁾	28.0	28.6 ⁽²⁾	
			64 MHz	40.8	43.6	44.9	46.9	22.3	24.1	25.0	25.5	
		External	48 MHz	30.2	32.9	33.5	34.8	17.0	18.7	19.1	19.6	
		clock (HSE	32 MHz	20.5	23.1	24.1	25.4	11.1	12.2	13.2	13.3	
	Supply	bypass)	24 MHz	15.4	17.1	18.3	19.5	8.5	9.7	10.1	10.2	
	current in		8 MHz	5.0	5.9	6.3	6.9	3.1	3.7	4.1	4.7	
IDD	executing		1 MHz	0.8	1.1	1.9	2.6	0.5	0.8	1.2	1.4	
	from RAM		64 MHz	37.3	41.1	41.8	43.3	22.0	23.8	24.4	24.9	
		Internal clock (HSI)	48 MHz	28.0	31.1	31.6	33.2	16.4	18.0	18.3	18.6	mA
			32 MHz	18.8	21.3	22.1	23.1	10.9	11.9	12.8	13.1	
			24 MHz	14.2	15.9	16.8	17.9	5.5	6.4	6.7	7.3	
			8 MHz	4.8	5.1	6.0	6.5	2.9	3.5	4.1	4.2	
			72 MHz	30.0	32.8 ⁽²⁾	33.1	34.1 ⁽²⁾	5.9	6.8 ⁽²⁾	6.9	7.4 ⁽²⁾	
			64 MHz	26.7	29.2	29.6	30.5	5.3	5.9	6.2	6.7	
		External	48 MHz	16.7	18.5	19.0	19.7	3.6	4.5	4.5	5.3	
	Quarte	clock (HSE	32 MHz	13.3	14.9	15.3	15.4	2.9	3.7	3.8	4.3	
	current in	bypass)	24 MHz	10.2	11.4	12.0	12.3	2.2	2.7	2.9	3.2	
	Sleep		8 MHz	3.6	4.4	4.8	5.3	0.9	1.2	1.5	2.1	
IDD	executing		1 MHz	0.5	0.8	1.1	1.3	0.1	0.4	0.8	0.8	
	from Flash		64 MHz	23.2	25.3	25.6	26.2	5.0	5.7	6.1	6.2	
			48 MHz	17.5	19.2	19.4	19.9	3.9	4.7	4.8	5.3	
		Internal clock (HSI)	32 MHz	11.7	12.9	13.2	13.3	2.6	3.4	3.6	4.2	mA
			24 MHz	8.9	10.2	10.6	10.8	1.4	2.1	2.4	2.7	
			8 MHz	3.4	4.0	4.6	5.1	0.7	1.1	1.4	1.9	

Table 29. Typical and maximum current consumption from VDD supply at VDD = 3.6V (continued)

1. Guaranteed by characterization results.

2. Data based on characterization results and tested in production with code executing from RAM.



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Тур	Max ⁽²⁾	Unit
	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	
I _{DD}		LSEDRV[1:0]=10 medium low driving capability	-	-	1	μΑ
		LSEDRV[1:0]=01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
		LSEDRV[1:0]=00 lower driving capability	5	-	-	
a	Oscillator	LSEDRV[1:0]=10 medium low driving capability	8	-	-	
Эm	transconductance	LSEDRV[1:0]=01 medium high driving capability	15	-	-	μ~νν
g _m		LSEDRV[1:0]=11 higher driving capability	LSEDRV[1:0]=11 25 -		-	
t _{SU(LSE)} ⁽³⁾	Startup time	V _{DD} is stabilized	-	2	-	S

Table 43. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

2. Guaranteed by design.

3. t_{SU(LSE)} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website <u>www.st.com</u>.



Low-speed internal (LSI) RC oscillator

Table 45. LSI o	oscillator	characteristics ⁽¹⁾
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Symbol	Parameter	Min	Тур	Max	Unit
f _{LSI}	Frequency	30	40	50	kHz
t _{su(LSI)} ⁽²⁾	LSI oscillator startup time	-	-	85	μs
I _{DD(LSI)} ⁽²⁾	LSI oscillator power consumption	-	0.75	1.2	μA

1. V_{DDA} = 3.3 V, T_A = -40 to 105 °C unless otherwise specified.

2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 46* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23*.

Symbol f _{PLL_IN} f _{PLL_OUT} t _{LOCK} Jitter	Deremeter		Unit		
	Parameter	Min	Тур	Max	Unit
f	PLL input clock ⁽¹⁾	1 ⁽²⁾	-	24 ⁽²⁾	MHz
'PLL_IN	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
f _{PLL_OUT}	PLL multiplier output clock	16 ⁽²⁾	-	72	MHz
t _{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μs
Jitter	Cycle-to-cycle jitter	-	-	300 ⁽²⁾	ps

Table 46. PLL characteristics

 Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

2. Guaranteed by design.



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Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Symbol	Parameter	Conditions	Monitored	Max vs. [f _{HSE} /f _{HCLK}]	Unit
Cymbol		Conditione	frequency band	8/72 MHz	•
		$V_{DD} = 3.3 \text{ V}, T_A = 25 ^{\circ}\text{C},$ LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	5	
s	Poak lovel		30 to 130 MHz	6	dBµV
SEMI	reakievei		130 MHz to 1GHz	28	
			SAE EMI Level	4	-

Table 50. EMI characteristics

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \times (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Symbol	Ratings	Conditions	Packages	Class	Maximum value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, conforming to JESD22-A114	All	2	2000	V
V _{ESD(CDM)}	Electrostatic discharge voltage	$T_A = +25 \degree C$, conforming	LQFP64, WLCSP49	C3	250	v
	(charge device model)		All other	C4	500	

Table 51. ESD absolute maximum ratings

1. Guaranteed by characterization results.



6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under the conditions summarized in *Table 23*. All I/Os are CMOS and TTL compliant.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
		TTa and TT I/O	-	-	$0.3 V_{DD} + 0.07$ ⁽¹⁾	
		FT and FTf I/O	-	-	0.475 V_{DD} -0.2 $^{(1)}$	
Vii	Low level input	BOOT0 I/O	-	-	$0.3 V_{DD} - 0.3$ ⁽¹⁾	V
- 12	voltage	All I/Os except BOOT0	-	-	0.3 V _{DD} ⁽²⁾	-
		TTa and TT I/O	0.445 V _{DD} +0.398 ⁽¹⁾	-	-	
		FT and FTf I/O	0.5 V _{DD} +0.2 ⁽¹⁾	-	-	
Vill	High level input	BOOT0	0.2 V _{DD} +0.95 ⁽¹⁾	-	-	V
- 10	voltage	All I/Os except BOOT0	0.7 V _{DD} ⁽²⁾	-	-	-
		TC and TTa I/O	-	200 (1)	-	
V _{hys}	Schmitt trigger hysteresis	FT and FTf I/O	-	100 ⁽¹⁾	-	mV
		BOOT0	-	300 (1)	-	
		TC, FT and FTf I/O				
		TTa I/O in digital mode	-	-	±0.1	
		V _{SS} ≤V _{IN} ≤V _{DD}				
	Input lookago	TTa I/O in digital mode	-	-	1	
	current ⁽³⁾	V _{DD} ≤V _{IN} ≤V _{DDA}				
l _{lkg}	ourion	TTa I/O in analog mode			+0.2	μA
		V _{SS} ≤V _{IN} ≤V _{DDA}	-	-	10.2	
		FT and FTf I/O ⁽⁴⁾			10	
		V _{DD} ≤V _{IN} ≤5 V	-	-	10	
R _{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	V _{IN} = V _{SS}	25	40	55	kΩ
R _{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	25	40	55	kΩ
C _{IO}	I/O pin capacitance	-	-	5	-	pF

Table 54	. I/O	static	characteristics
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1. Data based on design simulation

2. Tested in production.

3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to Table 53: I/O current injection susceptibility.

- 4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
- 5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).





Figure 23. I/O AC characteristics definition

1. See Table 56: I/O AC characteristics.

6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IL(NRST)} ⁽¹⁾	NRST Input low level voltage	-	-	-	0.3V _{DD} + 0.07 ⁽¹⁾	V
V _{IH(NRST)} ⁽¹⁾	NRST Input high level voltage	-	0.445V _{DD} + 0.398 ⁽¹⁾	-	-	v
V _{hys(NRST)}	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R _{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ
V _{F(NRST)} ⁽¹⁾	NRST Input filtered pulse	-	-	-	100 ⁽¹⁾	ns
V _{NF(NRST)} ⁽¹⁾	NRST Input not filtered pulse	-	500 ⁽¹⁾	-	-	ns

Table 57. NRST pin characteristics

1. Guaranteed by design.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).



Table 33. TWDG minimax timeout periou at 40 km2 (LGI)							
Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF				
/4	0	0.1	409.6				
/8	1	0.2	819.2				
/16	2	0.4	1638.4				
/32	3	0.8	3276.8				
/64	4	1.6	6553.6				
/128	5	3.2	13107.2				
/256	7	6.4	26214.4				

Table 59. IWDG min/max timeout period at 40 kHz (LSI) ⁽¹⁾

 These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 60. WWDO	S min-max timeout	value @72 MHz	(PCLK) ⁽¹⁾
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Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design.



	Sompling	Sompling		R _{AIN} max (kΩ)	
Resolution	cycle @ 72 MHz	time [ns] @ 72 MHz	Fast channels ⁽²⁾	Slow channels	Other channels ⁽³⁾
	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
10 bits	7.5	104.17	1.20	0.82	0.68
TO DIIS	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
8 DIIS	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	(kΩ) Other channels ⁽³⁾ NA 2 0.100 0 0.330 0 0.68 2.20 6.8 22.0 6.8 22.0 6.8 0.039 0.180 0 0.470 1.00 2.70 2.270 8.20 0 0.470 0 0.150 0 0.330 0 0.150 1.50 3.90 12.0 39.0 100.0 100.0
	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
6 hito	7.5	104.17	2.20	1.80	1.50
6 bits	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

Table 65. Maximum ADC R_{AIN} ⁽¹⁾ (continued)

1. Guaranteed by characterization results.

2. All fast channels, expect channel on PA6.

3. Channel available on PA6.



STM32F301x6 STM32F301x8

Symbol	Parameter	Conditions				Max (4)	Unit
			Single ended	Fast channel 5.1 Ms	-	±6.5	
ст	Total		Single ended	Slow channel 4.8 Ms	-	±6.5	
	error		Differential	Fast channel 5.1 Ms	-	±4	
			Dillerential	Slow channel 4.8 Ms	-	±4.5	
			Single ended	Fast channel 5.1 Ms	-	±3	
E0	Offect orror		Single ended	Slow channel 4.8 Ms	-	±3	
EO	Oliset en ol		Differential	Fast channel 5.1 Ms	-	±2.5	
			Differential	Slow channel 4.8 Ms	-	±2.5	
			Single ended	Fast channel 5.1 Ms	-	±6	
EG Gain error	Coin orror		Single ended	Slow channel 4.8 Ms	-	±6	
	Gainenoi		Differential	Fast channel 5.1 Ms	-	±3.5	LOD
				Slow channel 4.8 Ms	-	±4	-
		erential ADC clock freq. \leq 72 MHz, arity Sampling freq. \leq 5 Msps r 2.0 V \leq V _{DDA} \leq 3.6 V	Single ended	Fast channel 5.1 Ms	-	±1.5	
ED	Differential			Slow channel 4.8 Ms	-	±1.5	
ED	error		Differential	Fast channel 5.1 Ms	-	±1.5	
			Differential	Slow channel 4.8 Ms	-	±1.5	
			Single ended	Fast channel 5.1 Ms	-	±3	
-	Integral	Integral linearity error		Slow channel 4.8 Ms	-	±3.5	
	error		Differential	Fast channel 5.1 Ms	-	±2	
			Dillerential	Slow channel 4.8 Ms	-	±2.5	
			Single ended	Fast channel 5.1 Ms	10.4	-	
ENOB	Effective		Single ended	Slow channel 4.8 Ms	10.4	-	hito
(5)	bits		Differential	Fast channel 5.1 Ms	10.8	-	DILS
			Dillerential	Slow channel 4.8 Ms	10.8	-	
	Signal to		Single ended	Fast channel 5.1 Ms	64	-	
SINAD	noise and			Slow channel 4.8 Ms	63	-	dP
(5)	distortion		Difforantial	Fast channel 5.1 Ms	67	-	
	ratio	ratio		Slow channel 4.8 Ms	67	-]

Table 67. ADC accuracy ⁽¹⁾⁽²⁾⁽³⁾



Symbol	Parameter	C	Min ⁽⁴⁾	Max (4)	Unit		
SNR ⁽⁵⁾			Single ended	Fast channel 5.1 Ms	64	-	
	Signal-to-		Single ended	Slow channel 4.8 Ms	64	-	
	noise ratio	ADC clock freq. \leq 72 MHz,	Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	dD
		$2 V \le V_{\Box \Box \Delta} \le 3.6 V$	Single ended	Fast channel 5.1 Ms	-	-75	uВ
тun ⁽⁵⁾	Total			Slow channel 4.8 Ms	-	-75	
THD	distortion		Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

Table 67. ADC accuracy ⁽¹⁾⁽²⁾⁽³⁾ (continued)

1. ADC DC accuracy values are measured after internal calibration.

 ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in Section 6.3.14 does not affect the ADC accuracy.

- 3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
- 4. Guaranteed by characterization results.
- 5. Value measured with a -0.5dB Full Scale 50kHz sine wave input signal.

Table	68. ADC	accuracy ⁽¹⁾⁽²⁾
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Symbol	Parameter	Test condition	IS	Тур	Max ⁽³⁾	Unit
ст	Total upadiusted error		Fast channel	±2.5	±5	
			Slow channel	±3.5	±5	
FO	Offset error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V _{DDA} = V _{REF+} ≤ 3.6 V	Fast channel	±1	±2.5	-
LO			Slow channel	±1.5	±2.5	
EG	Cain arrar		Fast channel	±2	±3	
LG	Gainenoi		Slow channel	±3	±4	LOD
ED	Differential linearity error	Single-ended mode	Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
I	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.

 ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in Section 6.3.14: I/O port characteristics does not affect the ADC accuracy.

3. Guaranteed by characterization results.



6.3.19 DAC electrical specifications

Symbol	Parameter	Cond	itions	Min	Тур	Мах	Unit
V _{DDA}	Analog supply voltage	DAC output buffer ON		2.4	-	3.6	V
р (1)	Posiativo lood		Connected to V _{SSA}	5	-	-	kΩ
RLOAD'	Resistive load	DAC output buller ON	Connected to V _{DDA}	25	-	-	
R ₀ ⁽¹⁾	Output impedance	DAC output buffer ON		-	-	15	kΩ
C _{LOAD} ⁽¹⁾	Capacitive load	DAC output buffer ON		-	-	50	pF
V _{DAC OUT}	Voltage on DAC_OUT output	Corresponds to 12-bit i (0xF1C) at V _{DDA} = 3.6 and (0x155) and (0xEA DAC output buffer ON.	nput code (0x0E0) to V vB) at V _{DDA} = 2.4 V	0.2	-	V _{DDA} – 0.2	V
		DAC output buffer OFF		-	0.5	V _{DDA} - 1LSB	mV
مرما ⁽³⁾	DAC DC current consumption in	With no load, middle code (0x800) on the input.		-	-	380	μA
UDA	^{IDDA^(*) quiescent mode (Standby mode)⁽²⁾ With no load, wors}		le (0xF1C) on the input.	-	-	480	μA
Differential non		Given for a 10-bit input	code	-	-	±0.5	LSB
DNL ⁽³⁾	linearity Difference between two consecutive code- 1LSB)	Given for a 12-bit input code		-	-	±2	LSB
	Integral non linearity	Given for a 10-bit input	code	-	-	±1	LSB
INL ⁽³⁾	(difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 12-bit input code		-	-	±4	LSB
	Offset error (difference		-	-	-	±10	mV
Offset ⁽³⁾	value at Code (0x800)	Given for a 10-bit input	code at V_{DDA} = 3.6 V	-	-	±3	LSB
	and the ideal value = V _{DDA} /2)	Given for a 12-bit input	code at V _{DDA} = 3.6 V	-	-	±12	LSB
Gain error ⁽³⁾	Gain error	Given for a 12-bit input	code	-	-	±0.5	%
tsettling ⁽³⁾	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches	C _{LOAD} ∕50 pF, R _{LOAD} ≥ 5 kΩ		-	3	4	μs

Table 69. DAC characteristics



7.2 LQFP64 package information

Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat
package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Max	Min	Тур	Max
А	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
С	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-



package mechanical data (continued)						
Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Мах
E3	-	7.500	-	-	0.2953	-
е	-	0.500	-	-	0.0197	-
К	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
CCC	-	-	0.080	-	-	0.0031

Table 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

1. Values in inches are converted from mm and rounded to 4 decimal digits.



Figure 40. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

1. Dimensions are expressed in millimeters.



7.5 Thermal characteristics

The maximum chip junction temperature (T_Jmax) must never exceed the values given in *Table 23: General operating conditions*.

The maximum chip-junction temperature, $T_{\rm J}$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J max = T_A max + (P_D max x \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in ° C/W,
- P_D max is the sum of P_{INT} max and P_{I/O} max (P_D max = P_{INT} max + P_{I/O}max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

 $P_{I/O}$ max represents the maximum power dissipation on output pins where:

 $\mathsf{P}_{\mathsf{I}/\mathsf{O}} \max = \Sigma \; (\mathsf{V}_{\mathsf{OL}} \times \mathsf{I}_{\mathsf{OL}}) + \Sigma ((\mathsf{V}_{\mathsf{DD}} - \mathsf{V}_{\mathsf{OH}}) \times \mathsf{I}_{\mathsf{OH}}),$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Symbol	Parameter	Value	Unit	
Θ _{JA}	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45		
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	°C 111	
	Thermal resistance junction-ambient WCSP49 - 3.4 x 3.4 mm	49		
	Thermal resistance junction-ambient UFQFN32 - 5 x 5 mm	37		

Table 80. Package thermal characteristics

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

