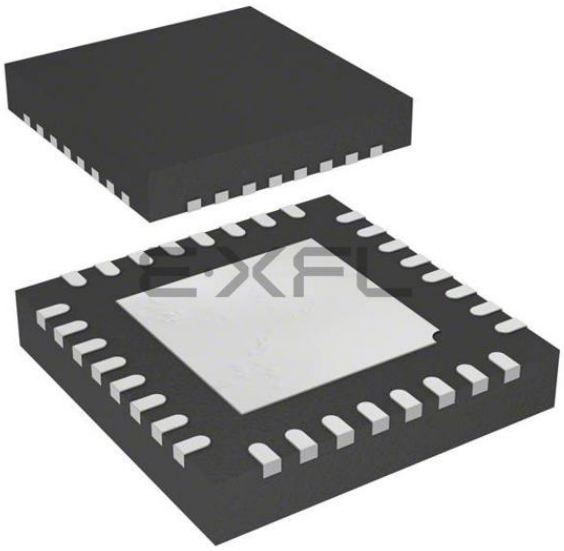

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f301k6u6tr

Contents

mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI2 and SPI3.

Table 9. STM32F301x6/8 SPI/I2S implementation

SPI features(1)	SPI2	SPI3
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	X	X
TI mode	X	X

1. X = supported.

3.20 Touch sensing controller (TSC)

The STM32F301x6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (for example glass, plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

3.22 Development support

3.22.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Table 13. STM32F301x6/8 pin definitions (continued)

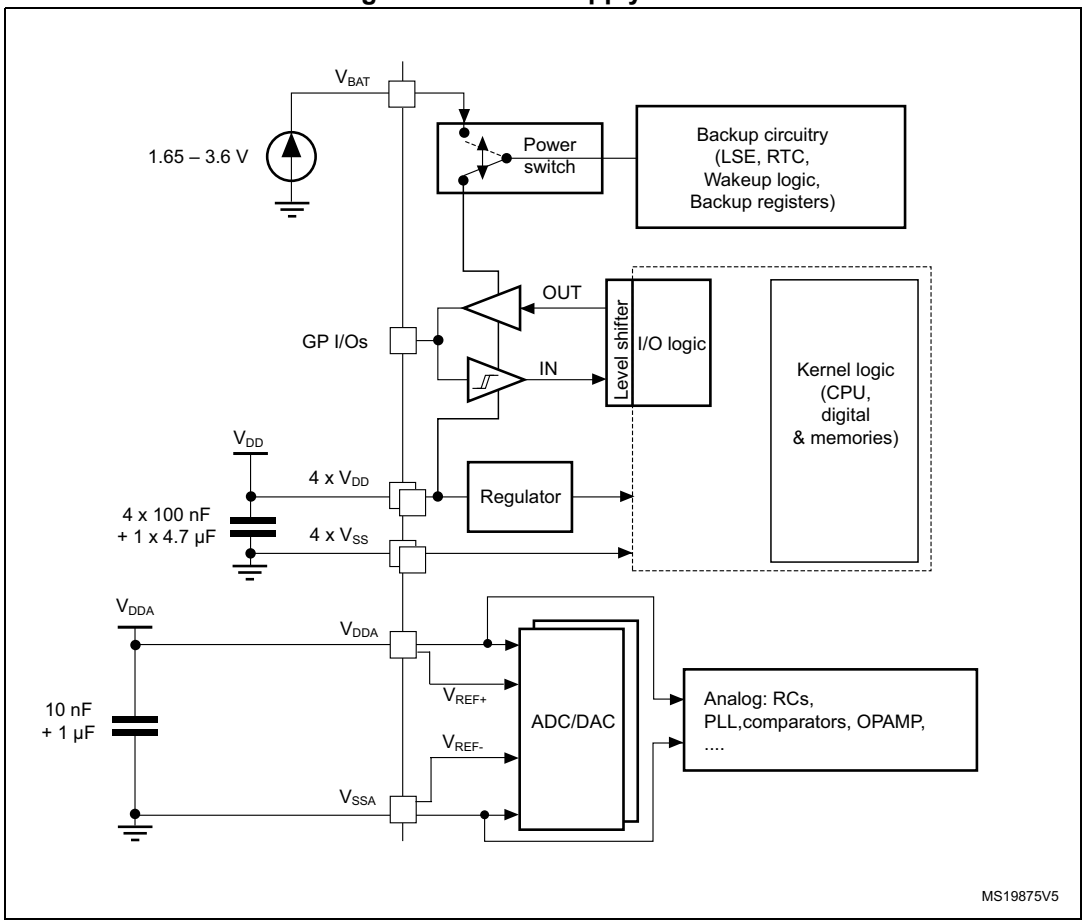
Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	24	PC4	I/O	TT	-	EVENTOUT, TIM1_ETR, USART1_TX	
-	-	-	25	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	OPAMP2_VINM
15	G5	18	26	PB0	I/O	TTa	-	TSC_G3_IO2, TIM1_CH2N, EVENTOUT	ADC1_IN11, COMP4_INP, OPAMP2_VINP
-	G4	19	27	PB1	I/O	TTa	-	TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC1_IN12
-	G3	20	28	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	COMP4_INM
-	E3	21	29	PB10	I/O	TT	-	TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	
-	G2	22	30	PB11	I/O	TTa	-	TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC1_IN14, COMP6_INP
16	D3	23	31	VSS_2	S	-	-	Digital ground	
17	B2	24	32	VDD_2	S	-	-	Digital power supply	
-	E2	25	33	PB12	I/O	TT	-	TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	
-	G1	26	34	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	ADC1_IN13

Table 13. STM32F301x6/8 pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN32	WLCSP49	LQFP48	LQFP64						
-	-	-	51	PC10	I/O	FT	-	EVENTOUT, SPI3_SCK/I2S3_CK, USART3_TX	-
-	-	-	52	PC11	I/O	FT	-	EVENTOUT, SPI3_MISO/I2S3ext_SD, USART3_RX	-
-	-	-	53	PC12	I/O	FT	-	EVENTOUT, SPI3_MOSI/I2S3_SD, USART3_CK	-
-	-	-	54	PD2	I/O	FT	-	EVENTOUT	-
26	A3	39	55	PB3	I/O	FT	-	JTDO-TRACESWO, TIM2_CH2, TSC_G5_IO1, SPI3_SCK/I2S3_CK, USART2_TX, EVENTOUT	-
27	A4	40	56	PB4	I/O	FT	-	JTRST, TIM16_CH1, TSC_G5_IO2, SPI3_MISO/I2S3ext_SD, USART2_RX, TIM17_BKIN, EVENTOUT	-
28	B4	41	57	PB5	I/O	FT	-	TIM16_BKIN, I2C1_SMBAI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, EVENTOUT	-
29	C4	42	58	PB6	I/O	FTf	-	TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, EVENTOUT	-
30	D4	43	59	PB7	I/O	FTf	-	TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, EVENTOUT	-

6.1.6 Power supply scheme

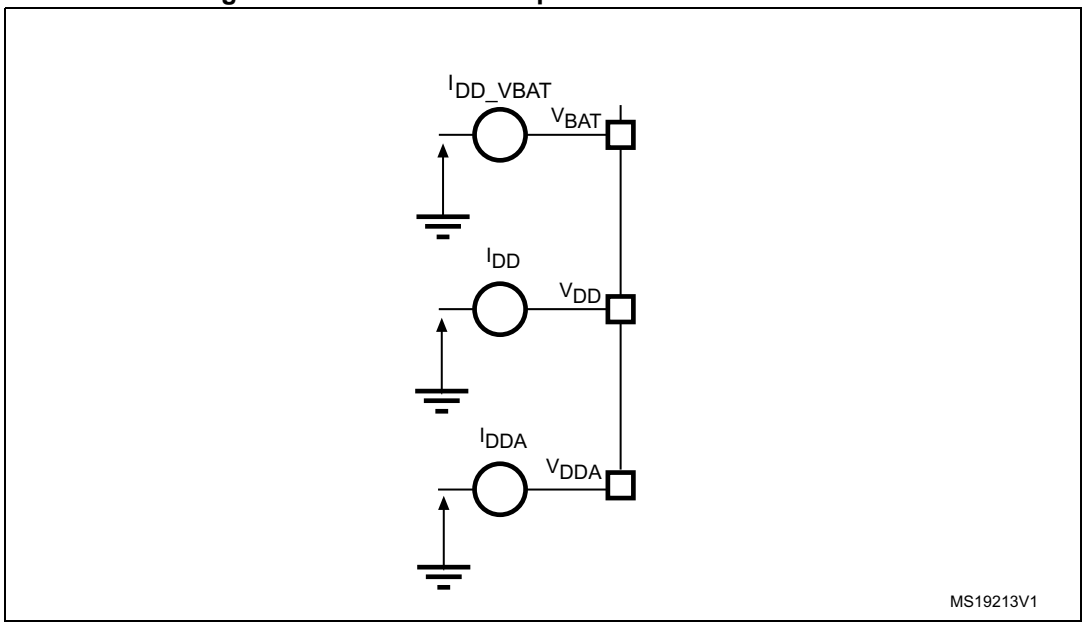
Figure 11. Power supply scheme



Caution: Each power supply pair (for example V_{DD}/V_{SS}, V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 54: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 37: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 38* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23*.

Table 38. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD}, V_{DD} = V_{DDA}						Max	Unit
			2.0 V	2.4 V	2.7 V	3 V	3.3 V	3.6 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.5	4.2	4.1	4.0	3.8	3.8	4.5	µs
		Regulator in low-power mode	8.2	7.0	6.4	6.0	5.7	5.5	9.0	
$t_{WUSTANDBY}$(1)	Wakeup from Standby mode	LSI and IWDG OFF	72.8	63.4	59.2	56.1	53.1	51.3	103	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	6						-	CPU clock cycles

1. Guaranteed by characterization results.

Table 39. Wakeup time using USART(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART baud rate allowing to wakeup up from Stop mode when the USART clock source is HSI	Stop mode with main regulator in low-power mode	-	13.125	µs
		Stop mode with main regulator in run mode	-	3.125	

1. Guaranteed by design.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

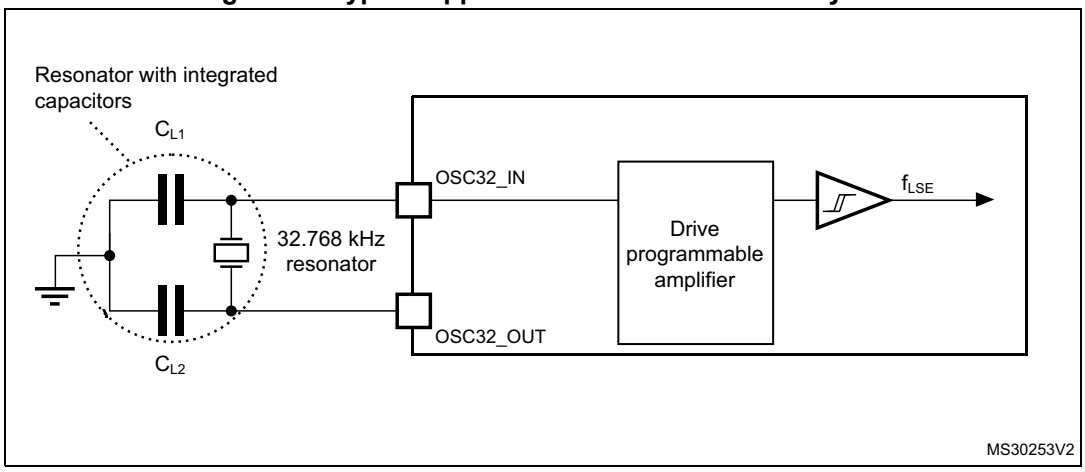
Table 43. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]=10 medium low driving capability	-	-	1	
		LSEDRV[1:0]=01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]=10 medium low driving capability	8	-	-	
		LSEDRV[1:0]=01 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 17. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23*.

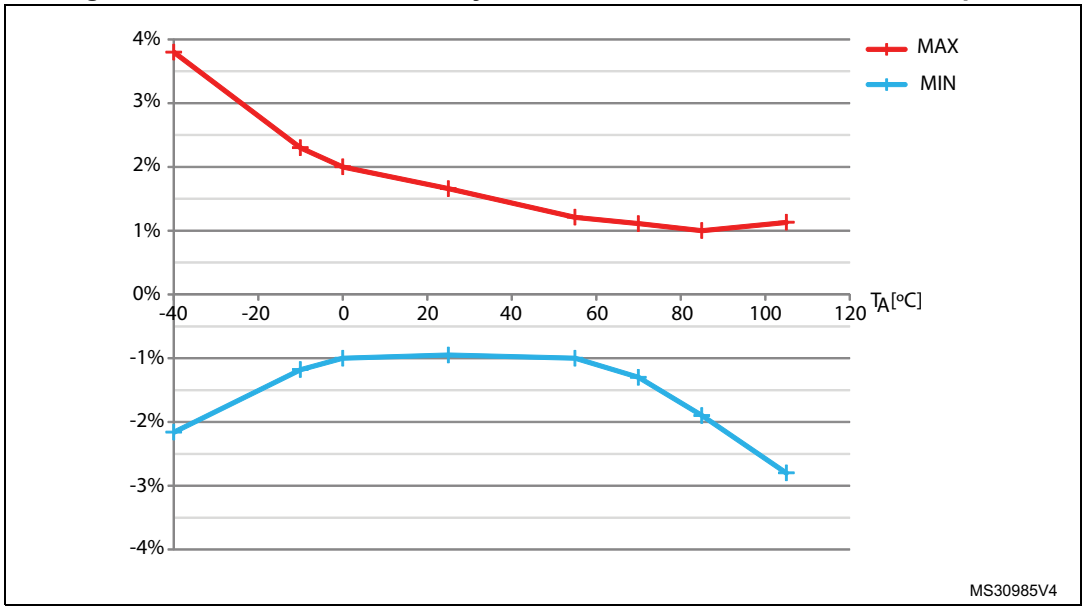
High-speed internal (HSI) RC oscillator

Table 44. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Factory calibrated, parts not soldered.

Figure 18. HSI oscillator accuracy characterization results for soldered parts



6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 47. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design.

Table 48. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 52. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	2 level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

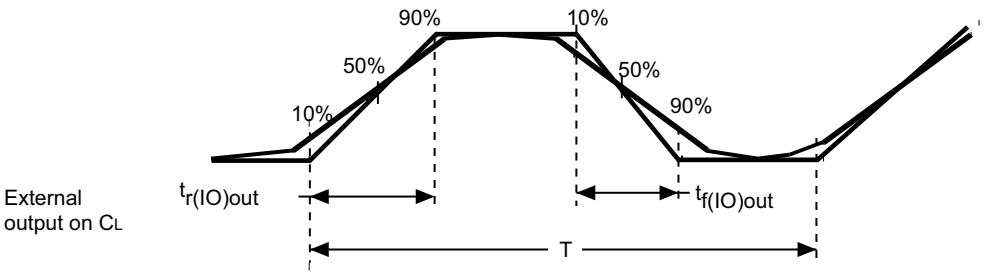
The test results are given in *Table 53*

Table 53. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PC0 pin (TTa pin)	-0	+5	
	Injected current PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA6, PA7, PC4, PB0, PB10, PB11, PB13 with induced leakage current on other pins from this group less than -100 µA or more than +100 µA	-5	+5	
	Injected current on any other TT, FT and FTf pins	-5	NA	
	Injected current on all other TC, TTa and RESET pins	-5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

Figure 23. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by C_L (see note 1).

MS34942V1

1. See *Table 56: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23*.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}$+ 0.07(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD}$+ 0.398(1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500(1)	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 62* for SPI or in *Table 63* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 23*.

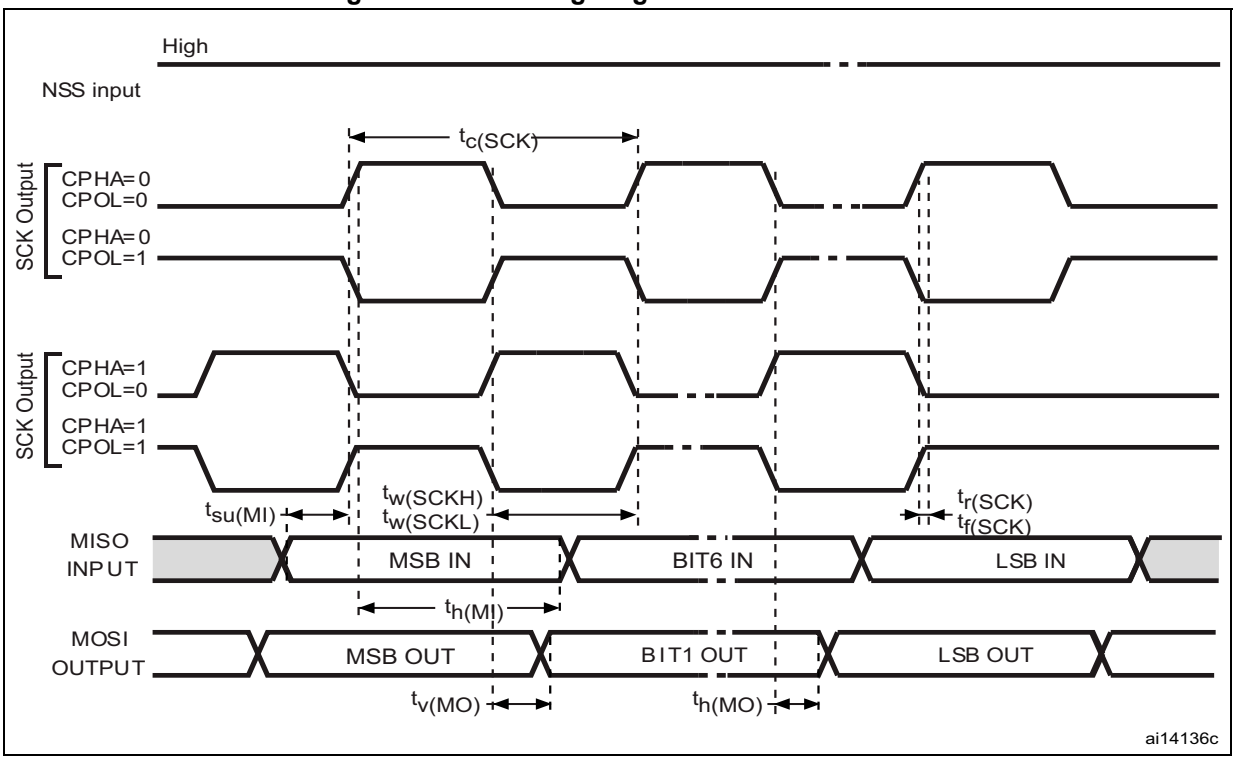
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 62. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	18	MHz
		Slave mode	-	-	18	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	0	-	-	
		Slave mode	1	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	
$t_{h(SI)}$		Slave mode	2.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	8	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	8	-	14	
$t_{v(SO)}$	Data output valid time	Slave mode	-	12	27	
$t_{v(MO)}$		Master mode	-	1.5	4	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Guaranteed by characterization results.

Figure 27. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Table 63. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs (2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%

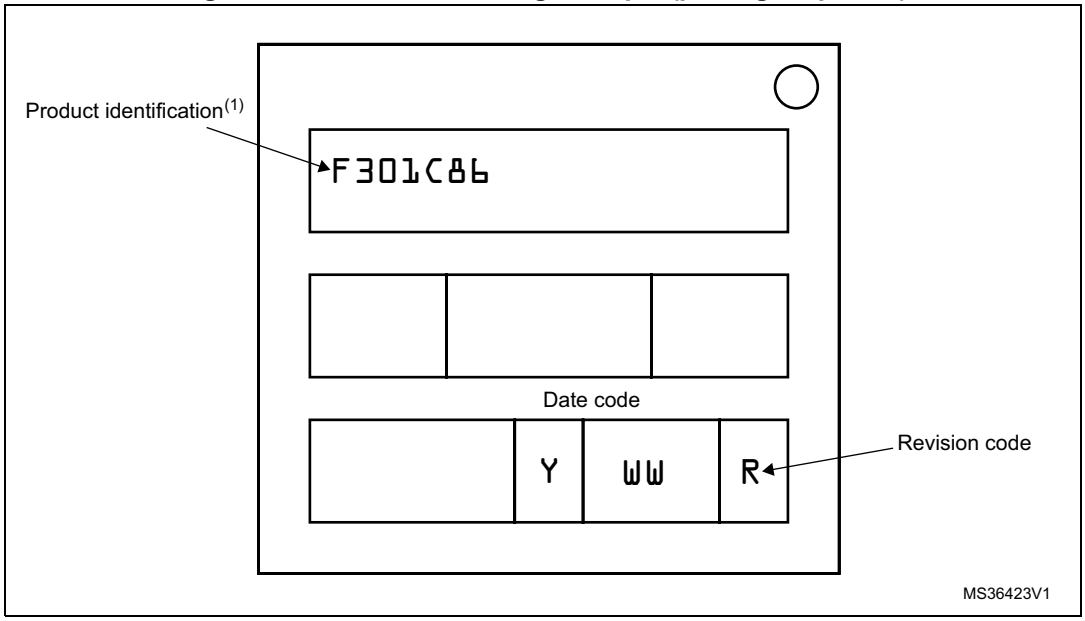
Table 76. WLCSP49 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

Device marking

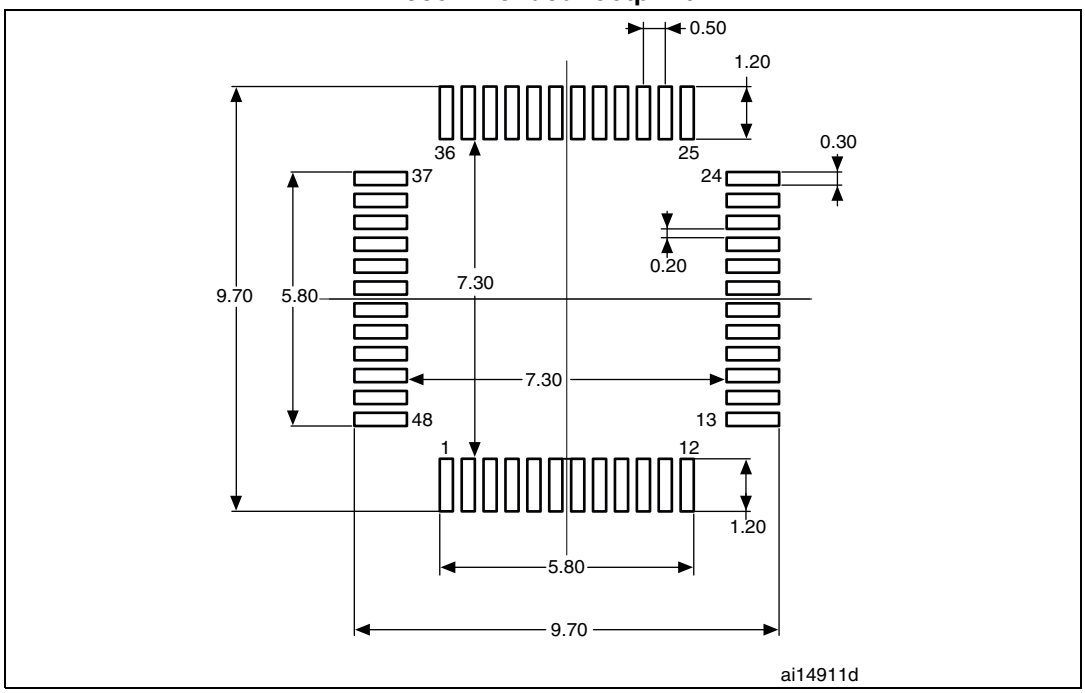
The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 38. WLCSP49 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Figure 43. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 82. Document revision history (continued)

Date	Revision	Changes
04-Jun-2015	5	Updated: – AF9 value for PA1, PA3 and PA9 in *Table 14: Alternate functions for Port A*, – the structure of *Section 7: Package information*.
22-Jul-2016	6	Updated notes on: – All document tables by removing the “not tested in production” specification. – *Table 13: STM32F301x6/8 pin definitions*. – *Table 20: Voltage characteristics*. – *Table 70: Comparator characteristics*. – *Figure 4: STM32F301x6/8 UFQFN32 pinout*. – *Figure 5: STM32F301x6/8 LQFP48 pinout*. – *Figure 6: STM32F301x6/8 LQFP64 pinout*. – *Figure 7: STM32F301x6/8 WLCSP49 ballout*. – *Figure 24: Recommended NRST pin protection*. – *Figure 45: UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline*. Updated tables: – Updated V_{REFINT} line on *Table 27: Embedded internal reference voltage*. – Updated “Conditions” column on *Table 43: LSE oscillator characteristics (fLSE = 32.768 kHz)*. – Added CMIR and t_{STAB} lines on *Table 64: ADC characteristics*. – Updated R_{LOAD} line on *Table 69: DAC characteristics*. – Updated VOH_{SAT} and VOL_{SAT} lines on *Table 71: Operational amplifier characteristics*. Updated figures: – *Figure 2: Clock tree*. – *Figure 7: STM32F301x6/8 WLCSP49 ballout*. – *Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port*. – *Figure 24: Recommended NRST pin protection*. Added: – *Table 39: Wakeup time using USART* Updated name of *Section 8: Ordering information*