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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 15x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f301r8t6 |

**Table 2. STM32F301x6/8 device features and peripheral counts**

| Peripheral | | STM32F301Kx | | STM32F301Cx | | STM32F301Rx | |
|---|---|---|---|---|---|---|---|
| Flash (Kbytes) | | 32 | 64 | 32 | 64 | 32 | 64 |
| SRAM (Kbytes) | | 16 | | | | | |
| Timers | Advanced control | 1 (16-bit) | | | | | |
| | General purpose | 3 (16-bit)<br>1 (32 bit) | | | | | |
| | Basic | 1 | | | | | |
| | SysTick timer | 1 | | | | | |
| | Watchdog timers (independent, window) | 2 | | | | | |
| | PWM channels (all) (1) | 16 | | 18 | | | |
| | PWM channels (except complementary) | 10 | | 12 | | | |
| Comm. interfaces | SPI/I2S | 2 | | | | | |
| | $I^2C$ | 3 | | | | | |
| | USART | 2 | | 3 | | | |
| DMA channels | | 7 | | | | | |
| Capacitive sensing channels | | 18 | | | | | |
| 12-bit ADC<br>Number of channels | | 1<br>8 | | 1<br>11 | | 1<br>15 | |
| 12-bit DAC channels | | 1 | | | | | |
| Analog comparator | | 2 | | 3 | | | |
| Operational amplifier | | 1 | | | | | |
| CPU frequency | | 72 MHz | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | |
| Operating temperature | | Ambient operating temperature:<br>- 40 to 85°C / - 40 to 105°C<br>Junction temperature: - 40 to 125°C | | | | | |
| Packages | | UFQFPN32 | | LQFP48, WLCSP49 | | LQFP64 | |

1. This total number considers also the PWMs generated on the complementary output channels.

## 3.18 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F301x6/8 devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbit/s.

All USARTs support hardware management of the CTS and RTS signals, multiprocessor communication mode, single-wire half-duplex communication mode and synchronous mode.

USART1 supports SmartCard mode, IrDA SIR ENDEC, LIN Master capability and autobaudrate detection.

All USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features available in all USARTs interfaces.

**Table 8. USART features**

| USART modes/features(1) | USART1 | USART2 | USART3 |
|---|---|---|---|
| Hardware flow control for modem | X | X | X |
| Continuous communication using DMA | X | X | X |
| Multiprocessor communication | X | X | X |
| Synchronous mode | X | X | X |
| SmartCard mode | X | - | - |
| Single-wire half-duplex communication | X | X | X |
| IrDA SIR ENDEC block | X | - | - |
| LIN mode | X | - | - |
| Dual clock domain and wakeup from Stop mode | X | - | - |
| Receiver timeout interrupt | X | - | - |
| Modbus communication | X | - | - |
| Auto baud rate detection | X | - | - |
| Driver Enable | X | X | X |

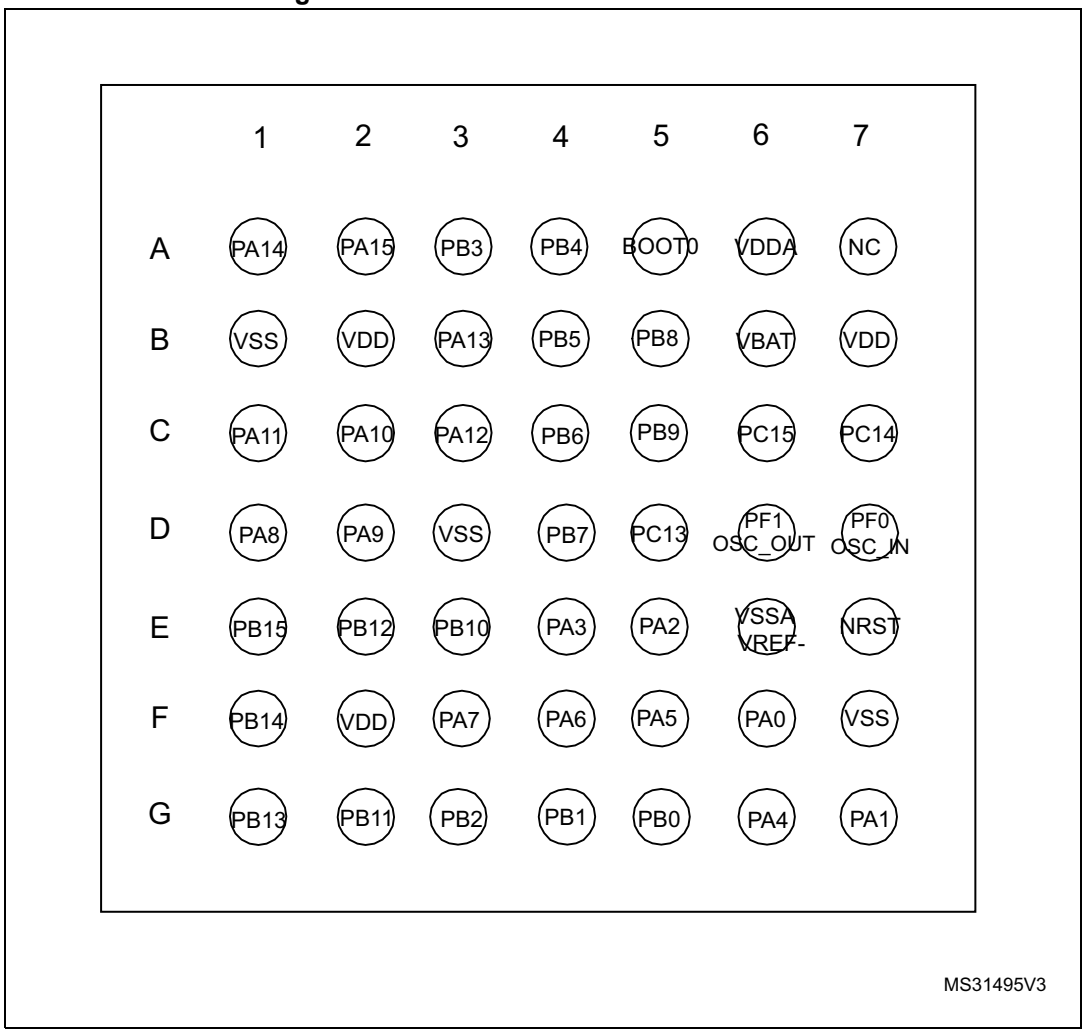
1. X = supported.

## 3.19 Serial peripheral interfaces (SPI)/Inter-integrated sound interfaces (I2S)

Two SPI interfaces (SPI2 and SPI3) allow communication up to 18 Mbit/s in slave and master modes in full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master

**Figure 7. STM32F301x6/8 WLCSP49 ballout**




1. The above figure shows the package top view.
2. NC: Not connected.

**Table 13. STM32F301x6/8 pin definitions**

| Pin Number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| UQFN32 | WLCSP49 | LQFP48 | LQFP64 | | | | | | |
| - | B6 | 1 | 1 | VBAT | S | - | - | Backup power supply | |
| - | D5 | 2 | 2 | PC13(1) TAMPER1 WKUP2 (PC13) | I/O | TC | (1) | TIM1_CH1N | WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT |
| - | C7 | 3 | 3 | PC14(1) OSC32_IN (PC14) | I/O | TC | (1) | - | OSC32_IN |
| - | C6 | 4 | 4 | PC15(1) OSC32_OUT (PC14) | I/O | TC | (1) | - | OSC32_OUT |
| 2 | D7 | 5 | 5 | PF0 OSC_IN (PF0) | I/O | FTf | - | I2C2_SDA, SPI2_NSS/I2S2_WS, TIM1_CH3N | OSC_IN |
| 3 | D6 | 6 | 6 | PF1 OSC_OUT (PF1) | O | FTf | - | I2C2_SCL, SPI2_SCK/I2S2_CK | OSC_OUT |
| 4 | E7 | 7 | 7 | NRST | I/O | RST | - | Device reset input/internal reset output (active low) | |
| - | - | - | 8 | PC0 | I/O | TTa | - | EVENTOUT, TIM1_CH1 | ADC1_IN6 |
| - | - | - | 9 | PC1 | I/O | TTa | - | EVENTOUT, TIM1_CH2 | ADC1_IN7 |
| - | - | - | 10 | PC2 | I/O | TTa | - | EVENTOUT, TIM1_CH3 | ADC1_IN8 |
| - | - | - | 11 | PC3 | I/O | TTa | - | EVENTOUT, TIM1_CH4, TIM1_BKIN2 | ADC1_IN9 |
| 6 | E6 | 8 | 12 | VSSA/VREF- | S | - | - | Analog ground/Negative reference voltage | |
| 5 | A6 | 9 | 13 | VDDA/VREF+ | S | - | - | Analog power supply/Positive reference voltage | |

Table 13. STM32F301x6/8 pin definitions (continued)

| Pin Number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| UQFN32 | WLCSP49 | LQFP48 | LQFP64 | | | | | | |
| - | - | - | 51 | PC10 | I/O | FT | - | EVENTOUT, SPI3_SCK/I2S3_CK, USART3_TX | - |
| - | - | - | 52 | PC11 | I/O | FT | - | EVENTOUT, SPI3_MISO/I2S3ext_SD, USART3_RX | - |
| - | - | - | 53 | PC12 | I/O | FT | - | EVENTOUT, SPI3_MOSI/I2S3_SD, USART3_CK | - |
| - | - | - | 54 | PD2 | I/O | FT | - | EVENTOUT | - |
| 26 | A3 | 39 | 55 | PB3 | I/O | FT | - | JTDO-TRACESWO, TIM2_CH2, TSC_G5_IO1, SPI3_SCK/I2S3_CK, USART2_TX, EVENTOUT | - |
| 27 | A4 | 40 | 56 | PB4 | I/O | FT | - | JTRST, TIM16_CH1, TSC_G5_IO2, SPI3_MISO/I2S3ext_SD, USART2_RX, TIM17_BKIN, EVENTOUT | - |
| 28 | B4 | 41 | 57 | PB5 | I/O | FT | - | TIM16_BKIN, I2C1_SMBAI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, EVENTOUT | - |
| 29 | C4 | 42 | 58 | PB6 | I/O | FTf | - | TIM16_CH1N, TSC_G5_IO3, I2C1_SCL, USART1_TX, EVENTOUT | - |
| 30 | D4 | 43 | 59 | PB7 | I/O | FTf | - | TIM17_CH1N, TSC_G5_IO4, I2C1_SDA, USART1_RX, EVENTOUT | - |

**Table 13. STM32F301x6/8 pin definitions (continued)**

| Pin Number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| UQFN32 | WLCSP49 | LQFP48 | LQFP64 | | | | | | |
| 31 | A5 | 44 | 60 | BOOT0 | I | B | - | Boot memory selection | |
| - | B5 | 45 | 61 | PB8 | I/O | FTf | - | TIM16_CH1, TSC_SYNC, I2C1_SCL, USART3_RX, TIM1_BKIN, EVENTOUT | - |
| - | C5 | 46 | 62 | PB9 | I/O | FTf | - | TIM17_CH1, I2C1_SDA, IR-OUT, USART3_TX, COMP2_OUT, EVENTOUT | - |
| 32 | D3 | 47 | 63 | VSS_1 | S | - | - | Digital ground | |
| "1" | B7 | 48 | 64 | VDD_1 | S | - | - | Digital power supply | |

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:

   - The speed should not exceed 2 MHz with a maximum load of 30 pF

   - These GPIOs must not be used as current sources (e.g. to drive an LED).

   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0366 reference manual.

2. Fast ADC channel.

3. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

**Table 14. Alternate functions for Port A**

| Port & pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS_AF | TIM2/TIM15/TIM16 /TIM17/EVENT | I2C3/TIM1/TIM2/TIM15 | I2C3/TIM15/TSC | I2C1/I2C2/TIM1/ TIM16/TIM17 | SPI2/I2S2/ SPI3/I2S3/Infrared | SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared | USART1/USART2/USART3/ GPCOMP6 | I2C3/GPCOMP2 /GPCOMP4/GPCOMP6 | TIM1/TIM15 | TIM2/TIM17 | TIM1 | TIM1 | - | - | EVENT |
| PA0 | - | TIM2 _CH1/ TIM2 _ETR | - | TSC _G1_IO1 | - | - | - | USART2 _CTS | - | - | - | - | - | - | - | EVENT OUT |
| PA1 | RTC _REFIN | TIM2 _CH2 | - | TSC _G1_IO2 | - | - | - | USART2 _RTS_D E | - | TIM15 _CH1N | - | - | - | - | - | EVENT OUT |
| PA2 | - | TIM2 _CH3 | - | TSC _G1_IO3 | - | - | - | USART2 _TX | COMP2 _OUT | TIM15 _CH1 | - | - | - | - | - | EVENT OUT |
| PA3 | - | TIM2 _CH4 | - | TSC _G1_IO4 | - | - | - | USART2 _RX | - | TIM15 _CH2 | - | - | - | - | - | EVENT OUT |
| PA4 | - | - | - | TSC _G2_IO1 | - | - | SPI3_NSS/ I2S3_WS | USART2 _CK | - | - | - | - | - | - | - | EVENT OUT |
| PA5 | - | TIM2 _CH1/ TIM2 _ETR | - | TSC _G2_IO2 | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| PA6 | - | TIM16 _CH1 | - | TSC _G2_IO3 | - | - | TIM1_BKIN | - | - | - | - | - | - | - | - | EVENT OUT |
| PA7 | - | TIM17 _CH1 | - | TSC _G2_IO4 | - | - | TIM1 _CH1N | - | - | - | - | - | - | - | - | EVENT OUT |
| PA8 | MCO | - | - | I2C3 _SCL | I2C2 _SMBAL | I2S2 _MCK | TIM1_CH1 | USART1 _CK | - | - | - | - | - | - | - | EVENT OUT |

Table 14. Alternate functions for Port A (continued)

| Port & pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS_AF | TIM2/TIM15/TIM16 /TIM17/EVENT | I2C3/TIM1/TIM2/TIM15 | I2C3/TIM15/TSC | I2C1/I2C2/TIM1/ TIM16/TIM17 | SPI2/I2S2/ SPI3/I2S3/Infrared | SPI2/I2S2/SPI3/ I2S3/TIM1/Infrared | USART1/USART2/USART3/ GPCOMP6 | I2C3/GPCOMP2 /GPCOMP4/GPCOMP6 | TIM1/TIM15 | TIM2/TIM17 | TIM1 | TIM1 | - | - | EVENT |
| PA9 | - | - | I2C3 _SMBAL | TSC _G4_IO1 | I2C2 _SCL | I2S3 _MCK | TIM1_CH2 | USART1 _TX | - | TIM15 _BKIN | TIM2 _CH3 | - | - | - | - | EVENT OUT |
| PA10 | - | TIM17 _BKIN | | TSC _G4_IO2 | I2C2 _SDA | SPI2_MIS O/I2S2ext _SD | TIM1_CH3 | USART1 _RX | COMP6 _OUT | - | TIM2 _CH4 | - | - | - | - | EVENT OUT |
| PA11 | - | - | - | - | - | SPI2_MO SI/I2S2 _SD | TIM1 _CH1N | USART1 _CTS | - | - | - | TIM1 _CH4 | TIM1 _BKIN2 | - | - | EVENT OUT |
| PA12 | - | TIM16 _CH1 | - | - | - | I2SCKIN | TIM1 _CH2N | USART1 _RTS_D E | COMP2 _OUT | - | - | TIM1 _ETR | - | - | - | EVENT OUT |
| PA13 | SWDAT-JTMS | TIM16 _CH1N | - | TSC _G4_IO3 | - | IR-OUT | - | USART3 _CTS | - | - | - | - | - | - | - | EVENT OUT |
| PA14 | SWCLK-JTCK | | - | TSC _G4_IO4 | I2C1 _SDA | - | TIM1_BKIN | USART2 _TX | - | - | - | - | - | - | - | EVENT OUT |
| PA15 | JTDI | TIM2_C H1/ TIM2_E TR | - | TSC _SYNC | I2C1 _SCL | - | SPI3_NSS/ I2S3_WS | USART2 _RX | - | TIM1 _BKIN | - | - | - | - | - | EVENT OUT |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$ = 25 °C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = $V_{DDA}$= 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

**Figure 9. Pin loading conditions**

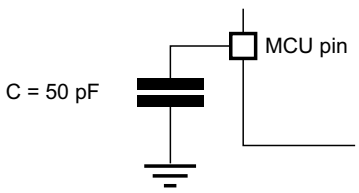
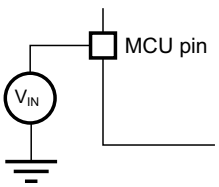



**Figure 10. Pin input voltage**



### I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

**I/O static current consumption**

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 54: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

**I/O dynamic current consumption**

In addition to the internal peripheral current consumption (see *Table 37: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 43*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 43. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions(1) | Min(2) | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0]=00 lower driving capability | - | 0.5 | 0.9 | µA |
| | | LSEDRV[1:0]=10 medium low driving capability | - | - | 1 | |
| | | LSEDRV[1:0]=01 medium high driving capability | - | - | 1.3 | |
| | | LSEDRV[1:0]=11 higher driving capability | - | - | 1.6 | |
| $g_m$ | Oscillator transconductance | LSEDRV[1:0]=00 lower driving capability | 5 | - | - | µA/V |
| | | LSEDRV[1:0]=10 medium low driving capability | 8 | - | - | |
| | | LSEDRV[1:0]=01 medium high driving capability | 15 | - | - | |
| | | LSEDRV[1:0]=11 higher driving capability | 25 | - | - | |
| $t_{SU(LSE)}$(3) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

*Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.*

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 52. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | 2 level A |

## 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 53*

**Table 53. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 | -0 | NA | mA |
| | Injected current on PC0 pin (TTa pin) | -0 | +5 | |
| | Injected current PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA6, PA7, PC4, PB0, PB10, PB11, PB13 with induced leakage current on other pins from this group less than -100 µA or more than +100 µA | -5 | +5 | |
| | Injected current on any other TT, FT and FTf pins | -5 | NA | |
| | Injected current on all other TC, TTa and RESET pins | -5 | +5 | |

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

**Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port**

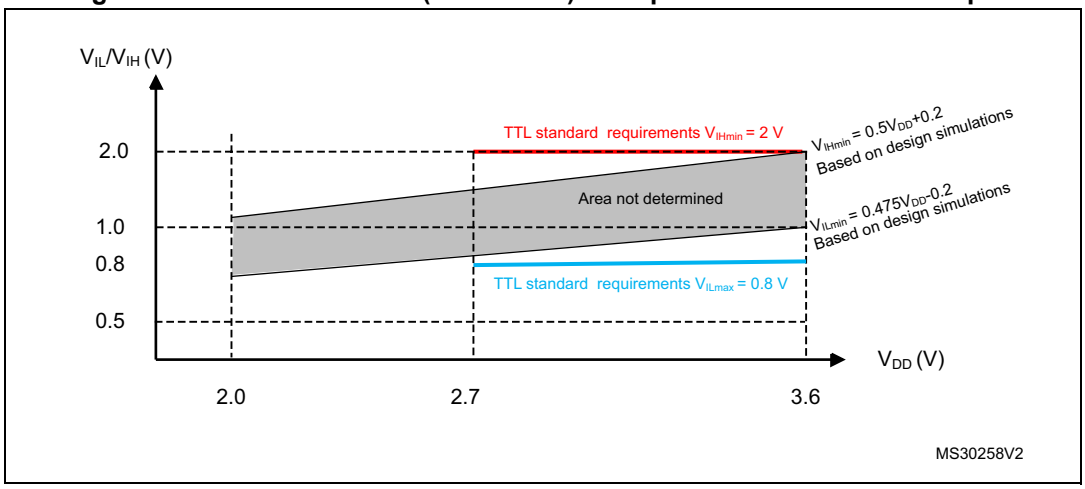
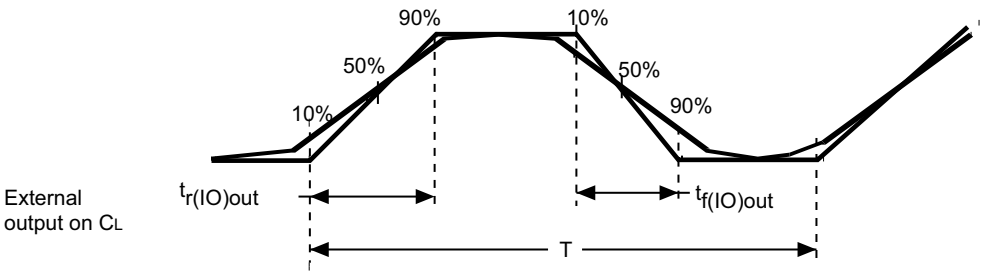


**Figure 23. I/O AC characteristics definition**




Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by $C_L$ (see note 1).

MS34942V1

1. See *Table 56: I/O AC characteristics*.

## 6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 54*).

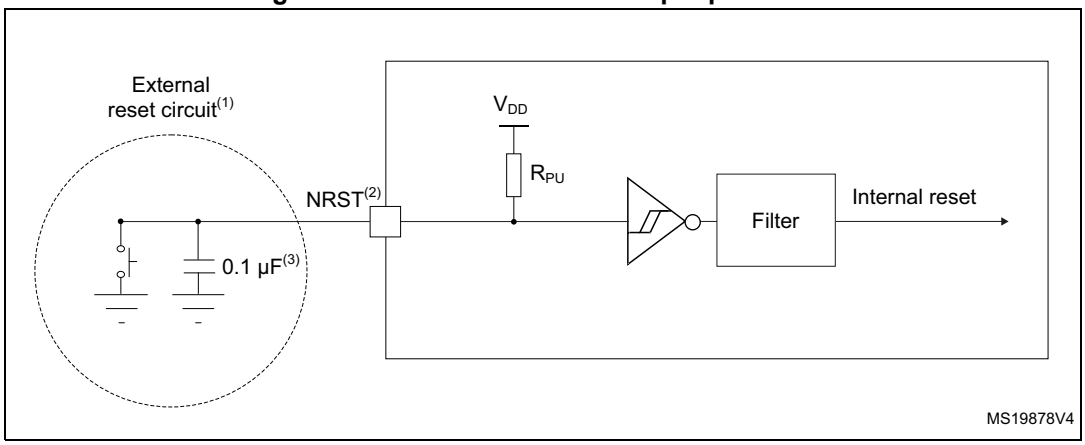
Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 23*.

**Table 57. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | - | - | - | $0.3V_{DD}$+ 0.07(1) | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | - | $0.445V_{DD}$+ 0.398(1) | - | - | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $V_{F(NRST)}$(1) | NRST Input filtered pulse | - | - | - | 100(1) | ns |
| $V_{NF(NRST)}$(1) | NRST Input not filtered pulse | - | 500(1) | - | - | ns |

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

**Figure 24. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 57*. Otherwise the reset will not be taken into account by the device.
3. The user must place the external capacitor on NRST as close as possible to the chip.

## 6.3.16 Timer characteristics

The parameters given in *Table 58* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 58. TIMx(1)(2) characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | - | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 13.9 | - | ns |
| | | $f_{TIMxCLK}$ = 144 MHz, x = 1, 15,16, 17 | 6.95 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | - | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 72 MHz | 0 | 36 | MHz |
| $Res_{TIM}$ | Timer resolution | TIMx (except TIM2) | - | 16 | bit |
| | | TIM2 | - | 32 | |
| $t_{COUNTER}$ | 16-bit counter clock period | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | 0.0139 | 910 | µs |
| | | $f_{TIMxCLK}$ = 144 MHz, x= 1/15/16/17 | 0.0069 | 455 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72 MHz | - | 59.65 | s |
| | | $f_{TIMxCLK}$ = 144 MHz, x= 1/15/16/17 | - | 29.825 | s |

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design.

*Figure 30* illustrates the ADC current consumption as per the clock frequency in single-ended and differential modes.

**Figure 30. ADC typical current consumption in single-ended and differential modes**

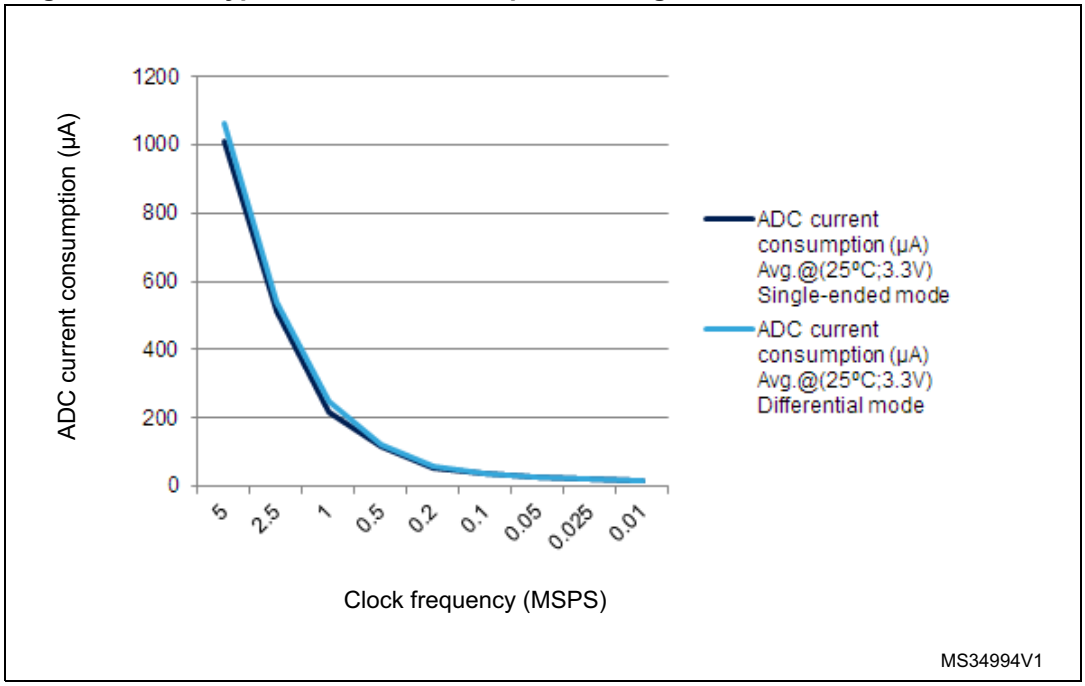



**Table 65. Maximum ADC $R_{AIN}$ (1)**

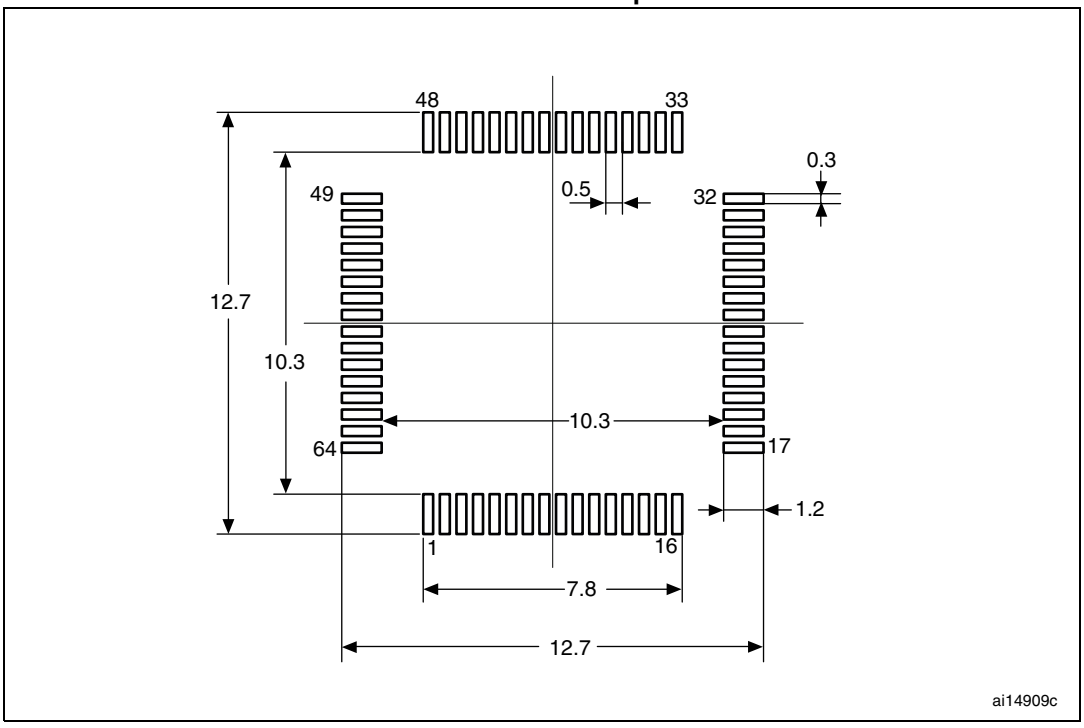
| Resolution | Sampling cycle @ 72 MHz | Sampling time [ns] @ 72 MHz | $R_{AIN}$ max (kΩ) | | |
|---|---|---|---|---|---|
| | | | Fast channels(2) | Slow channels | Other channels(3) |
| 12 bits | 1.5 | 20.83 | 0.018 | NA | NA |
| | 2.5 | 34.72 | 0.150 | NA | 0.022 |
| | 4.5 | 62.50 | 0.470 | 0.220 | 0.180 |
| | 7.5 | 104.17 | 0.820 | 0.560 | 0.470 |
| | 19.5 | 270.83 | 2.70 | 1.80 | 1.50 |
| | 61.5 | 854.17 | 8.20 | 6.80 | 4.70 |
| | 181.5 | 2520.83 | 22.0 | 18.0 | 15.0 |
| | 601.5 | 8354.17 | 82.0 | 68.0 | 47.0 |

**Table 77. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 40. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**

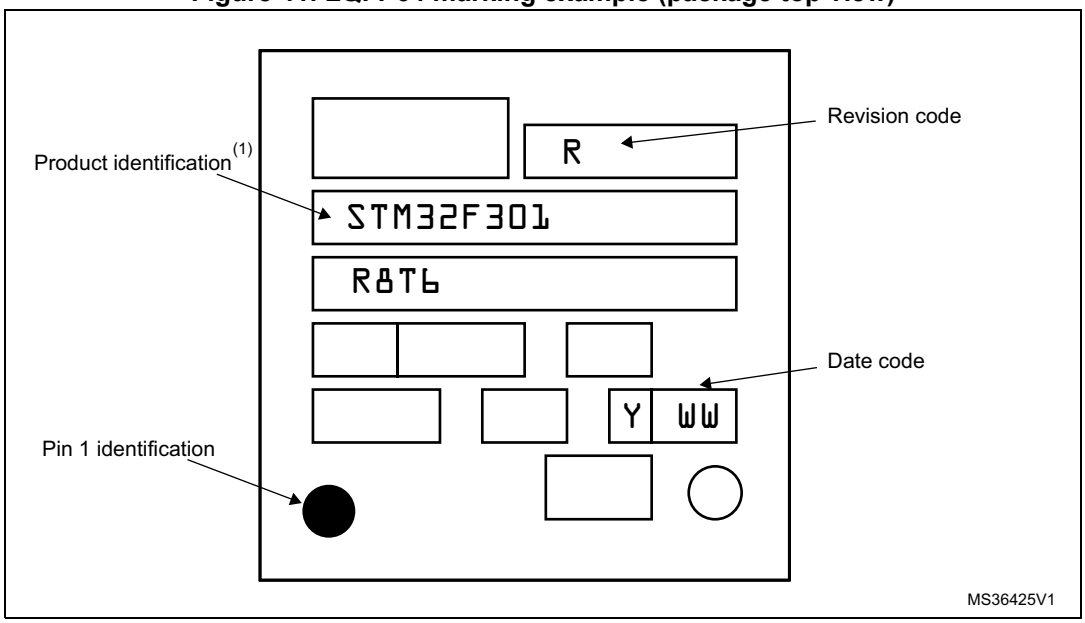



1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 41. LQFP64 marking example (package top view)**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 23: General operating conditions*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 80. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | °C/W |
| | **Thermal resistance junction-ambient** LQFP48 - 7 × 7 mm | 55 | |
| | **Thermal resistance junction-ambient** WCSP49 - 3.4 x 3.4 mm | 49 | |
| | **Thermal resistance junction-ambient** UFQFN32 - 5 x 5 mm | 37 | |

### 7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

# 8 Ordering information

**Table 81. Ordering information scheme**

Example: STM32 F 301 K 8 T 6 xxx

**Device family**

STM32 = ARM®-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

301 = STM32F301xx, 2.0 to 3.6 V operating voltage

**Pin count**

K = 32 pins

C = 48 or 49 pins

R = 64 pins

**Flash memory size**

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

**Package**

T = LQFP

Y= WLCSP

U= UFQFPN

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

**Options**

xxx = programmed parts

TR = tape and reel