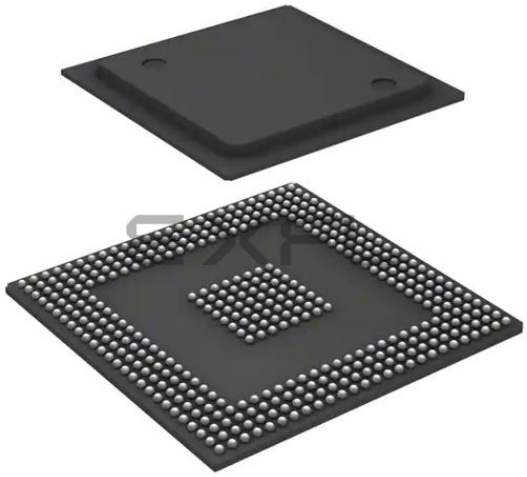

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	132MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	238
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	416-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc5567mvr132

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

Table 6. V_{RC} and POR Electrical Specifications (continued)

Spec	Characteristic		Symbol	Min.	Max.	Units
9	Absolute value of slew rate on power supply pins		—	—	50	V/ms
10	Required gain at Tj: $I_{DD} \div I_{VRCCTL}$ (@ $f_{sys} = f_{MAX}$) 6, 7, 8, 9	– 40° C 25° C 150° C	BETA[10]	40 45 55	— — 500	— — —

1 The internal POR signals are V_{POR15}, V_{POR33}, and V_{POR5}. On power up, assert $\overline{\text{RESET}}$ before the internal POR negates. $\overline{\text{RESET}}$ must remain asserted until the power supplies are within the operating conditions as specified in Table 9 DC Electrical Specifications. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.

2 V_{IL_S} (Table 9, Spec15) is guaranteed to scale with V_{DDEH6} down to V_{POR5}.

3 Supply full operating current for the 1.5 V supply when the 3.3 V supply reaches this range.

4 It is possible to reach the current limit during ramp up—do not treat this event as short circuit current.

5 At peak current for device.

6 Requires compliance with Freescale's recommended board requirements and transistor recommendations. Board signal traces/routing from the V_{RCCTL} package signal to the base of the external pass transistor and between the emitter of the pass transistor to the V_{DD} package signals must have a maximum of 100 nH inductance and minimal resistance (less than 1 Ω). V_{RCCTL} must have a nominal 1 µF phase compensation capacitor to ground. V_{DD} must have a 20 µF (nominal) bulk capacitor (greater than 4 µF over all conditions, including lifetime). Place high-frequency bypass capacitors consisting of eight 0.01 µF, two 0.1 µF, and one 1 µF capacitors around the package on the V_{DD} supply signals.

7 I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.

8 Refer to Table 1 for the maximum operating frequency.

9 Values are based on I_{DD} from high-use applications as explained in the I_{DD} Electrical Specification.

10 Represents the worst-case external transistor BETA. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).

3.7 Power-Up/Down Sequencing

Power sequencing between the 1.5 V power supply and V_{DDSYN} or the $\overline{\text{RESET}}$ power supplies is required if using an external 1.5 V power supply with V_{RC33} tied to ground (GND). To avoid power-sequencing, V_{RC33} must be powered up within the specified operating range, even if the on-chip voltage regulator controller is not used. Refer to Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," and Section 3.7.3, "Power-Down Sequence (VRC33 Grounded)."

Power sequencing requires that V_{DD33} must reach a certain voltage where the values are read as ones before the POR signal negates. Refer to Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33."

Although power sequencing is not required between V_{RC33} and V_{DDSYN} during power up, V_{RC33} must not lead V_{DDSYN} by more than 600 mV or lag by more than 100 mV for the V_{RC} stage turn-on to operate within specification. Higher spikes in the emitter current of the pass transistor occur if V_{RC33} leads or lags V_{DDSYN} by more than these amounts. The value of that higher spike in current depends on the board power supply circuitry and the amount of board level capacitance.

Furthermore, when all of the PORs negate, the system clock starts to toggle, adding another large increase of the current consumed by V_{RC33}. If V_{RC33} lags V_{DDSYN} by more than 100 mV, the increase in current consumed can drop V_{DD} low enough to assert the 1.5 V POR again. Oscillations are possible when the 1.5 V POR asserts and stops the system clock, causing the voltage on V_{DD} to rise until the 1.5 V POR negates again. All oscillations stop when V_{RC33} is powered sufficiently.

When powering down, V_{RC33} and V_{DDSYN} have no delta requirement to each other, because the bypass capacitors internal and external to the device are already charged. When not powering up or down, no delta between V_{RC33} and V_{DDSYN} is required for the V_{RC} to operate within specification.

There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up and power down varies depending on which supplies are powered.

Table 7 gives the pin state for the sequence cases for all pins with pad type pad_fc (fast type).

Table 7. Pin Status for Fast Pads During the Power Sequence

V_{DDE}	V_{DD33}	V_{DD}	POR	Pin Status for Fast Pad Output Driver pad_fc (fast)
Low	—	—	Asserted	Low
V_{DDE}	Low	Low	Asserted	High
V_{DDE}	Low	V_{DD}	Asserted	High
V_{DDE}	V_{DD33}	Low	Asserted	High impedance (Hi-Z)
V_{DDE}	V_{DD33}	V_{DD}	Asserted	Hi-Z
V_{DDE}	V_{DD33}	V_{DD}	Negated	Functional

Table 8 gives the pin state for the sequence cases for all pins with pad type pad_mh (medium type) and pad_sh (slow type).

Table 8. Pin Status for Medium and Slow Pads During the Power Sequence

V_{DDEH}	V_{DD}	POR	Pin Status for Medium and Slow Pad Output Driver pad_mh (medium) pad_sh (slow)
Low	—	Asserted	Low
V_{DDEH}	Low	Asserted	High impedance (Hi-Z)
V_{DDEH}	V_{DD}	Asserted	Hi-Z
V_{DDEH}	V_{DD}	Negated	Functional

The values in Table 7 and Table 8 do not include the effect of the weak-pull devices on the output pins during power up.

Before exiting the internal POR state, the voltage on the pins go to a high-impedance state until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak-pull devices
(up or down) are enabled as defined in the device reference manual. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}.

To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.

During initial power ramp-up, when V_{stby} is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until V_{DD} is applied. This current will not reoccur until V_{stby} is lowered below V_{stby} min. specification.

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

Table 12. FMPLL Electrical Specifications (continued)

(V_{DDSYN} = 3.0–3.6 V; V_{SS} = V_{SSSYN} = 0.0 V; T_A = T_L to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
19	CLKOUT period jitter, measured at f_{SYS} max: [15, 16] Peak-to-peak jitter (clock edge to clock edge) Long term jitter (averaged over a 2 ms interval)	C_{JITTER}	 — —	 5.0 0.01	% f_{CLKOUT}
20	Frequency modulation range limit [17] (do not exceed f_{sys} maximum)	C_{MOD}	0.8	2.4	$\%f_{SYS}$
21	ICO frequency $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ [18] $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$	f_{ico}	48	f_{MAX}	MHz
22	Predivider output frequency (to PLL)	f_{PREDIV}	4	20 [19]	MHz

1 Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.

2 The 8–20 MHz crystal or external reference values have PLLCFG[2] pulled low.

3 The 20–40 MHz crystal and external reference values have PLLCFG[2] pulled high, and the minimum frequency must be greater than 20 MHz. Use the 8–20 MHz setting (PLLCFG[2] pulled low) if a 20 MHz crystal or external reference is required. To exit RESET when using 40 MHz, set PLLCFG[2] to 1.

4 All internal registers retain data at 0 Hz.

5 Up to the maximum frequency rating of the device (refer to Table 1).

6 Loss of reference frequency is defined as the reference frequency detected internally, which transitions the PLL into self-clocked mode.

7 The PLL operates at self-clocked mode (SCM) frequency when the reference frequency falls below f_{LOR}. SCM frequency is measured on the CLKOUT ball with the divider set to divide-by-two of the system clock.
NOTE: In SCM, the MFD and PREDIV have no effect and the RFD is bypassed.

8 Use the EXTAL input high voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{extal} - V_{xtal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

9 Use the EXTAL input low voltage parameter when using the FlexCAN oscillator in crystal mode (no quartz crystals or resonators). ($V_{xtal} - V_{extal}$) must be ≥ 400 mV for the oscillator's comparator to produce the output clock.

10 I_{xtal} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded.

11 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

12 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, the lock time also includes the crystal startup time.

13 PLL is operating in 1:1 PLL mode.

14 V_{DDE} = 3.0–3.6 V.

15 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the jitter percentage for a given interval. CLKOUT divider is set to divide-by-two.

16 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of (jitter + Cmod).

17 Modulation depth selected must not result in f_{sys} value greater than the f_{sys} maximum specified value.

18 $f_{sys} = f_{ico} \div (2^{RFD})$.

19 Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) with the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).

3.10 eQADC Electrical Characteristics

Table 13. eQADC Conversion Specifications ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Minimum	Maximum	Unit
1	ADC clock (ADCLK) frequency [1]	F_{ADCLK}	1	12	MHz
2	Conversion cycles Differential Single ended	CC	 13 + 2 (15) 14 + 2 (16)	 13 + 128 (141) 14 + 128 (142)	ADCLK cycles
3	Stop mode recovery time [2]	T_{SR}	10	—	µs
4	Resolution [3]	—	1.25	—	mV
5	INL: 6 MHz ADC clock	INL6	–4	4	Counts [3]
6	INL: 12 MHz ADC clock	INL12	–8	8	Counts
7	DNL: 6 MHz ADC clock	DNL6	–3 [4]	3 [4]	Counts
8	DNL: 12 MHz ADC clock	DNL12	–6 [4]	6 [4]	Counts
9	Offset error with calibration	OFFWC	–4 [5]	4 [5]	Counts
10	Full-scale gain error with calibration	GAINWC	–8 [6]	8 [6]	Counts
11	Disruptive input injection current [7, 8, 9, 10]	I_{INJ}	–1	1	mA
12	Incremental error due to injection current. All channels are 10 kΩ < Rs <100 kΩ Channel under test has Rs = 10 kΩ, $I_{INJ} = I_{INJMAX}$, I_{INJMIN}	E_{INJ}	–4	4	Counts
13	Total unadjusted error (TUE) for single ended conversions with calibration [11, 12, 13, 14, 15]	TUE	–4	4	Counts

1 Conversion characteristics vary with F_{ADCLK} rate. Reduced conversion accuracy occurs at maximum F_{ADCLK} rate. The maximum value is based on 800 KS/s and the minimum value is based on 20 MHz oscillator clock frequency divided by a maximum 16 factor.

2 Stop mode recovery time begins when the ADC control register enable bits are set until the ADC is ready to perform conversions.

3 At $V_{RH} – V_{RL}$ = 5.12 V, one least significant bit (LSB) = 1.25, mV = one count.

4 Guaranteed 10-bit mono tonicity.

5 The absolute value of the offset error without calibration ≤ 100 counts.

6 The absolute value of the full scale gain error without calibration ≤ 120 counts.

7 Below disruptive current conditions, the channel being stressed has conversion values of: 0x3FF for analog inputs greater than V_{RH}, and 0x000 for values less than V_{RL}. This assumes that $V_{RH} \leq V_{DDA}$ and $V_{RL} \geq V_{SSA}$ due to the presence of the sample amplifier. Other channels are not affected by non-disruptive conditions.

8 Exceeding the limit can cause a conversion error on both stressed and unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.

9 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = – 0.3 V, then use the larger of the calculated values.

10 This condition applies to two adjacent pads on the internal pad.

11 The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to canceling errors.

12 TUE does not apply to differential conversions.

13 Measured at 6 MHz ADC clock. TUE with a 12 MHz ADC clock is: –16 counts < TUE < 16 counts.

14 TUE includes all internal device errors such as internal reference variation (75% Ref, 25% Ref).

15 Depending on the input impedance, the analog input leakage current (Table 9. DC Electrical Specifications, spec 35a) can affect the actual TUE measured on analog channels AN[12], AN[13], AN[14], AN[15].

3.11 H7Fa Flash Memory Electrical Characteristics

Table 14. Flash Program and Erase Specifications ($T_A = T_L$ to T_H)

Spec	Flash Program Characteristic	Symbol	Min.	Typical [1]	Initial Max. [2]	Max. [3]	Unit
3	Doubleword (64 bits) program time [4]	$T_{dwprogram}$	—	10	—	500	µs
4	Page program time [4]	$T_{pprogram}$	—	22	44 [5]	500	µs
7	16 KB block pre-program and erase time	$T_{16kpperase}$	—	265	400	5000	ms
9	48 KB block pre-program and erase time	$T_{48kpperase}$	—	345	400	5000	ms
10	64 KB block pre-program and erase time	$T_{64kpperase}$	—	415	500	5000	ms
8	128 KB block pre-program and erase time	$T_{128kpperase}$	—	500	1250	7500	ms
11	Minimum operating frequency for program and erase operations [6]	—	25	—	—	—	MHz

1 Typical program and erase times are calculated at 25 ^{o}C operating temperature using nominal supply values.

2 Initial factory condition: ≤ 100 program/erase cycles, 25 ^{o}C, using a typical supply voltage measured at a minimum system frequency of 80 MHz.

3 The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

5 Page size is 256 bits (8 words).

6 The read frequency of the flash can range up to the maximum operating frequency. There is no minimum read frequency condition.

Table 15. Flash EEPROM Module Life ($T_A = T_L$ to T_H)

Spec	Characteristic	Symbol	Min.	Typical [1]	Unit
1a	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range (T_J)	P/E	100,000	—	cycles
1b	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	P/E	1000	100,000	cycles
2	Data retention Blocks with 0–1,000 P/E cycles Blocks with 1,001–100,000 P/E cycles	Retention	 20 5	 — —	years

1 Typical endurance is evaluated at 25^{o} C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of typical endurance, refer to engineering bulletin EB619 Typical Endurance for Nonvolatile Memory.

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V) [1] (continued)

Spec	Pad	SRC / DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [4, 5] (ns)	Load Drive (pF)
3	Fast	00	3.1	2.7	10
		01		2.5	20
		10		2.4	30
		11		2.3	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9000	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 1.62–1.98 V; V_{DDEH} = 4.5–5.25 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and T_A = T_L to T_H.

2 This parameter is supplied for reference and is guaranteed by design (not tested).

3 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

4 The output delay and rise and fall are measured to 20% or 80% of the respective signal.

5 This parameter is guaranteed by characterization rather than 100% tested.

Table 18. Derated Pad AC Specifications (V_{DDEH} = 3.3 V, V_{DDE} = 3.3 V) [1]

Spec	Pad	SRC/DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [3, 5] (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	39	23	50
			120	87	200
		01	101	52	50
			188	111	200
		00	507	248	50
			597	312	200
2	Medium high voltage (MH)	11	23	12	50
			64	44	200
		01	50	22	50
			90	50	200
		00	261	123	50
			305	156	200
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9500	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 3.0–3.6 V; V_{DDEH} = 3.0–3.6 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and T_A = T_L to T_H.

2 This parameter is supplied for reference and guaranteed by design (not tested).

3 The output delay, and the rise and fall, are calculated to 20% or 80% of the respective signal.

4 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

5 This parameter is guaranteed by characterization rather than 100% tested.

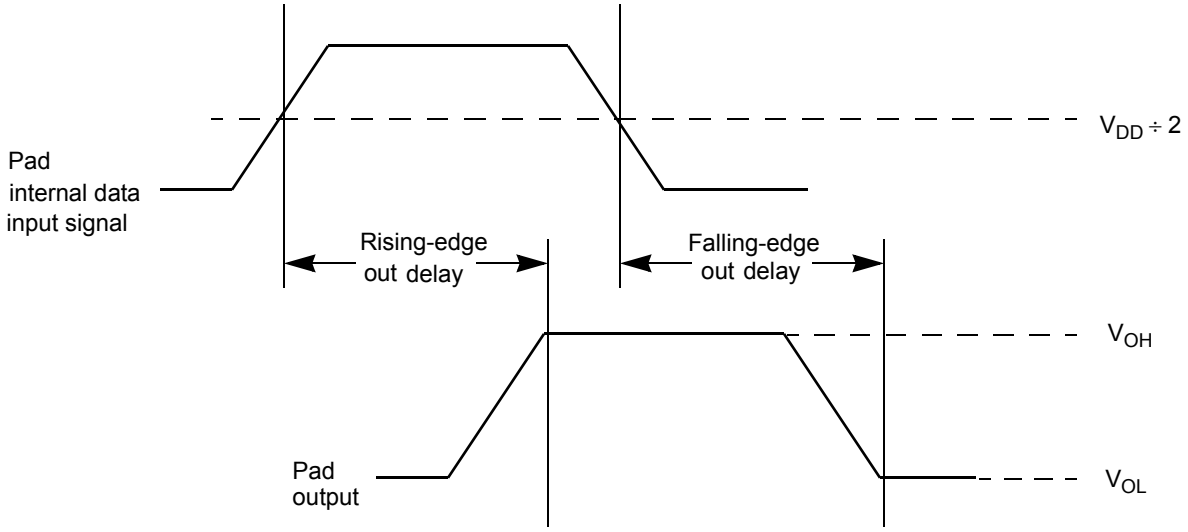


Figure 4. Pad Output Delay

3.13 AC Timing

3.13.1 Reset and Configuration Pin Timing

Table 19. Reset and Configuration Pin Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	$\overline{\text{RESET}}$ pulse width	t_{RPW}	10	—	t_{CYC}
2	$\overline{\text{RESET}}$ glitch detect pulse width	t_{GPW}	2	—	t_{CYC}
3	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ setup time to $\overline{\text{RSTOUT}}$ valid	t_{RCSU}	10	—	t_{CYC}
4	PLLCFG, BOOTCFG, WKPCFG, $\overline{\text{RSTCFG}}$ hold time from $\overline{\text{RSTOUT}}$ valid	t_{RCH}	0	—	t_{CYC}

1 Reset timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

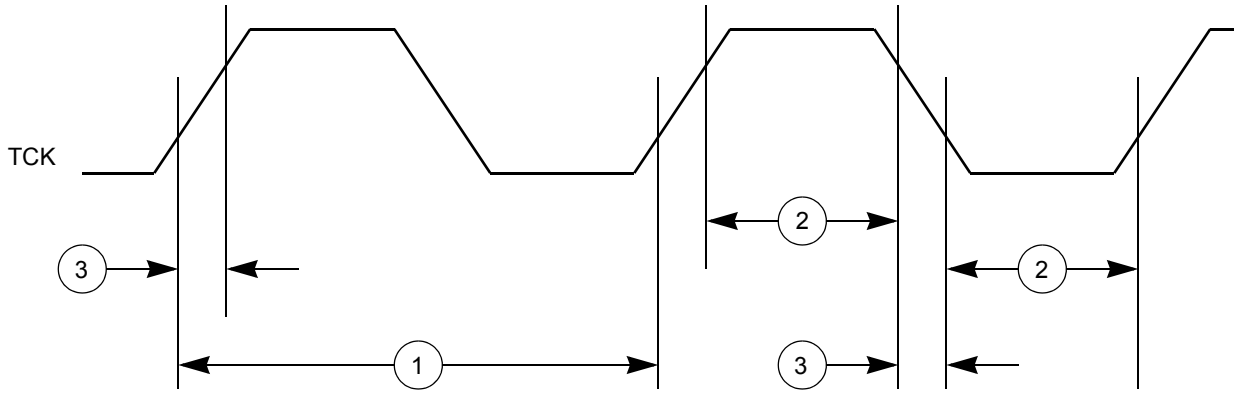


Figure 6. JTAG Test Clock Input Timing

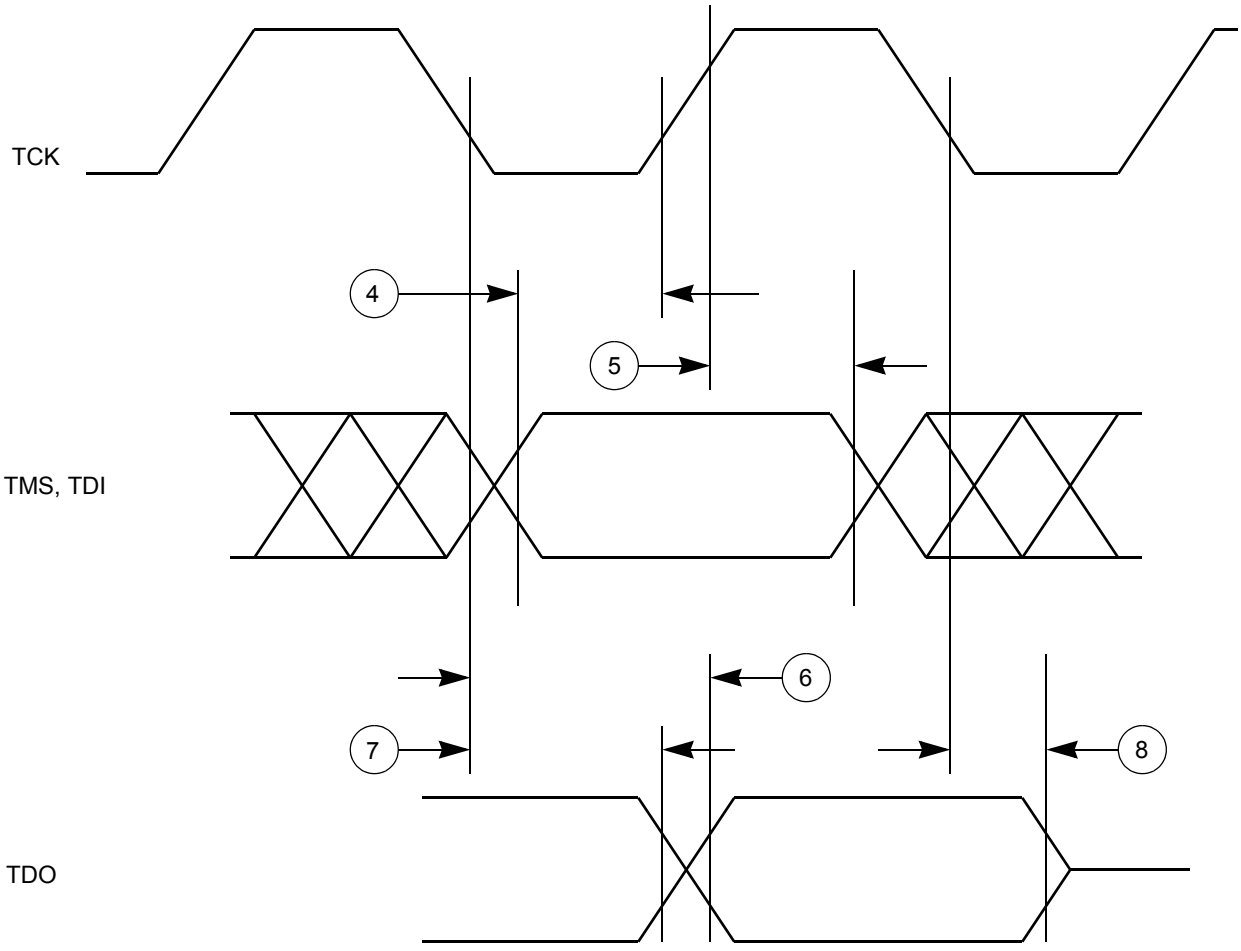


Figure 7. JTAG Test Access Port Timing

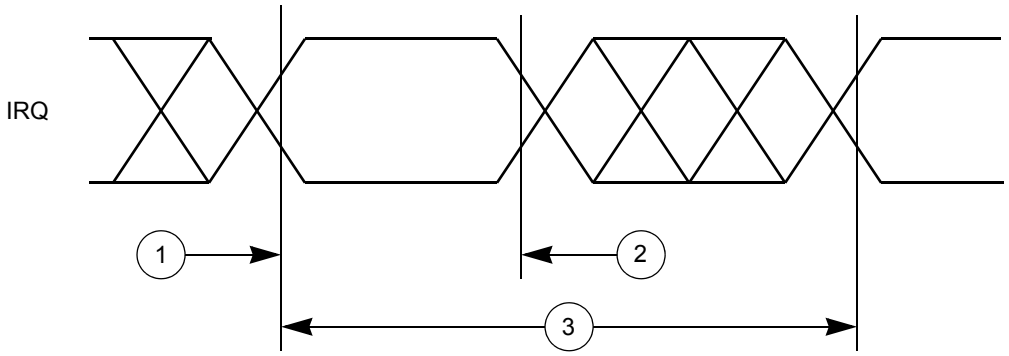


Figure 15. External Interrupt Timing

3.13.6 eTPU Timing

Table 24. eTPU Timing [1]

Spec	Characteristic	Symbol	Min.	Max	Unit
1	eTPU input channel pulse width	t_{ICPW}	4	—	t_{CYC}
2	eTPU output channel pulse width	t_{OCPW}	2 [2]	—	t_{CYC}

1 eTPU timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

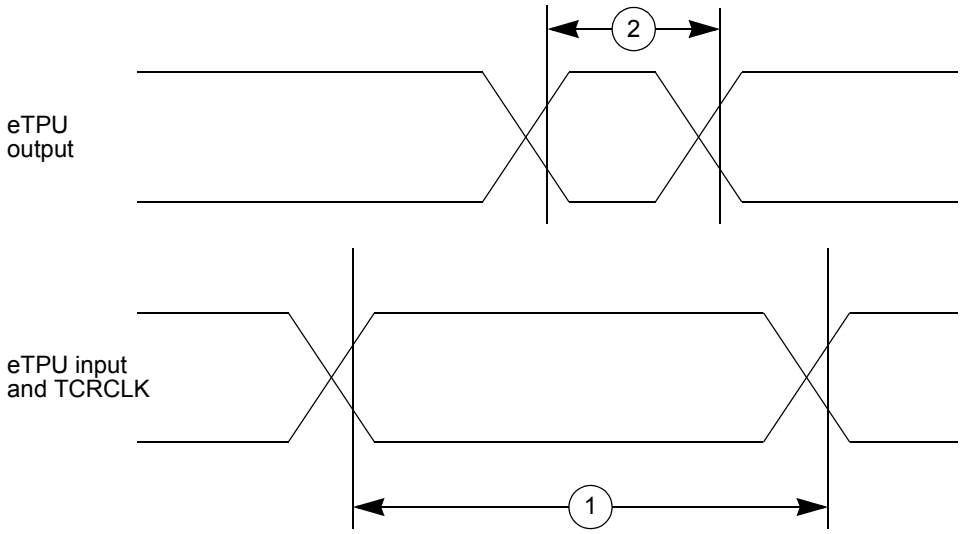


Figure 16. eTPU Timing

Table 26. DSPI Timing[1, 2] (continued)

Spec	Characteristic	Symbol	80 MHz		112 MHz		132 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
9	Data setup time for inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[7] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 20 2 –4 20	 — — — —	 20 2 3 20	 — — — —	 20 2 6 20	 — — — —	 ns ns ns ns
10	Data hold time for inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[7] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –4 7 21 –4	 — — — —	 –4 7 14 –4	 — — — —	 –4 7 12 –4	 — — — —	 ns ns ns ns
11	Data valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 5 25 18 5	 — — — —	 5 25 14 5	 — — — —	 5 25 13 5	 ns ns ns ns
12	Data hold time for outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –5 5.5 8 –5	 — — — —	 –5 5.5 4 –5	 — — — —	 –5 5.5 3 –5	 — — — —	 ns ns ns ns

1 All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate. DSPI timing is specified at: V_{DDEH} = 3.0–5.25 V;T_A = T_L to T_H; and CL = 50 pF with SRC = 0b11.

2 Speed is the nominal maximum frequency. Max. speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 135 MHz parts allow for 132 MHz system clock + 2% FM.

3 The minimum SCK cycle time restricts the baud rate selection for the given system clock rate. These numbers are calculated based on two MPC55xx devices communicating over a DSPI link.

4 The actual minimum SCK cycle time is limited by pad performance.

5 The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

6 The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

7 This number is calculated using the SMPL_PT field in DSPI_MCR set to 0b10.

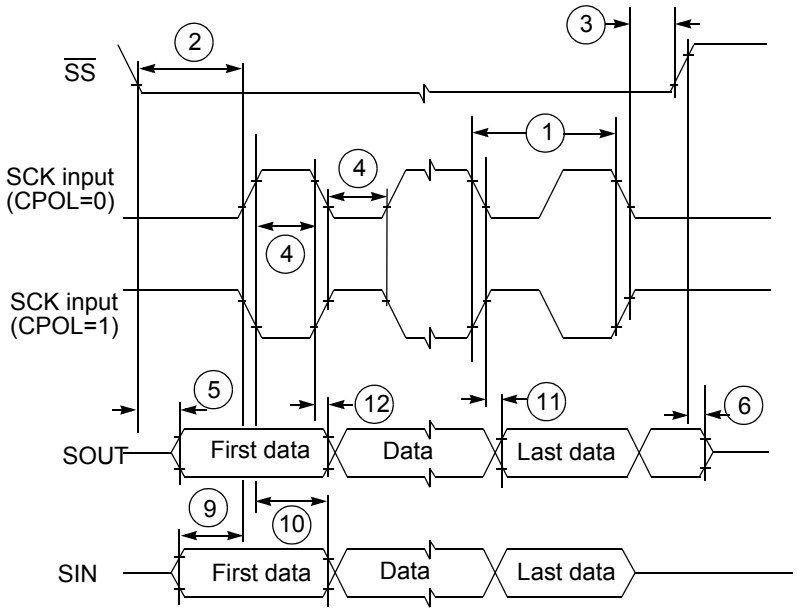


Figure 20. DSPI Classic SPI Timing—Slave, CPHA = 0

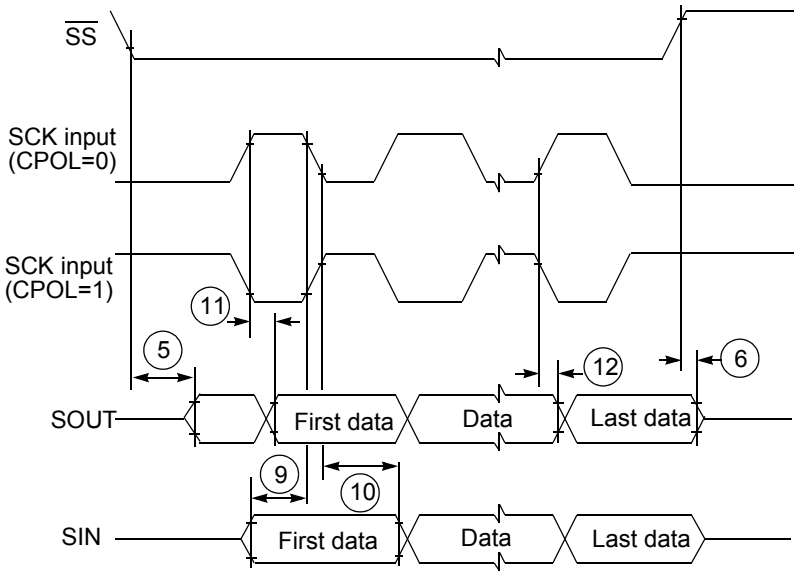


Figure 21. DSPI Classic SPI Timing—Slave, CPHA = 1

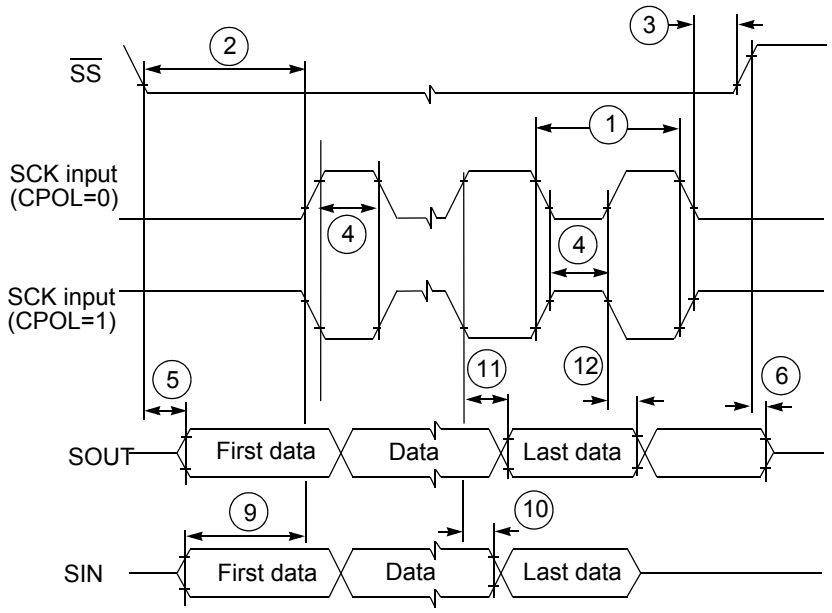


Figure 24. DSPI Modified Transfer Format Timing—Slave, CPHA = 0

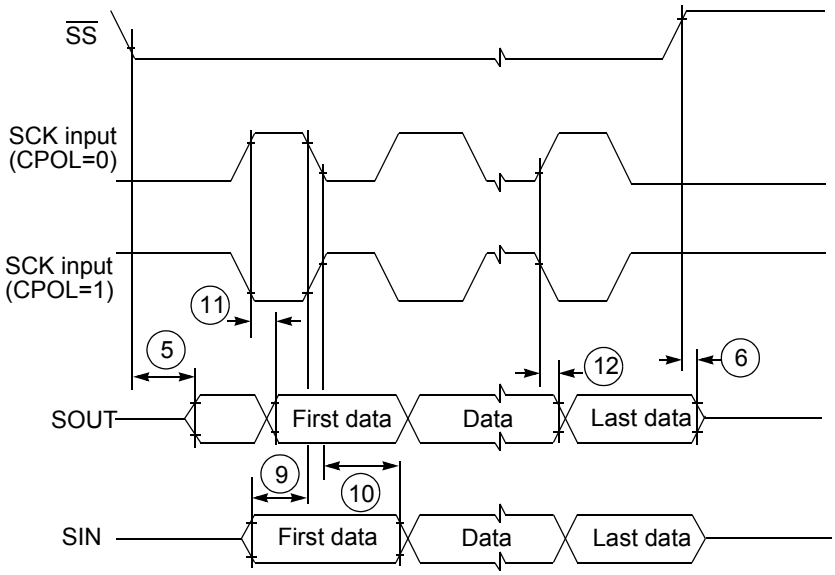


Figure 25. DSPI Modified Transfer Format Timing—Slave, CPHA = 1

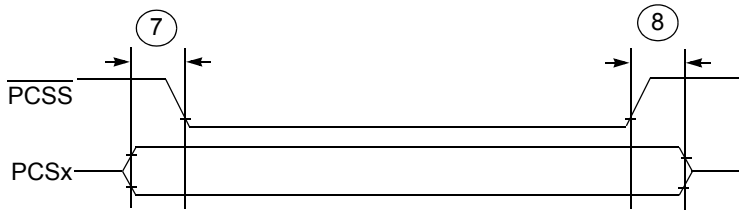


Figure 26. DSPI PCS Strobe ($\overline{\text{PCSS}}$) Timing

3.14.2 MII FEC Transmit Signal Timing FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, FEC_TX_CLK

The transmitter functions correctly up to the FEC_TX_CLK maximum frequency of 25 MHz plus one percent. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

The transmit outputs (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER) can be programmed to transition from either the rising- or falling-edge of TX_CLK, and the timing is the same in either case. These options allow the use of non-compliant MII PHYs.

Refer to the Fast Ethernet Controller (FEC) chapter of the device reference manual for details of this option and how to enable it.

Table 29 lists MII FEC transmit channel timings.

Table 29. MII FEC Transmit Signal Timing

Spec	Characteristic	Min.	Max	Unit
5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	25	ns
7	FEC_TX_CLK pulse-width high	35%	65%	FEC_TX_CLK period
8	FEC_TX_CLK pulse-width low	35%	65%	FEC_TX_CLK period

Figure 29 shows MII FEC transmit signal timings listed in Table 29.

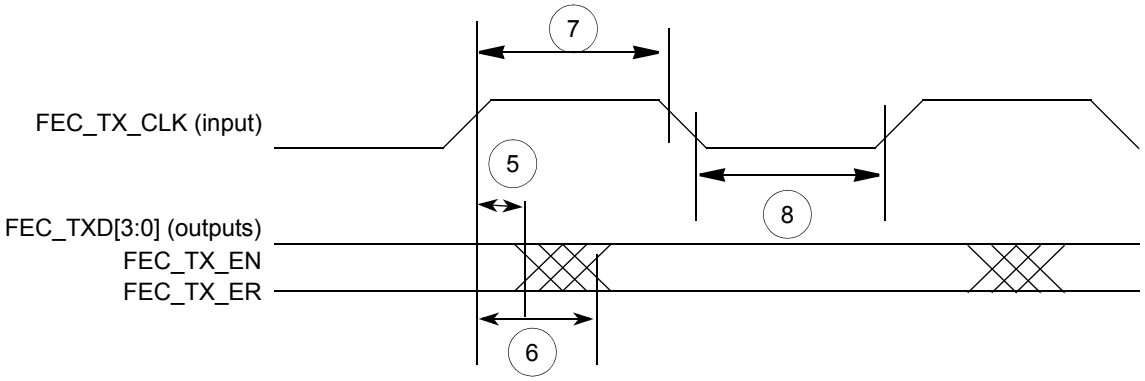


Figure 29. MII FEC Transmit Signal Timing Diagram

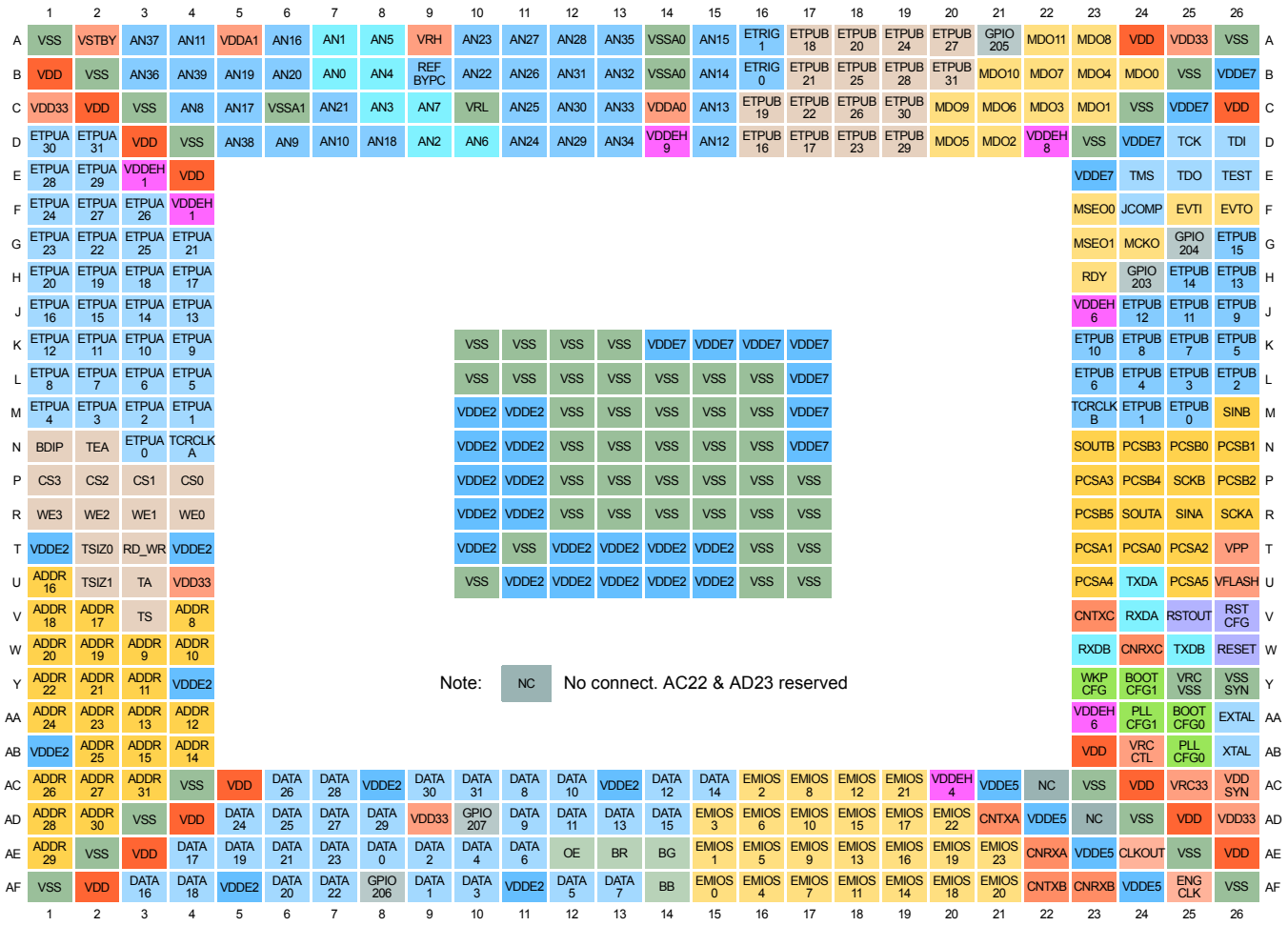
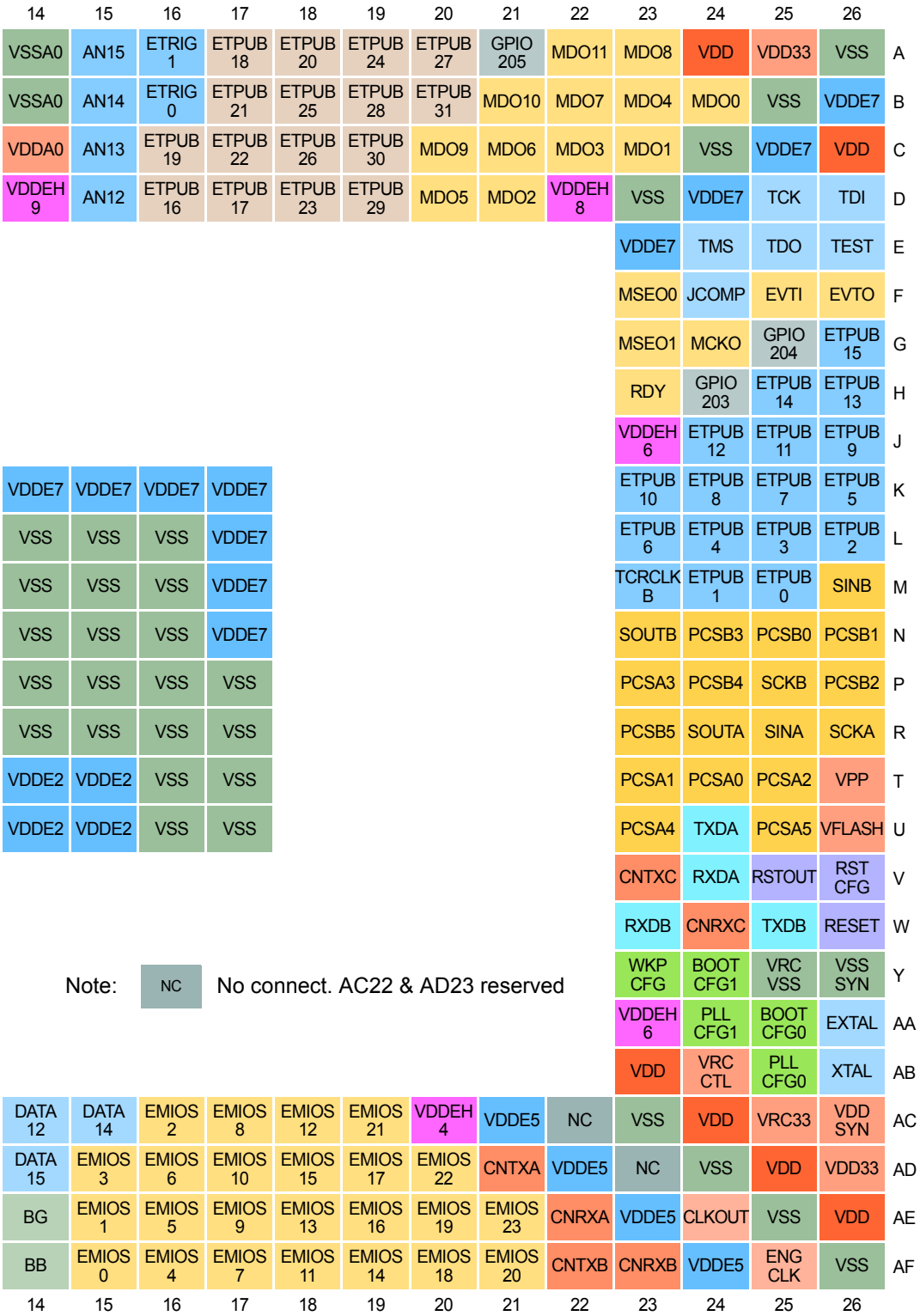


Figure 33. MPC5567 416 Package



14	15	16	17	18	19	20	21	22	23	24	25	26	
VSSA0	AN15	ETRIG 1	ETPUB 18	ETPUB 20	ETPUB 24	ETPUB 27	GPIO 205	MDO11	MDO8	VDD	VDD33	VSS	A
VSSA0	AN14	ETRIG 0	ETPUB 21	ETPUB 25	ETPUB 28	ETPUB 31	MDO10	MDO7	MDO4	MDO0	VSS	VDDE7	B
VDDA0	AN13	ETPUB 19	ETPUB 22	ETPUB 26	ETPUB 30	MDO9	MDO6	MDO3	MDO1	VSS	VDDE7	VDD	C
VDDEH 9	AN12	ETPUB 16	ETPUB 17	ETPUB 23	ETPUB 29	MDO5	MDO2	VDDEH 8	VSS	VDDE7	TCK	TDI	D
									VDDE7	TMS	TDO	TEST	E
									MSEO0	JCOMP	EVTI	EVTO	F
									MSEO1	MCKO	GPIO 204	ETPUB 15	G
									RDY	GPIO 203	ETPUB 14	ETPUB 13	H
									VDDEH 6	ETPUB 12	ETPUB 11	ETPUB 9	J
VDDE7	VDDE7	VDDE7	VDDE7						ETPUB 10	ETPUB 8	ETPUB 7	ETPUB 5	K
VSS	VSS	VSS	VDDE7						ETPUB 6	ETPUB 4	ETPUB 3	ETPUB 2	L
VSS	VSS	VSS	VDDE7						TCRCLKB	ETPUB 1	ETPUB 0	SINB	M
VSS	VSS	VSS	VDDE7						SOUTB	PCSB3	PCSB0	PCSB1	N
VSS	VSS	VSS	VSS						PCSA3	PCSB4	SCKB	PCSB2	P
VSS	VSS	VSS	VSS						PCSB5	SOUTA	SINA	SCKA	R
VDDE2	VDDE2	VSS	VSS						PCSA1	PCSA0	PCSA2	VPP	T
VDDE2	VDDE2	VSS	VSS						PCSA4	TXDA	PCSA5	VFLASH	U
									CNTXC	RXDA	RSTOUT	RST CFG	V
									RXDB	CNRXC	TXDB	RESET	W
									WKP CFG	BOOT CFG1	VRC VSS	VSS SYN	Y
									VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL	AA
									VDD	VRC CTL	PLL CFG0	XTAL	AB
DATA 12	DATA 14	EMIOS 2	EMIOS 8	EMIOS 12	EMIOS 21	VDDEH 4	VDDE5	NC	VSS	VDD	VRC33	VDD SYN	AC
DATA 15	EMIOS 3	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC	VSS	VDD	VDD33	AD
BG	EMIOS 1	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD	AE
BB	EMIOS 0	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Note: NC No connect. AC22 & AD23 reserved

Figure 35. MPC5567 416 Package Right Side (view 2 of 2)

Figure 36. MPC5567 416 Package

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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TITLE: 416 I/O, PBGA 27 X 27 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ARE10523D	REV: A
	CASE NUMBER: 1494–01	13 JUL 2005
	STANDARD: JEDEC MS–034 AAL–1	

Figure 38. MPC5567 416 TEPBGA Package (continued)

5 Revision History for the MPC5567 Data Sheet

The history of revisions made to this data sheet are described in this section. The changes are divided into each revision of this document, and are listed in sequential page number order.

5.1 Information Changed Between Revisions 1.0 and 2.0

The following table lists the substantive text changes made to paragraphs.

Table 32. Information changed between Rev 1.0 and 2.0

Section 3.7, "Power-Up/Down Sequencing"	Added the following paragraph in Section 3.7, "Power-Up/Down Sequencing": "During initial power ramp-up, when V_{stby} is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until VDD is applied. This current will not reoccur until V_{stby} is lowered below V_{stby} min. specification".
	Moved Figure 2 (fISTBY Worst-case Specifications) "ISTBY Worst-case Specifications" to Section 3.7, "Power-Up/Down Sequencing".
Section 3.8, "DC Electrical Specifications"	Removed the footnote "Figure 3 shows an illustration of the IDD_STBY values interpolated for these temperature values".
	Changed the footnote attached to IDD_STBY to "The current specification relates to average standby operation after SRAM has been loaded with data. For power up current see Section 3.7, "Power-Up/Down Sequencing",Figure 2 (fISTBY Worst-case Specifications)."
	In Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)) the Characteristic "Refer to Figure 3 for an interpolation of this data" changed to "RAM standby current".

5.2 Information Changed Between Rev. 0.0 and 1.0

The following table lists the global changes incorporated throughout the document, and substantive text changes made to paragraphs.

Table 34. Global and Text Changes Between Rev. 0.0 and 1.0

Location	Description of Change
Global Changes	

	• Starting at the third paragraph and throughout the document, replaced:
	  • kilobytes with KB
	  • megabytes with MB
	• Put overbars on the following signals: $\overline{\text{BDIP}}$, $\overline{\text{OE}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, $\overline{\text{RSTCFG}}$
	• Changed $\overline{\text{WE}}$[0:3]/$\overline{\text{BE}}$[0:3] to $\overline{\text{WE}}$/$\overline{\text{BE}}$[0:3].
	• Added the Fast Ethernet Controller (FEC) information.

Section 1, "Overview":	

Table 35. Table and Figure Changes Between Rev. 0.0 and 1.0

Location	Description of Changes
Figure 1 MPC5500 Family Part Numbers:	• Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text. • Changed Qualification Status by adding ‘, general market flow’ to the M designator, and added an ‘S’ designator with the description of ‘Fully spec. qualified, automotive flow. • Removed temperature code A for -55 C to 125 C.
Table 1 Orderable Part Numbers:	• Changed the 132 MHz maximum operating frequency to 135 MHz. • Reordered rows to group devices by lead-free package types in descending frequency order, and leaded package types. • Footnote 1 added that reads: All devices are PPC5567, rather than MPC5567 or SPC5567, until product qualifications are complete. Not all configurations are available in the PPC parts. • Footnote 2 added that reads:’ The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.’ • Footnote 3 added that reads: ‘Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 135 MHz parts allow for 132 MHz system clock + 2% FM.’
Table 2 Absolute Maximum Ratings:	• Deleted Spec 3, “Flash core voltage.” • Spec 12 “DC Input Voltage”: Deleted from second line‘. . .except for eTPUB15 and SINB (DSPI_B_SIN)’ leaving V_{DDEH} powered I/O pads. Deleted third line ‘V_{DDEH} powered by I/O pads (eTPUB15 and SINB), including the min and max values of -0.3 and 6.5 respectively, and deleted old footnote 7. • Spec 12 “DC Input Voltage”: Added footnote 8 to second line “V_{DDE} powered I/O pads” that reads: ‘Internal structures hold the input voltage less than the maximum voltage on all pads powered by the V_{DDE} supplies, if the maximum injection current specification is met (s mA for all pins) and V_{DDE} is within the operating voltage specifications. • Spec 14, column 2, changed: ‘V_{SS} differential voltage’ to ‘V_{SS} to V_{SSA} differential voltage.’ • Spec 15, column 2, changed: ‘V_{DD} differential voltage’ to ‘V_{DD} to V_{DDA} differential voltage.’ • Spec 21, Added the name of the spec, ‘*V_{RC33} to V_{DDSYN} differential voltage,’* as well as the name and cross reference to Table 9, *DC Electrical Specification*s, to which the Spec was moved. • Spec 26. Changed -40 to T_L in the Min. column. • Spec 28 “Maximum Solder Temperature”: Added two lines: Lead free (PbFree) and Leaded (SnPb) with maximum values of 260 C and 245 C respectively. • Footnote 1, added: ‘any of’ between ‘beyond’ and ‘the listed maxima.’ • Deleted footnote 2: ‘Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.’Spec 26 “Maximum Operating Temperature Range”: replaced -40 C with. • Footnote 6 (now footnote 5): Changed to the following sentence to the end, “Internal structures hold the input voltage greater than -1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than -0.6 V on eTPU[15] and on SINB during the internal power-on reset (POR) state.”
Table 3 MPC5567 Thermal Characteristics: Moved the Unit column to the far right column in the table.	
Table 4 EMI Testing Specifications:	• Changed the maximum operating frequency to from 132 to f_{MAX}. • Footnote 2: Deleted ‘Refer to Table 1 for the maximum operating frequency.’