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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	80 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c620-04-p

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 GENERAL DESCRIPTION

The PIC16C62X devices are 18 and 20-Pin ROM/ EPROM-based members of the versatile PICmicro[®] family of low cost, high performance, CMOS, fullystatic, 8-bit microcontrollers.

All PICmicro microcontrollers employ an advanced RISC architecture. The PIC16C62X devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16C62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC16C620A, PIC16C621A and PIC16CR620A have 96 bytes of RAM. The PIC16C622(A) has 128 bytes of RAM. Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16C62X adds two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low cost analog interface (e.g., battery chargers, threshold detectors, white goods controllers, etc).

PIC16C62X devices have special features to reduce external components, thus reducing system cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (Power-down) mode offers power savings. The user can wake-up the chip from SLEEP through several external and internal interrupts and RESET.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock- up.

A UV-erasable CERDIP-packaged version is ideal for code development while the cost effective One-Time-Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C62X midrange microcontroller families.

A simplified block diagram of the PIC16C62X is shown in Figure 3-1.

The PIC16C62X series fits perfectly in applications ranging from battery chargers to low power remote sensors. The EPROM technology makes

customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16C62X very versatile.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for the PIC16C5X can be easily ported to PIC16C62X family of devices (Appendix B). The PIC16C62X family fills the niche for users wanting to migrate up from the PIC16C5X family and not needing various peripheral features of other members of the PIC16XX mid-range microcontroller family.

1.2 Development Support

The PIC16C62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full-featured programmer. Third Party "C" compilers are also available.

NOTES:

FIGURE 4-4: DATA MEMORY MAP FOR THE PIC16C620/621

File Address	3		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	Osmanal		A0h
	Purpose		
6Eb	Register		
70n			
Į			_
7Fh	Donk 0	Dorld 1	FFh
	Dank U	Bank T	
Unimp	plemented data me	mory locations, r	ead as '0'.
Note 1:	Not a physical re	egister.	

FIGURE 4-5:

DATA MEMORY MAP FOR THE PIC16C622

File Address	3		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h			A0h
	General	General	7.011
	Purpose Register	Purpose Register	
	rtogiotor	rtogiotor	BFh
			C0h
7Fh			FFh
,,,,,	Bank 0	Bank 1	
Unimp	plemented data me	mory locations, re	ead as '0'.
Note 1:	Not a physical m	aistor	
NOLE T:	not a physical re	ะษารเษา.	

FIGURE 4-6: DATA MEMORY MAP FOR THE PIC16C620A/CR620A/621A

File Address	5		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	General Purpose Register		A0h
6Fh			
70h	General		F0h
7011	Purpose	Accesses	
7Fh	Register	1011-1711	FFh
	Bank 0	Bank 1	
Unimp	lemented data mer	nory locations, re	ad as '0'.
Note 1:	Not a physical re	gister.	

FIGURE 4-7: DATA MEMORY MAP FOR THE PIC16C622A

File Address	;		File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dn			
1En	014001		9En
1Fn	CMCON	VRCON	9Fn
20h	General	General	A0h
	Purpose	Purpose	
	Register	Register	BFh
			C0h
			0011
6Fh			– F0h
70h	General	Accesses	
	Register	70h-7Fh	EEh
/Fhl	Bank 0	Bank 1	
Unimp	elemented data me	mory locations, re	ead as '0'.
Note 1:	Not a physical re	egister.	

4.2.2.4 PIE1 Register

This register contains the individual enable bit for the comparator interrupt.

REGISTER 4-4:	PIE1 REGIS	STER (AD	DRESS 80	CH)				
	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
		CMIE	—	_	—	_		
	bit 7							bit 0
bit 7	Unimpleme	nted: Read	d as '0'					
bit 6	CMIE: Com	parator Inte	errupt Enable	e bit				
	1 = Enables 0 = Disables	the Compa the Comp	arator interru arator interr	upt upt				
bit 5-0	Unimpleme	nted: Read	d as '0'					
	Legend:							
	R = Readab	le bit	W = W	ritable bit	U = Unim	plemented	bit, read as '	0'
	- n = Value a	at POR	'1' = Bi	it is set	'0' = Bit i	s cleared	x = Bit is u	nknown

4.2.2.5 PIR1 Register

This register contains the individual flag bit for the comparator interrupt.

Note:	Interrupt flag bits get set when an interrupt
	condition occurs, regardless of the state of
	its corresponding enable bit or the global
	enable bit, GIE (INTCON<7>). User
	software should ensure the appropriate
	interrupt flag bits are clear prior to enabling
	an interrupt.

REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)

_I\ 4 -J.	FINTNEO			511)				
	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	CMIF		_	—	_	—	_
	bit 7							bit 0
bit 7	Unimplem	ented: Rea	d as '0'					
bit 6	CMIF: Com	nparator Inte	errupt Flag b	it				
	1 = Compa	rator input h	nas changed					
	0 = Compa	rator input h	nas not chan	ged				
bit 5-0	Unimplem	ented: Rea	d as '0'					
	Legend:							
	R = Reada	ble bit	W = W	ritable bit	U = Unim	plemented	bit, read as '	0'
	- n = Value	at POR	'1' = B	it is set	'0' = Bit is	s cleared	x = Bit is u	nknown

4.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-9. However, IRP is not used in the PIC16C62X.

A simple program to clear RAM location 20h-7Fh using indirect addressing is shown in Example 4-1.

EXAN	IPLE 4-	1: INI	DIRECT ADDRESSING
	movlw	0x20	;initialize pointer
	movwf	FSR	;to RAM
NEXT	clrf	INDF	clear INDF register;
	incf	FSR	;inc pointer
	btfss	FSR,7	;all done?
	goto	NEXT	;no clear next
			;yes continue
CONTI	NUE:		

FIGURE 4-9: DIRECT/INDIRECT ADDRESSING PIC16C62X



TABLE 5-1:PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
05h	PORTA		_		RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
85h	TRISA	_	_	_	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0	1 1111	1 1111
1Fh	CMCON	C2OUT	C1OUT	_	_	CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown

Note: Shaded bits are not used by PORTA.

6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- · Interrupt on overflow from FFh to 00h
- · Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

6.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before reenabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP, since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.



FIGURE 6-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER

Counter)	(PC-1	X PC	(PC+1)	PC+2	PC+3	PC+4	<u>PC+5</u> χ	PC+6
Instruction Fetch	1 1 1	MOVWF TMR	0MOVF TMR0,V	MOVF TMR0,V	MOVF TMR0,W	MOVF TMR0,V	MOVF TMR0,W	I
TMR0	T0 X	T0+1)	T0+2	I	NT0		NT0+1 \	NT0+2 \
Instruction	1 1 1	1 1 1	≜	≜	1	≜	↑	≜
Executed	1	1	Write TMR0	Read TMR0	Read TMR0	Read TMR0	Read TMR0	Read TMR0

6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.



FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

PIC16C62X

FIGURE 9-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP) Vdd Vdd D R R1 MCLR PIC16C62X С Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down. **2:** < 40 k Ω is recommended to make sure that voltage drop across R does not violate the device's electrical specification. **3:** R1 = 100Ω to 1 k Ω will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin

breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 9-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate RESET when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
 - **2:** Internal Brown-out Reset circuitry should be disabled when using this circuit.

FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



3: Resistors should be adjusted for the characteristics of the transistor.

FIGURE 9-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both high and low active RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

PIC16C62X

RETFIE	Return from Interrupt						
Syntax:	[label]	RETFIE	-				
Operands:	None						
Operation:	$TOS \rightarrow PC$, 1 $\rightarrow GIE$						
Status Affected:	None						
Encoding:	00	0000	0000	1001			
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.						
Words:	1						
Cycles:	2						
Example	RETFIE						
	After Inte	rrupt PC = GIE =	TOS 1				

RETLW	Return with Literal in W						
Syntax:	[<i>label</i>] RETLW k						
Operands:	$0 \leq k \leq 255$						
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC						
Status Affected:	None						
Encoding:	11 01xx kkkk kkkk						
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.						
Words:	1						
Cycles:	2						
Example	CALL TABLE;W contains table						
TABLE	;offset value • ;W now has table value •						
	ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ;						
	• RETLW kn ;End of table						
	Before Instruction						
	W = 0x07 After Instruction W = value of k8						
RETURN	Return from Subroutine						
Svntax:	[<i>label</i>] RETURN						
Operands:	None						
Operation:	$TOS \rightarrow PC$						
Status Affected:	None						
Encoding:	00 0000 0000 1000						
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.						
Words:	1						
Cycles:	2						
Example	RETURN						
	After Interrupt PC = TOS						

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of pre-compiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command-line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities, and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, time-keeping, and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high level source debugging with the MPLAB IDE.

11.6 MPLAB ASM30 Assembler, Linker, and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce it's object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- · Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- · MPLAB IDE compatibility

11.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

11.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high speed simulator is designed to debug, analyze and optimize time intensive DSP routines.

PIC16C62X

12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended (CONT.)

PIC16C62XA			Stand Opera	dard O ating te	perati empera	n g Con iture -4 -4	ditions (unless otherwise stated) $10^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial and $10^{\circ}C \leq TA \leq +125^{\circ}C$ for extended		
PIC16LC62XA			Stand Opera	Standard Operating Conditions (unless otherwise st Departing temperature -40° C \leq TA \leq +85°C for indust 0° C \leq TA \leq +70°C for common -40°C \leq TA \leq +125°C for extermine					
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
D022	ΔİWDT	WDT Current ⁽⁵⁾	—	6.0	10 12	μA μA	VDD = 4.0V (125°C)		
D022A	Δ IBOR	Brown-out Reset Current ⁽⁵⁾	—	75	125	μA	BOD enabled, VDD = 5.0V		
D023		Comparator Current for each Comparator ⁽⁵⁾	_	30	60	μA	VDD = 4.0V		
D023A	ΔIVREF	VREF Current ⁽³⁾	_	80	135	μA	VDD = 4.0V		
D022	Δ IWDT	WDT Current ⁽⁵⁾	—	6.0	10	μΑ	VDD=4.0V		
DOODA	41	Descent Descet Operation (5)		75	12	μA	$\frac{(125^{\circ}C)}{200} = 5.0$		
D022A		Brown-out Reset Current ^(e)		75	125	μΑ	BOD enabled, $VDD = 5.0V$		
D023	AICOMP	Comparator Current for each		30	60	μΑ	VDD - 4.0V		
D023A	Δ IVREF	VREF Current ⁽⁵⁾	_	80	135	μA	VDD = 4.0V		
1A	Fosc	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures		
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures		
		XT Oscillator Operating Frequency	0		4	MHz	All temperatures		
		HS Oscillator Operating Frequency	0	—	20	MHZ	All temperatures		
1A	Fosc	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures		
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures		
		HS Oscillator Operating Frequency	0	_	4 20	MHZ MHZ	All temperatures All temperatures		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

 $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40⁽⁷⁾ (Commercial) PIC16CR620A-40⁽⁷⁾ (Commercial)

DC CHARACTERISTICS Standard Operating Conditions (unless otherwise state Operating temperature 0°C ≤ TA ≤ +70°C for commerc					(unless otherwise stated) A ≤ +70°C for commercial		
Param No.	Sym	Characteristic	Min	Тур†	Мах	Unit	Conditions
	VIL	Input Low Voltage					
		I/O ports					
D030		with TTL buffer	Vss	—	0.8V 0.15Vdd	V	VDD = 4.5V to 5.5V, otherwise
D031		with Schmitt Trigger input	Vss		0.2VDD	V	
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	Vss	—	0.2Vdd	V	(Note 1)
D033		OSC1 (in XT and HS)	Vss	—	0.3VDD	V	
		OSC1 (in LP)	Vss	_	0.6Vdd - 1.0	V	
	Viн	Input High Voltage					
		I/O ports					
D040		with TTL buffer	2.0V	—	VDD	V	VDD = 4.5V to 5.5V, otherwise
D044		with Ochavitt Triansations t	0.25 VDD + 0.8		VDD		
D041					VDD		
D042		MCLR RA4/TUCKI		_	VDD	V	
D043		OSC1 (A1, HS and LP) OSC1 (in RC mode)		_	VDD	v	(Note 1)
D070	IPURB	PORTB Weak Pull-up Current	50	200	400	μА	$V_{DD} = 5.0V$. VPIN = Vss
	lil	Input Leakage Current ^(2, 3)					
		I/O ports (except PORTA)			±1.0	μA	VSS \leq VPIN \leq VDD, pin at hi-impedance
D060		PORTA	_	_	±0.5	μA	Vss \leq VPIN \leq VDD, pin at hi-impedance
D061		RA4/T0CKI	—	—	±1.0	μA	$Vss \le VPIN \le VDD$
D063		OSC1, MCLR	_	—	±5.0	μA	$Vss \leq VPIN \leq VDD,$ XT, HS and LP osc configuration
	Vol	Output Low Voltage					
D080		I/O ports	_	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C
		(2)	_		0.6	V	IOL = 1.2 mA, VDD = 4.5V, +125°C
	Vон	Output High Voltage ⁽³⁾					
D090		I/O ports (except RA4)	VDD-0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40° to +85°C
			VDD-0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, +125°C
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to +85°C
*0450	1/25	On an Duain Ulink Matterna	VDD-0.7	_		V	IOH = -1.0 mA, VDD = 4.5V, +125°C
"D150	VOD	Open Drain High Voltage			8.5	V	RA4 pin
		Output Pins					
D100	Cosc2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD; WDT enabled/disabled as specified.
 The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in bi-impedance state and tied to VDD or VSS.

 mode, with all I/O pins in hi-impedance state and tied to VDD or VSs.
 For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/ 2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

7: See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾		75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
11*	TosH2ck H	OSC1↑ to CLKOUT↑ ⁽¹⁾	_	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
12*	TckR	CLKOUT rise time ⁽¹⁾		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
13*	TckF	CLKOUT fall time ⁽¹⁾		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
14*	TckL2ioV	CLKOUT \downarrow to Port out valid ⁽¹⁾	_	—	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑ ⁽¹⁾	Tosc +200 ns Tosc +400 ns	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
16*	TckH2iol	Port in hold after CLKOUT $\uparrow^{(1)}$	0	—		ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	_	50	150 300	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
19*	TioV2osH	Port input valid to OSC1 [↑] (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
21*	TioF	Port output fall time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
22*	Tinp	RB0/INT pin high or low time	25 40	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
23	Trbp	RB<7:4> change interrupt high or low time	Тсү	—	—	ns	

TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

13.0 DEVICE CHARACTERIZATION INFORMATION

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution, while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.



FIGURE 13-1: IDD VS. FREQUENCY (XT MODE, VDD = 5.5V)

FIGURE 13-2: PIC16C622A IPD VS. VDD (WDT DISABLE)



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APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

- Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
- 2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
- 3. Data memory paging is slightly redefined. STATUS register is modified.
- Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
 Two instructions TRIS and OPTION are being phased out, although they are kept for compatibility with PIC16C5X.
- 5. OPTION and TRIS registers are made addressable.
- 6. Interrupt capability is added. Interrupt vector is at 0004h.
- 7. Stack size is increased to 8 deep.
- 8. RESET vector is changed to 0000h.
- RESET of all registers is revisited. Five different RESET (and wake-up) types are recognized. Registers are reset differently.
- 10. Wake-up from SLEEP through interrupt is added.
- 11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
- 12. PORTB has weak pull-ups and interrupt-onchange feature.
- 13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
- 14. FSR is made a full 8-bit register.
- 15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
- PCON STATUS register is added with a Poweron-Reset (POR) STATUS bit and a Brown-out Reset STATUS bit (BOD).
- 17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
- 18. PORTA inputs are now Schmitt Trigger inputs.
- 19. Brown-out Reset reset has been added.
- 20. Common RAM registers F0h-FFh implemented in bank1.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

- 1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to 0000h.

PIC16C62X

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