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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	·
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	·
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	·
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c620a-04e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 GENERAL DESCRIPTION

The PIC16C62X devices are 18 and 20-Pin ROM/ EPROM-based members of the versatile PICmicro[®] family of low cost, high performance, CMOS, fullystatic, 8-bit microcontrollers.

All PICmicro microcontrollers employ an advanced RISC architecture. The PIC16C62X devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two-stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC16C62X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC16C620A, PIC16C621A and PIC16CR620A have 96 bytes of RAM. The PIC16C622(A) has 128 bytes of RAM. Each device has 13 I/O pins and an 8-bit timer/counter with an 8-bit programmable prescaler. In addition, the PIC16C62X adds two analog comparators with a programmable on-chip voltage reference module. The comparator module is ideally suited for applications requiring a low cost analog interface (e.g., battery chargers, threshold detectors, white goods controllers, etc).

PIC16C62X devices have special features to reduce external components, thus reducing system cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (Power-down) mode offers power savings. The user can wake-up the chip from SLEEP through several external and internal interrupts and RESET.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock- up.

A UV-erasable CERDIP-packaged version is ideal for code development while the cost effective One-Time-Programmable (OTP) version is suitable for production in any volume.

Table 1-1 shows the features of the PIC16C62X midrange microcontroller families.

A simplified block diagram of the PIC16C62X is shown in Figure 3-1.

The PIC16C62X series fits perfectly in applications ranging from battery chargers to low power remote sensors. The EPROM technology makes

customization of application programs (detection levels, pulse generation, timers, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16C62X very versatile.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A for a detailed list of enhancements. Code written for the PIC16C5X can be easily ported to PIC16C62X family of devices (Appendix B). The PIC16C62X family fills the niche for users wanting to migrate up from the PIC16C5X family and not needing various peripheral features of other members of the PIC16XX mid-range microcontroller family.

1.2 Development Support

The PIC16C62X family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full-featured programmer. Third Party "C" compilers are also available.

		PIC16C620 ⁽³⁾	PIC16C620A ⁽¹⁾⁽⁴⁾	PIC16CR620A ⁽²⁾	PIC16C621 ⁽³⁾	PIC16C621A ⁽¹⁾⁽⁴⁾	PIC16C622 ⁽³⁾	PIC16C622A ⁽¹⁾⁽⁴⁾
Clock	Maximum Frequency of Operation (MHz)	20	40	20	20	40	20	40
Memory	EPROM Program Memory (x14 words)	512	512	512	1K	1K	2K	2K
	Data Memory (bytes)	80	96	96	80	96	128	128
Peripherals	Timer Module(s)	TMR0	TMR0	TMRO	TMR0	TMR0	TMR0	TMR0
	Comparators(s)	2	2	2	2	2	2	2
	Internal Reference Voltage	Yes						
Features	Interrupt Sources	4	4	4	4	4	4	4
	I/O Pins	13	13	13	13	13	13	13
	Voltage Range (Volts)	2.5-6.0	2.7-5.5	2.5-5.5	2.5-6.0	2.7-5.5	2.5-6.0	2.7-5.5
	Brown-out Reset	Yes						
	Packages	18-pin DIP, SOIC; 20-pin SSOP						

TABLE 1-1: PIC16C62X FAMILY OF DEVICES

All PICmicro[®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability. All PIC16C62X Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

2: For ROM parts, operation from 2.0V - 2.5V will require the PIC16LCR62XA parts.

3: For OTP parts, operation from 2.5V - 3.0V will require the PIC16LC62X part.

4: For OTP parts, operation from 2.7V - 3.0V will require the PIC16LC62XA part.

NOTES:

OPTION Register 4.2.2.2

The OPTION register is a readable and writable register, which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note:	To achieve a 1:1 prescaler assignment for
	TMR0, assign the prescaler to the WDT
	(PSA = 1).

REGISTER 4-2:	OPTION REGISTER (ADDRESS 81H)
---------------	-------------------------------

RBPU INTEDG TOCS TOSE bit 7 bit 7 RBPU: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual por bit 6 INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin bit 5 TOCS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT) bit 4 TOSE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0 0 = Increment on low-to-high transition on RA4/T0 bit 3 PSA: Prescaler Assignment bit	PSA t latch va DCKI pin DCKI pin	PS2	PS1	PS0 bit 0					
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0 = Increment on low-to-high transition on RA4/T0 bit 3 PSA : Prescaler Assignment bit	OCKI pin								
bit 3 PSA : Prescaler Assignment bit									
1 = Prescaler is assigned to the WDT	1 = Prescaler is assigned to the WDT								
0 = Prescaler is assigned to the Timer0 module									
bit 2-0 PS<2:0> : Prescaler Rate Select bits									
Bit Value TMR0 Rate WDT Rate									
000 1:2 1:1									
001 1:4 1:2									
101 1:64 1:32									
110 1:128 1:64									
111 1:256 1:128									

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Reading the port register reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-2 shows the effect of two sequential read-modify-write instructions (ex., ${\tt BCF}\,,\;\;{\tt BSF},\; etc.)$ on an I/O port

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-2: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

; Initial PORT settings:	PORTB<7:4> Inpu	ıts				
;	PORTB<3:0> Outp	puts				
; PORTB<7:6> have external pull-up and are not ; connected to other circuitry						
;						
;	PORT latch PO	ORT pins				
;						
	-					
BCF PORTB, 7	;01pp pppp 11	ipp pppp				
BCF PORTB, 6	;10pp pppp 11	lpp pppp				
BSF STATUS, RPO	;					
BCF TRISB, 7	;10pp pppp 11	lpp pppp				
BCF TRISB, 6	;10pp pppp 10)pp pppp				
;						
; Note that the user may have expected the pin						
; values to be 00pp pppp. The 2nd BCF caused						
; RB7 to be latched as the	e pin value (High)).				

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-7). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



FIGURE 5-7: SUCCESSIVE I/O OPERATION

TABLE 7-1 :	REGISTERS ASSOCIATED WITH COMPARATOR MODULE
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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
1Fh	CMCON	C2OUT	C10UT			CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1		CMIF		_	_			_	-0	-0
8Ch	PIE1	_	CMIE	_	_	_	_	_	_	-0	-0
85h	TRISA		_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as "0"

-

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC16C62X devices can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 9-1). The PIC16C62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 9-2).

FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 9-1 and Table 9-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC



TABLE 9-1:CAPACITOR SELECTION FOR
CERAMIC RESONATORS

R	anges Chara	~[]			
Mode	Freq	OSC1(C1)	OSC2(C2)		
ХТ	455 kHz 2.0 MHz 4.0 MHz	22 - 100 pF 15 - 68 pF 15 - 68 pF	82 - 100 pF 15 - 68 pF 15 - 68 pF		
HS	8.0 MHz 16.0 MHz 🔨	10-68 bF 10-22 pF	10 - 68 pF 10 - 22 pF		
Higher capacitance increases the stability of the oscil- lator but also increases the start-up time. These webes are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.					

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1(C1)	OSC2(C2)		
LP	32 kHz	68 - 100 pF	68 - 100 pF		
	200 kHz	15 - 30 pF	15 - 30 pF		
хт	100 kHz	68 - 150 pF	150 - 300 pF		
	2 MHz	15 - 30 pF	15 - 30 pF		
	4 MHz	15 - 30 pF	15 - 30 pF		
HS	8 MHz	15-30 pF	^V 15 - 30 pF		
	10 MHz	15-30 pF	15 - 30 pF		
	20 MHz 🔨	15-30 pF	15 - 30 pF		
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.					

9.3 RESET

The PIC16C62X differentiates between various kinds of RESET:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during SLEEP
- d) WDT Reset (normal operation)
- e) WDT wake-up (SLEEP)
- f) Brown-out Reset (BOR)

Some registers are not affected in any RESET condition Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset,

MCLR Reset, WDT Reset and MCLR Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different RESET situations as indicated in Table 9-2. These bits are used in software to determine the nature of the RESET. See Table 9-5 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 9-6.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See Table 12-5 for pulse width specification.





9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in RC mode with <u>PWRTE</u> bit erased (<u>PWRT</u> disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Poweron Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{\text{BOR}} = 0$, indicating that a brown-out has occurred. The $\overline{\text{BOR}}$ STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (VDD may have gone too low).

Oscillator Configuration	Powe	er-up	Brown-out Reset	Wake-up from SLEEP	
	PWRTE = 0	PWRTE = 1	Brown out Rooot		
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc	
RC	72 ms	_	72 ms	_	

TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS

	TABLE 9-2 :	STATUS/PCON BITS AND THEIR SIGNIFICANCE
--	--------------------	---

POR	BOR	то	PD				
0	Х	1	1	Power-on Reset			
0	Х	0	Х	Illegal, TO is set on POR			
0	Х	Х	0	Illegal, PD is set on POR			
1	0	Х	Х	Brown-out Reset			
1	1	0	u	WDT Reset			
1	1	0	0	WDT Wake-up			
1	1	u	u	MCLR Reset during normal operation			
1	1	1	0	MCLR Reset during SLEEP			

Legend: u = unchanged, x = unknown

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS ⁽¹⁾
83h	STATUS				TO	PD				0001 1xxx	000q quuu
8Eh	PCON	_	_				_	POR	BOR	0x	uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

TABLE 9-6: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS ⁽¹⁾
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	_	_	—	—	—	-0	-0
8Ch	PIE1	—	CMIE	_	_	_	—	_	_	-0	-0

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

9.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W register and STATUS register). This will have to be implemented in software.

Example 9-3 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 9-3:

- · Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- · Restores the W register

EXAMPLE 9-3: SAVING THE STATUS AND W REGISTERS IN RAM

MOVWF	W_TEMP	;copy W to temp register, ;could be in either bank
SWAPF	STATUS,W	;swap status to be saved into W
BCF	STATUS, RPO	;change to bank 0 regardless ;of current bank
MOVWF	STATUS_TEMP	;save status to bank 0 ;register
:		
:	(ISR)	
:		
SWAPF	STATUS_TEMP, W	;swap STATUS_TEMP register ;into W, sets bank to origi- nal ;state
MOVWF	STATUS	;move W into STATUS register
SWAPF	W_TEMP,F	;swap W_TEMP
SWAPF	W_TEMP,W	;swap W_TEMP into W

9.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit in the STATUS register is cleared, the TO bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSs with no external circuitry drawing current from the I/O pin and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSs for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

Note:	It should be noted that a RESET generated
	by a WDT time-out does not drive MCLR
	pin low.

9.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- 1. External RESET input on MCLR pin
- 2. Watchdog Timer Wake-up (if WDT was enabled)
- 3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. PD bit, which is set on power-up, is cleared when SLEEP is invoked. TO bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction after the SLEEP instruction after the instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4	4 Q1	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
CLKOUT(4)	Tost(2)/	\/	\/'\	'
INT pin		1	ı ı ı ı	1	I
INTE flag	\		I I		
(INTCON<1>)	·····/	Interrupt Latend	şy		
	<u>i</u>	(Note 2)	i		
(INTCON<7>)	Processor in	1		<u> </u>	<u> </u>
	SLEEP	1	I I	i	i i
INSTRUCTION FLOW		1	і і і і	1	1
PC X PC+1	X PC+2	X PC+2	X PC + 2	<u>x 0004h x</u>	0005h
$\begin{array}{c} \mbox{Instruction} \\ \mbox{fetched} \end{array} \Big\{ \begin{array}{c} \mbox{Inst}(\mbox{PC}) = \mbox{SLEEP} & \mbox{Inst}(\mbox{PC} + 1) \end{array} \right.$		Inst(PC + 2)	 	Inst(0004h)	Inst(0005h)
Instruction { Inst(PC - 1) SLEEP	1 1 1	Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)
Note 1: XT, HS or LP Oscillator mode 2: Tos⊤ = 1024Tosc (drawing n	e assumed. ot to scale) This	delay will not be	e there for RC	Osc mode.	

FIGURE 9-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT

3: GIE = '1' assumed. In this case, after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these Osc modes, but shown here for timing reference.

TABLE 10-2:	PIC16C62X INSTRUCTION SET
-------------	---------------------------

Mnemonic,		Description	Cycles		14-Bit	Opcode	9	Status	Notes	
Operands				MSb			LSb	Affected		
BYTE-ORIENTED FILE REGISTER OPERATIONS										
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2	
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2	
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2	
CLRW	-	Clear W	1	00	0001	0000	0011	Z		
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2	
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2	
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3	
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2	
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3	
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2	
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2	
MOVWF	f	Move W to f	1	00	0000	lfff	ffff			
NOP	-	No Operation	1	00	0000	0xx0	0000			
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2	
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2	
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2	
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2	
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2	
BIT-ORIENT	ED FIL	E REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2	
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2	
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3	
LITERAL A	ND COI	NTROL OPERATIONS	-					-	-	
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z		
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z		
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk			
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD		
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk			
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z		
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk			
RETFIE	-	Return from interrupt	2	00	0000	0000	1001			
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk			
RETURN	-	Return from Subroutine	2	00	0000	0000	1000			
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD		
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z		
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z		

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

PIC16C62X

INCFSZ	Increment f, Skip if 0	IORWF	Inclusive OR W with f
Syntax:	[label] INCFSZ f,d	Syntax:	[<i>label</i>] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (dest), skip if result = 0	Operation:	(W) .OR. (f) \rightarrow (dest)
Status Affected:	None	Status Affected:	Z
Encoding:	00 1111 dfff ffff	Encoding:	00 0100 dfff ffff
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.	Description:	Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
	If the result is 0, the next instruc-	Words:	1
	discarded. A NOP is executed	Cycles:	1
	instead making it a two-cycle	Example	IORWF RESULT, 0
	Instruction.		Before Instruction
vvoras:	1		$\begin{array}{rcl} RESULI &= & 0x13 \\ W &= & 0x91 \end{array}$
Cycles: Example	1(2) HERE INCFSZ CNT, 1 GOTO LOOP CONTINUE • •		After Instruction $\begin{array}{rcl} RESULT &= & 0x13 \\ W & = & 0x93 \\ Z & = & 1 \end{array}$
	Before Instruction	MOVLW	Move Literal to W
	PC = address HERE After Instruction	Syntax:	[<i>label</i>] MOVLW k
	CNT = CNT + 1	Operands:	$0 \le k \le 255$
	if $CNT = 0$, PC = address CONTINUE	Operation:	$k \rightarrow (W)$
	if $CNT \neq 0$,	Status Affected:	None
	PC = address HERE +1	Encoding:	11 00xx kkkk kkkk
IORLW	Inclusive OR Literal with W	Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.
Syntax:	[<i>label</i>] IORLW k	Words:	1
Operands:	$0 \le k \le 255$	Cycles:	1
Operation:	(W) .OR. $k \rightarrow$ (W)	Example	MOVLW 0x5A
Status Affected:	Z	·	After Instruction
Encoding:	11 1000 kkkk kkkk		W = 0x5A
Description:	The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.		
Words:	1		
Cycles:	1		
Example	IORLW 0x35		
	Before Instruction W = 0x9A		
	After Instruction		

W = Z =

0xBF 1

11.20 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/De-multiplexed and 16-bit Memory modes. The board includes 2 Mb external FLASH memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

11.21 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PICmicro microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 FLASH microcontroller serves as the master. All three micro-controllers are programmed with firmware to provide LIN bus communication.

11.22 PICkit[™] 1 FLASH Starter Kit

A complete "development system in a box", the PICkit FLASH Starter Kit includes a convenient multi-section board for programming, evaluation, and development of 8/14-pin FLASH PIC[®] microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the user's guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB[®] IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin FLASH PIC[®] Microcontrollers" Handbook and a USB Interface Cable. Supports all current 8/14-pin FLASH PIC microcontrollers, as well as many future planned devices.

11.23 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

11.24 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip's HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA[®] development kit
- microID development and rfLab[™] development software
- SEEVAL[®] designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high power IR driver, delta sigma ADC, and flow rate sensor

Check the Microchip web page and the latest Product Line Card for the complete list of demonstration and evaluation kits.

12.1 DC Characteristics: PIC16C62X-04 (Commercial, Industrial, Extended) PIC16C62X-20 (Commercial, Industrial, Extended) PIC16LC62X-04 (Commercial, Industrial, Extended)

PIC16C	62X		Stan Oper	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
PIC16L	C62X		Stand Oper Oper	Standard Operating Conditions (unless otherwise stated)Operating temperature -40° C \leq TA \leq +85°C for industrial and 0° C \leq TA \leq +70°C for commercial and -40° C \leq TA \leq +125°C for extendedOperating voltage VDD range is the PIC16C62X range.							
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions				
D001	Vdd	Supply Voltage	3.0		6.0	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5				
D001	Vdd	Supply Voltage	2.5	—	6.0	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5				
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	_	1.5*	—	V	Device in SLEEP mode				
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode				
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss	—	V	See section on Power-on Reset for details				
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss	—	V	See section on Power-on Reset for details				
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details				
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details				
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.3	V	BOREN configuration bit is cleared				
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.3	V	BOREN configuration bit is cleared				
D010	IDD	Supply Current ⁽²⁾	-	1.8	3.3	mA	Fosc = 4 MHz, Vdd = 5.5V, WDT disabled, XT mode, (Note 4)*				
			_	35	70	μA	Fosc = 32 kHz, VDD = 4.0V, WDT disabled, LP				
			-	9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V, WDT disabled, HS mode				
D010	IDD	Supply Current ⁽²⁾	-	1.4	2.5	mA	Fosc = 2.0 MHz, VDD = 3.0V, WDT disabled, XT mode, (Note 4)				
			_	26	53	μA	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP mode				
D020	IPD	Power-down Current ⁽³⁾		1.0	2.5 15	μΑ μΑ	VDD=4.0V, WDT disabled (125°C)				
D020	IPD	Power-down Current ⁽³⁾	_	0.7	2	μA	VDD=3.0V, WDT disabled				

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended) (CONT.)

PIC16C62X/C62XA/CR62XA				$\begin{array}{llllllllllllllllllllllllllllllllllll$								
PIC16LC62X/LC62XA/LCR62XA				Standard Operating Conditions (unless otherwise stated)Operating temperature -40° C \leq TA \leq +85°C for industrial and 0° C \leq TA \leq +70°C for commercial and -40° C \leq TA \leq +125°C for extended								
Param. No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions					
	Vol	Output Low Voltage										
D080		I/O ports	_	_	0.6	v	IOL = 8.5 mA, VDD = 4.5V, -40° to +85°C					
			_	_	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C					
D083		OSC2/CLKOUT (RC only)	_	_	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40° to +85°C					
			_	_	0.6	V	IoL = 1.2 mA, VDD = 4.5V, +125°C					
	Vон	Output High Voltage ⁽³⁾										
D090		I/O ports (Except RA4)	VDD-0.7		_	v	ІОН = -3.0 mA, VDD = 4.5V, -40° to +85°С					
			VDD-0.7		_	V	Іон = -2.5 mA, Vdd = 4.5V, +125°C					
D092		OSC2/CLKOUT (RC only)	VDD-0.7	_	_	V	ІОН = -1.3 mA, VDD = 4.5V, -40° to +85°С					
			VDD-0.7	_	—	V	Іон = -1.0 mA, Vdd = 4.5V, +125°С					
	Vон	Output High Voltage ⁽³⁾										
D090		I/O ports (Except RA4)	VDD-0.7	_	—	V	ІОН = -3.0 mA, VDD = 4.5V, -40° to +85°C					
			VDD-0.7	_	_	V	ІОН = -2.5 mA, VDD = 4.5V, +125°C					
D092		OSC2/CLKOUT (RC only)	VDD-0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40° to +85°С					
			VDD-0.7		—	V	IOH = -1.0 mA, VDD = 4.5V, +125°С					
D150	Vod	Open-Drain High Voltage			10 8.5*	V	RA4 pin PIC16C62X, PIC16LC62X RA4 pin PIC16C62XA, PIC16LC62XA, PIC16CR62XA, PIC16LCR62XA					
D150	Vod	Open-Drain High Voltage			10 8.5*	V	RA4 pin PIC16C62X, PIC16LC62X RA4 pin PIC16C62XA, PIC16LC62XA, PIC16CR62XA, PIC16LCR62XA					
		Capacitive Loading Specs on Output Pins										
D100	COSC 2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.					
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF						
		Capacitive Loading Specs on Output Pins										
D100	COSC 2	OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.					
D101	Сю	All I/O pins/OSC2 (in RC mode)			50	pF						

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

*

12.8 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. TppS

2. 1990								
т								
F	Frequency	Т	Time					
Lowercase subscripts (pp) and their meanings:								
рр								
ck	CLKOUT	OSC	OSC1					
io	I/O port	tO	TOCKI					
mc	MCLR							
Uppercase letters and their meanings:								
S								
F	Fall	Р	Period					
н	High	R	Rise					
I	Invalid (Hi-impedance)	V	Valid					
L	Low	Z	Hi-Impedance					

FIGURE 12-11: LOAD CONDITIONS



13.0 DEVICE CHARACTERIZATION INFORMATION

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution, while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.



FIGURE 13-1: IDD VS. FREQUENCY (XT MODE, VDD = 5.5V)

FIGURE 13-2: PIC16C622A IPD VS. VDD (WDT DISABLE)



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PIC16C62X









18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



	Units	INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-007