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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c620a-20i-ss">https://www.e-xfl.com/product-detail/microchip-technology/pic16c620a-20i-ss</a>

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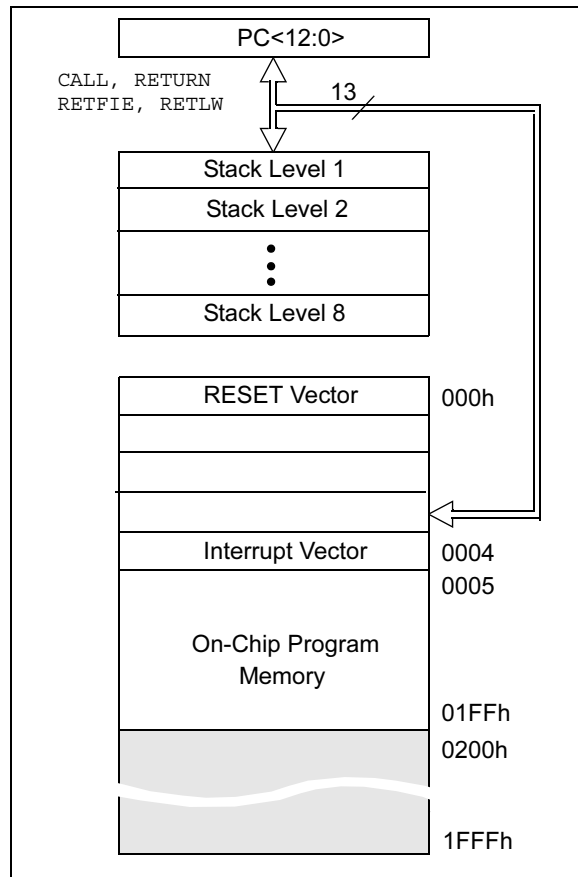
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## 4.0 MEMORY ORGANIZATION

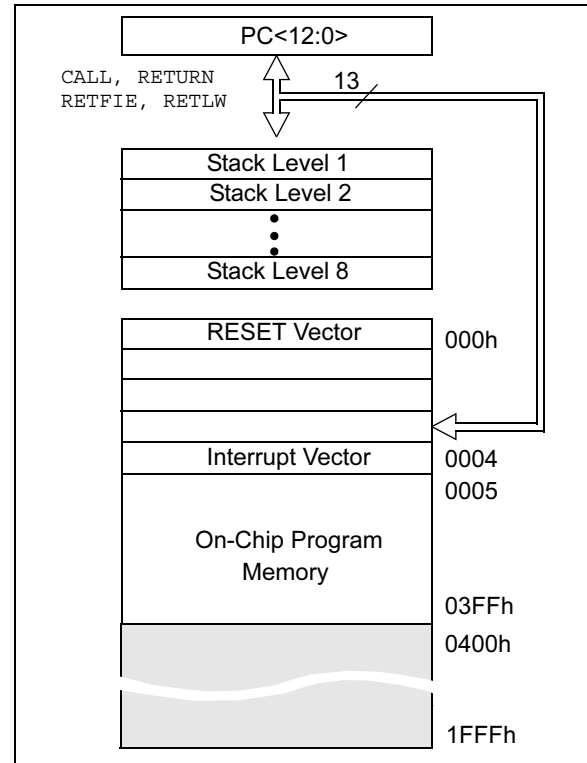
### 4.1 Program Memory Organization

The PIC16C62X has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 512 x 14 (0000h - 01FFh) for the PIC16C620(A) and PIC16CR620, 1K x 14 (0000h - 03FFh) for the PIC16C621(A) and 2K x 14 (0000h - 07FFh) for the PIC16C622(A) are physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 512 x 14 space (PIC16C(R)620(A)) or 1K x 14 space (PIC16C621(A)) or 2K x 14 space (PIC16C622(A)). The RESET vector is at 0000h and the interrupt vector is at 0004h (Figure 4-1, Figure 4-2, Figure 4-3).

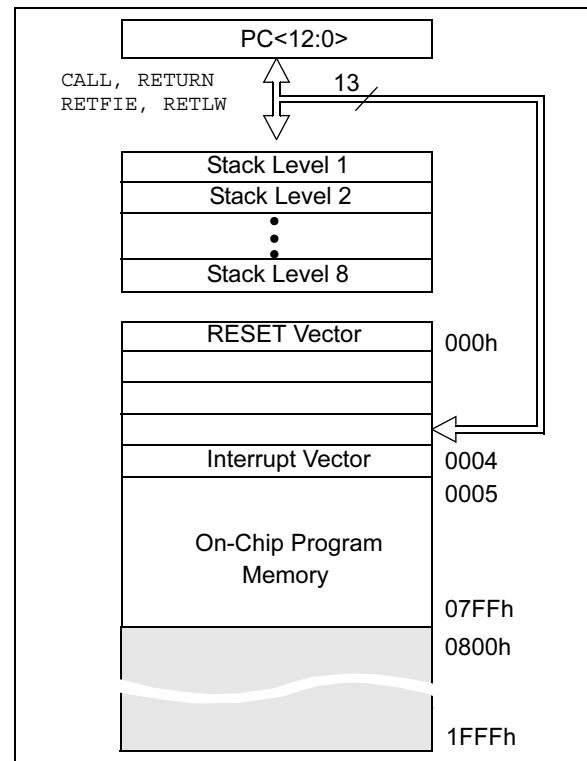
**FIGURE 4-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C620/PIC16C620A/ PIC16CR620A**



**FIGURE 4-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C621/PIC16C621A**



**FIGURE 4-3: PROGRAM MEMORY MAP AND STACK FOR THE PIC16C622/PIC16C622A**



# PIC16C62X

**FIGURE 4-6: DATA MEMORY MAP FOR THE PIC16C620A/CR620A/621A**

File Address			File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	General Purpose Register		A0h
6Fh			
70h	General Purpose Register	Accesses 70h-7Fh	F0h
7Fh			FFh
Bank 0		Bank 1	

☐ Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.

**FIGURE 4-7: DATA MEMORY MAP FOR THE PIC16C622A**

File Address			File Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh			8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh	CMCON	VRCON	9Fh
20h	General Purpose Register	General Purpose Register	A0h
			BFh
			C0h
6Fh			
70h	General Purpose Register	Accesses 70h-7Fh	F0h
7Fh			FFh
Bank 0		Bank 1	

☐ Unimplemented data memory locations, read as '0'.

**Note 1:** Not a physical register.

## 4.2.2.4 PIE1 Register

This register contains the individual enable bit for the comparator interrupt.

### REGISTER 4-4: PIE1 REGISTER (ADDRESS 8CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIE	—	—	—	—	—	—
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6 **CMIE:** Comparator Interrupt Enable bit  
1 = Enables the Comparator interrupt  
0 = Disables the Comparator interrupt
- bit 5-0 **Unimplemented:** Read as '0'

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
- n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

## 4.2.2.5 PIR1 Register

This register contains the individual flag bit for the comparator interrupt.

**Note:** Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

### REGISTER 4-5: PIR1 REGISTER (ADDRESS 0CH)

U-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
—	CMIF	—	—	—	—	—	—
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6 **CMIF:** Comparator Interrupt Flag bit  
1 = Comparator input has changed  
0 = Comparator input has not changed
- bit 5-0 **Unimplemented:** Read as '0'

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
- n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

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## 4.2.2.6 PCON Register

The PCON register contains flag bits to differentiate between a Power-on Reset, an external MCLR Reset, WDT Reset or a Brown-out Reset.

**Note:**  $\overline{\text{BOR}}$  is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if  $\overline{\text{BOR}}$  is cleared, indicating a brown-out has occurred. The BOR STATUS bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (by programming BODEN bit in the Configuration word).

### REGISTER 4-6: PCON REGISTER (ADDRESS 8Eh)

	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	POR	BOR
	bit 7						bit 0	
bit 7-2	<b>Unimplemented:</b> Read as '0'							
bit 1	<b>POR:</b> Power-on Reset STATUS bit							
	1 = No Power-on Reset occurred							
	0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)							
bit 0	<b>BOR:</b> Brown-out Reset STATUS bit							
	1 = No Brown-out Reset occurred							
	0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)							
Legend:								
R = Readable bit			W = Writable bit			U = Unimplemented bit, read as '0'		
- n = Value at POR			'1' = Bit is set			'0' = Bit is cleared      x = Bit is unknown		

**TABLE 5-3: PORTB FUNCTIONS**

Name	Bit #	Buffer Type	Function
RB0/INT	bit0	TTL/ST <sup>(1)</sup>	Input/output or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock pin.
RB7	bit7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data pin.

Legend: ST = Schmitt Trigger, TTL = TTL input

**Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.

**2:** This buffer is a Schmitt Trigger input when used in Serial Programming mode.

**TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	RBP <sub>U</sub>	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: u = unchanged, x = unknown

**Note 1:** Shaded bits are not used by PORTB.

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# PIC16C62X

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NOTES:

# PIC16C62X

## 9.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

### 9.4.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level for proper operation. To take advantage of the POR, just tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce an internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting".

### 9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, **PWRT**, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

The Power-up Time delay will vary from chip-to-chip and due to VDD, temperature and process variation. See DC parameters for details.

### 9.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

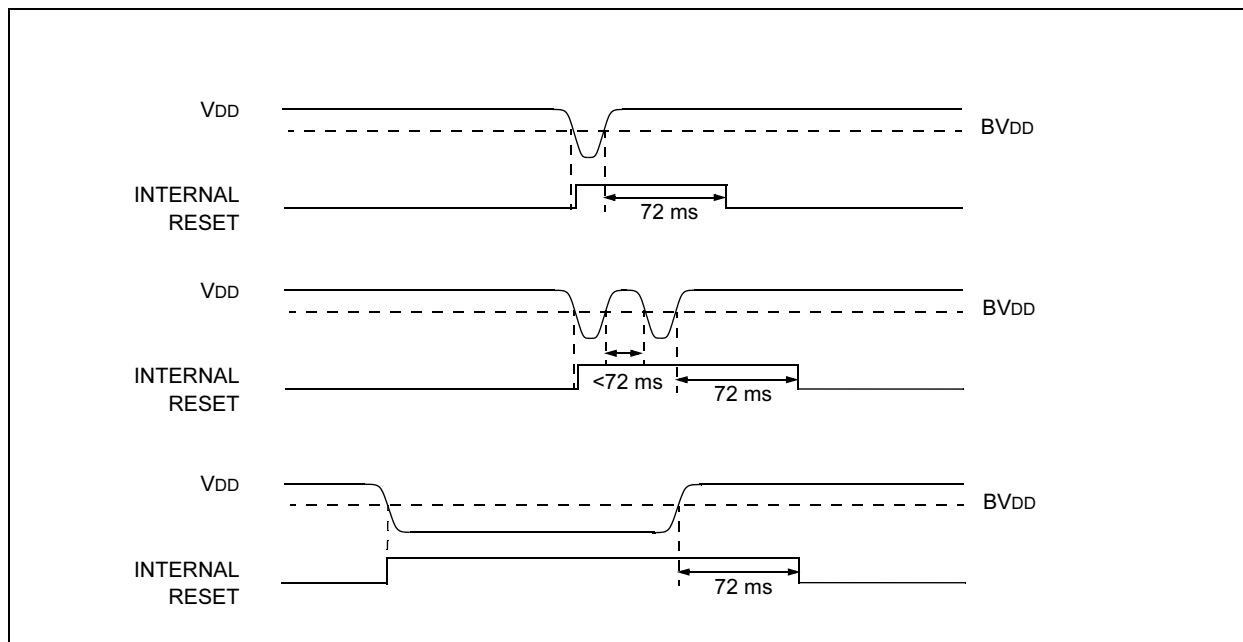
### 9.4.4 BROWN-OUT RESET (BOR)

The PIC16C62X members have on-chip Brown-out Reset circuitry. A configuration bit, **BODEN**, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V refer to VBOR parameter D005 (VBOR) for greater than parameter (TBOR) in Table 12-5. The brown-out situation will RESET the chip. A RESET won't occur if VDD falls below 4.0V for less than parameter (TBOR).

On any RESET (Power-on, Brown-out, Watchdog, etc.) the chip will remain in RESET until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms.

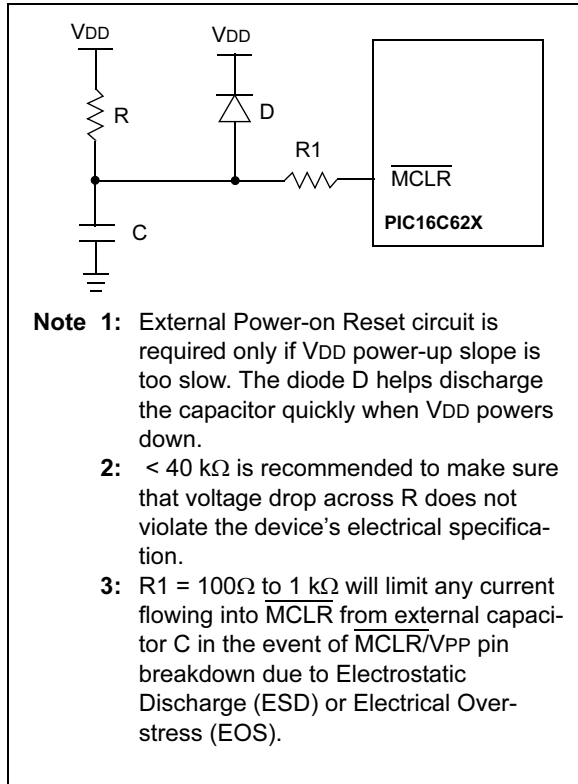
If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-Up Timer will execute a 72 ms RESET. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 9-7 shows typical Brown-out situations.

**FIGURE 9-7: BROWN-OUT SITUATIONS**

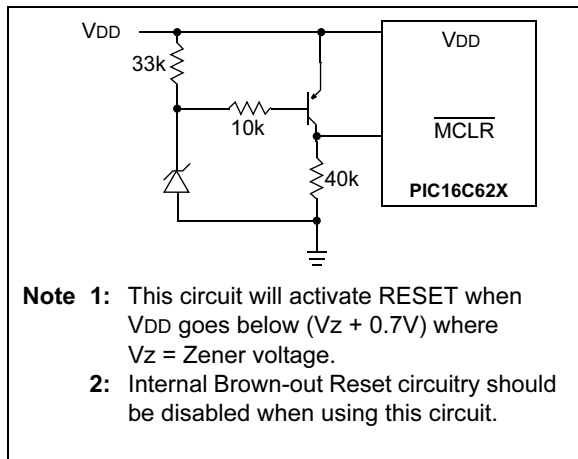


# PIC16C62X

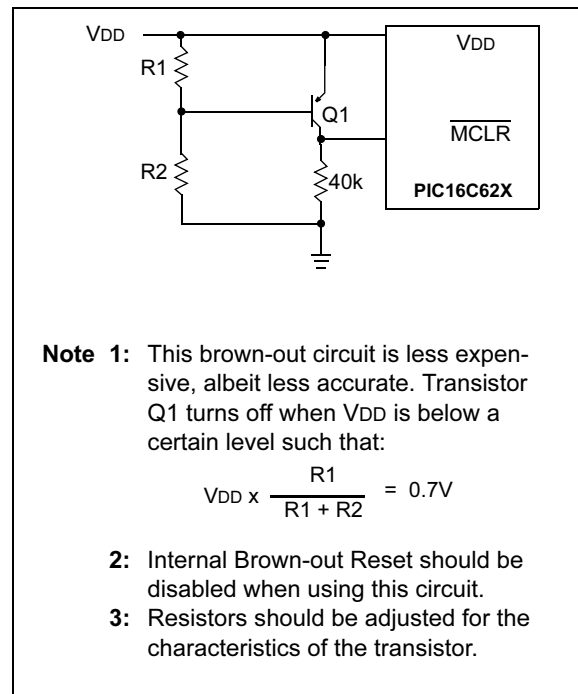
**FIGURE 9-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V<sub>DD</sub> POWER-UP)**



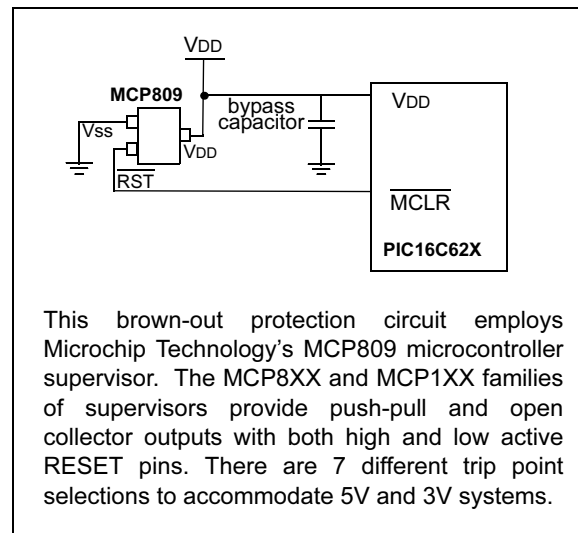
**FIGURE 9-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1**



**FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2**



**FIGURE 9-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3**



# PIC16C62X

## 9.5.1 RB0/INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered, either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before re-enabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.8 for details on SLEEP and Figure 9-18 for timing of wake-up from SLEEP through RB0/INT interrupt.

## 9.5.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 6.0.

## 9.5.3 PORTB INTERRUPT

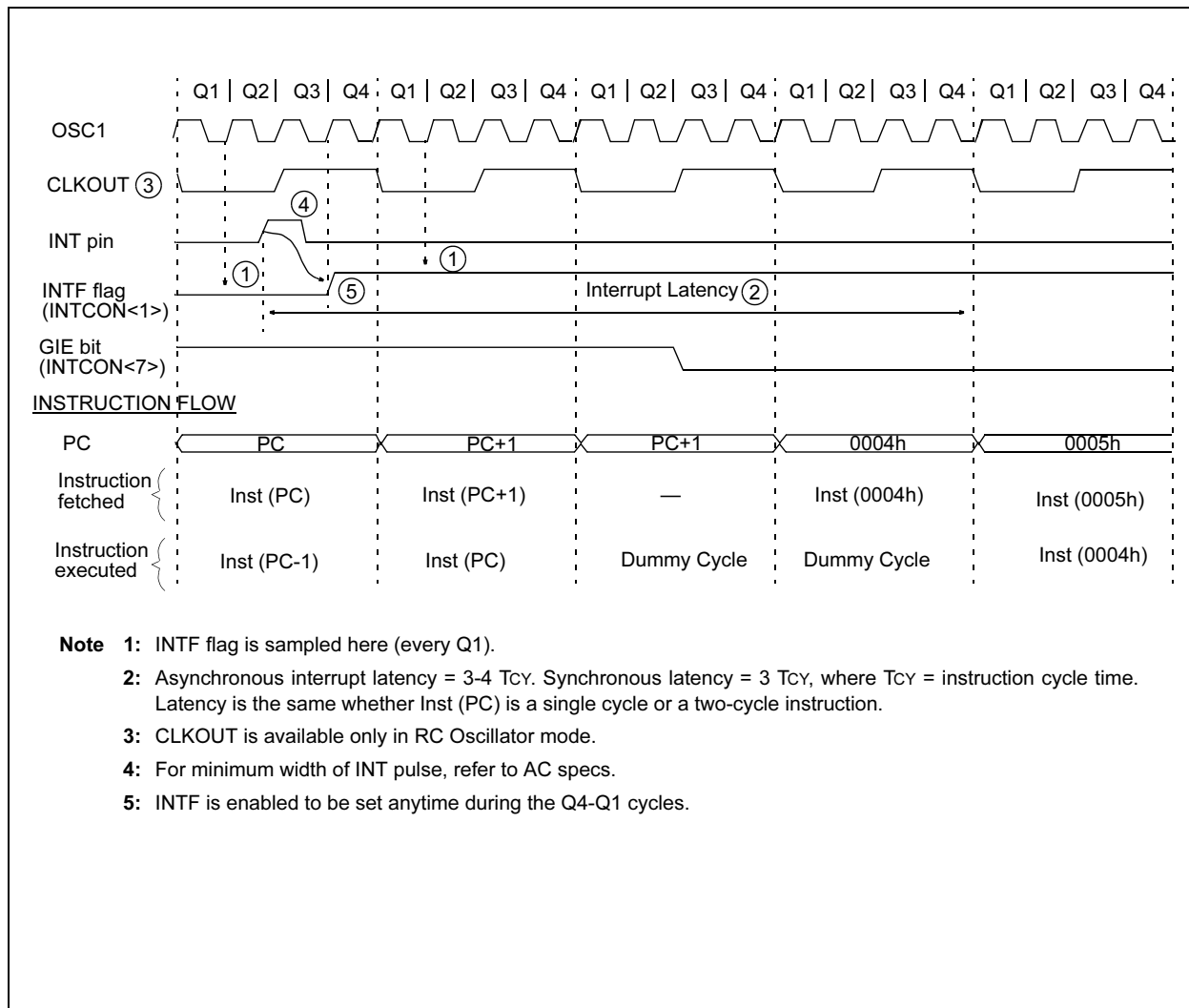
An input change on PORTB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB (Section 5.2).

**Note:** If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set.

## 9.5.4 COMPARATOR INTERRUPT

See Section 7.6 for complete description of comparator interrupts.

**FIGURE 9-16: INT PIN INTERRUPT TIMING**



## 10.1 Instruction Descriptions

ADDLW		Add Literal and W							
Syntax:	[ <i>label</i> ] ADDLW    k								
Operands:	$0 \leq k \leq 255$								
Operation:	$(W) + k \rightarrow (W)$								
Status Affected:	C, DC, Z								
Encoding:	<table border="1"><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>					11	111x	kkkk	kkkk
11	111x	kkkk	kkkk						
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ADDLW    0x15								
	Before Instruction								
	W        =    0x10								
	After Instruction								
	W        =    0x25								

ADDWF		Add W and f							
Syntax:	[ <i>label</i> ] ADDWF    f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	$(W) + (f) \rightarrow (dest)$								
Status Affected:	C, DC, Z								
Encoding:	<table border="1"><tr><td>00</td><td>0111</td><td>dfff</td><td>ffff</td></tr></table>					00	0111	dfff	ffff
00	0111	dfff	ffff						
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example	ADDWF    FSR,    0								
	Before Instruction								
	W    =    0x17								
	FSR =    0xC2								
	After Instruction								
	W    =    0xD9								
	FSR =    0xC2								

ANDLW		AND Literal with W							
Syntax:	[ <i>label</i> ] ANDLW    k								
Operands:	$0 \leq k \leq 255$								
Operation:	$(W) .\text{AND}. (k) \rightarrow (W)$								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>					11	1001	kkkk	kkkk
11	1001	kkkk	kkkk						
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ANDLW    0x5F								
	Before Instruction								
	W        =    0xA3								
	After Instruction								
	W        =    0x03								

ANDWF		AND W with f							
Syntax:	[ <i>label</i> ] ANDWF    f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	(W) .AND. (f) $\rightarrow$ (dest)								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>00</td><td>0101</td><td>dfff</td><td>ffff</td></tr></table>					00	0101	dfff	ffff
00	0101	dfff	ffff						
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example	ANDWF    FSR,    1								
Before Instruction									
W    =    0x17									
FSR =    0xC2									
After Instruction									
W    =    0x17									
FSR =    0x02									

## RLF Rotate Left f through Carry

**Syntax:** [ *label* ] RLF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

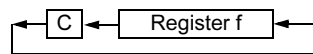
**Operation:** See description below

**Status Affected:** C

**Encoding:**

00	1101	dfff	ffff
----	------	------	------

**Description:** The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.



**Words:** 1

**Cycles:** 1

**Example** RLF REG1,0

**Before Instruction**

REG1 = 1110 0110  
 C = 0

**After Instruction**

REG1 = 1110 0110  
 W = 1100 1100  
 C = 1

## RRF Rotate Right f through Carry

**Syntax:** [ *label* ] RRF f,d

**Operands:**  $0 \leq f \leq 127$   
 $d \in [0,1]$

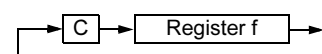
**Operation:** See description below

**Status Affected:** C

**Encoding:**

00	1100	dfff	ffff
----	------	------	------

**Description:** The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



**Words:** 1

**Cycles:** 1

**Example** RRF REG1,0

**Before Instruction**

REG1 = 1110 0110  
 C = 0

**After Instruction**

REG1 = 1110 0110  
 W = 0111 0011  
 C = 0

## SLEEP

**Syntax:** [ *label* ] SLEEP ]

**Operands:** None

**Operation:** 00h → WDT,  
 0 → WDT prescaler,  
 1 →  $\overline{TO}$ ,  
 0 → PD

**Status Affected:**  $\overline{TO}$ , PD

**Encoding:**

00	0000	0110	0011
----	------	------	------

**Description:** The power-down STATUS bit, PD is cleared. Time-out STATUS bit,  $\overline{TO}$  is set. Watch-dog Timer and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See Section 9.8 for more details.

**Words:** 1

**Cycles:** 1

**Example:** SLEEP

## 11.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
  - MPLAB dsPIC30 Software Simulator
- Emulators
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  - PICDEM MSC
  - microID®
  - CAN
  - PowerSmart®
  - Analog

## 11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files (assembly or C)
  - absolute listing file (mixed assembly and C)
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

## 11.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 12.0 ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings †

Ambient Temperature under bias .....	-40° to +125°C
Storage Temperature .....	-65° to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$ ) .....	-0.6V to VDD +0.6V
Voltage on VDD with respect to VSS .....	0 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS ( <b>Note 2</b> ) .....	0 to +14V
Voltage on RA4 with respect to VSS .....	8.5V
Total power Dissipation ( <b>Note 1</b> ) .....	1.0W
Maximum Current out of VSS pin .....	300 mA
Maximum Current into VDD pin .....	250 mA
Input Clamp Current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > VDD) .....	±20 mA
Output Clamp Current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > VDD) .....	±20 mA
Maximum Output Current sunk by any I/O pin .....	25 mA
Maximum Output Current sourced by any I/O pin .....	25 mA
Maximum Current sunk by PORTA and PORTB .....	200 mA
Maximum Current sourced by PORTA and PORTB .....	200 mA

**Note 1:** Power dissipation is calculated as follows:  $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$ .

**2:** Voltage spikes below VSS at the  $\overline{\text{MCLR}}$  pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the  $\overline{\text{MCLR}}$  pin rather than pulling this pin directly to VSS.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



# PIC16C62X

<b>PIC16CR62XA-04</b> <b>PIC16CR62XA-20</b>			<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
<b>PIC16LCR62XA-04</b>			<b>Standard Operating Conditions (unless otherwise stated)</b> Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula:  $I_r = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.

**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**6:** Commercial temperature range only.

## 12.6 DC Characteristics: PIC16C620A/C621A/C622A-40<sup>(3)</sup> (Commercial) PIC16CR620A-40<sup>(3)</sup> (Commercial)

DC CHARACTERISTICS Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial			
Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
Supply Voltage	VDD	4.5	—	5.5	V	HS Option from 20 - 40 MHz
Supply Current <sup>(2)</sup>	IDD	—	5.5	11.5	mA	FOSC = 40 MHz, VDD = 4.5V, HS mode
		—	7.7	16	mA	FOSC = 40 MHz, VDD = 5.5V, HS mode
HS Oscillator Operating Frequency	FOSC	20	—	40	MHz	OSC1 pin is externally driven, OSC2 pin not connected
Input Low Voltage OSC1	VIL	VSS	—	0.2VDD	V	HS mode, OSC1 externally driven
Input High Voltage OSC1	VIH	0.8VDD	—	VDD	V	HS mode, OSC1 externally driven

\* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS,  
T0CKI = VDD, MCLR = VDD; WDT disabled, HS mode with OSC2 not connected.

**3:** For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

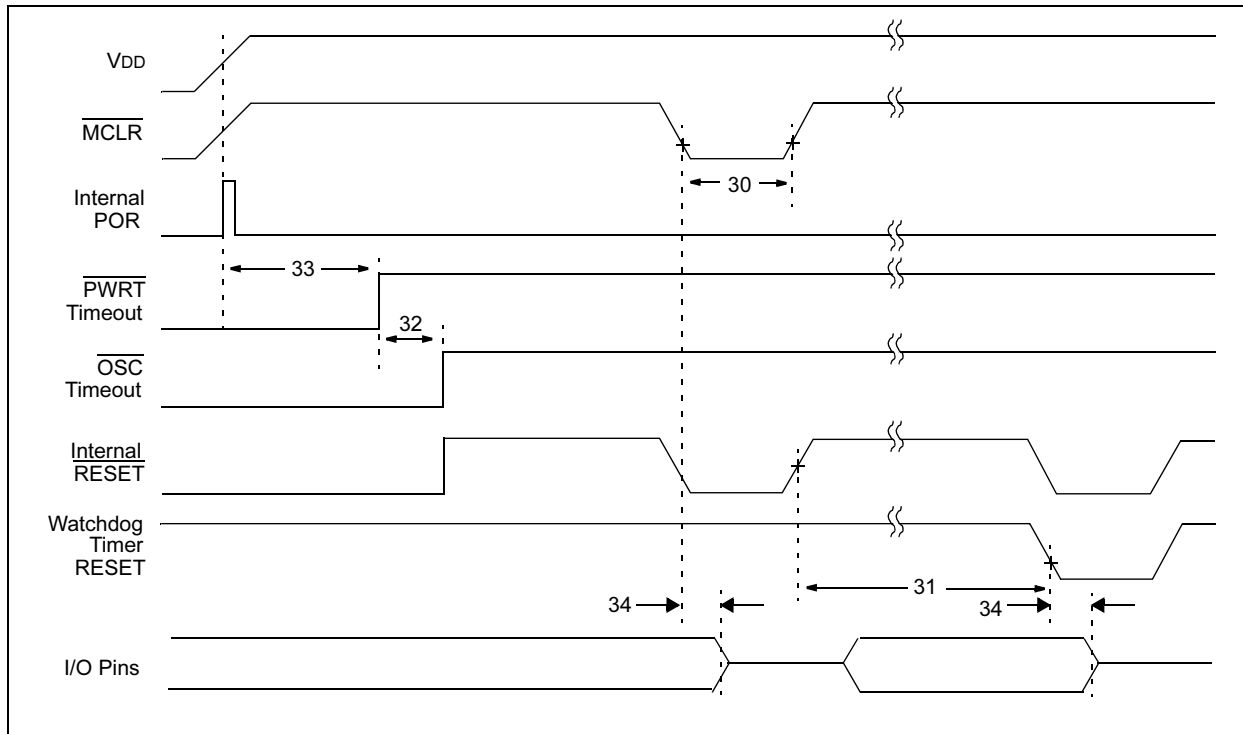
## 12.7 AC Characteristics: PIC16C620A/C621A/C622A-40<sup>(2)</sup> (Commercial) PIC16CR620A-40<sup>(2)</sup> (Commercial)

AC CHARACTERISTICS All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial			
Characteristic	Sym	Min	Typ <sup>(1)</sup>	Max	Units	Conditions
External CLKIN Frequency	FOSC	20	—	40	MHz	HS mode, OSC1 externally driven
External CLKIN Period	Tosc	25	—	50	ns	HS mode (40), OSC1 externally driven
Clock in (OSC1) Low or High Time	TosL, TosH	6	—	—	ns	HS mode, OSC1 externally driven
Clock in (OSC1) Rise or Fall Time	TosR, TosF	—	—	6.5	ns	HS mode, OSC1 externally driven
OSC1↑ (Q1 cycle) to Port out valid	TosH2ioV	—	—	100	ns	—
OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TosH2ioI	50	—	—	ns	—

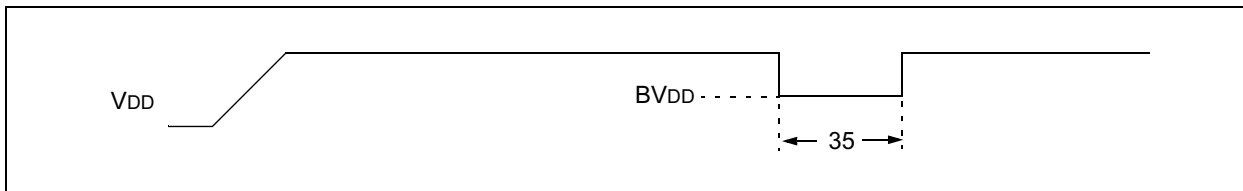
**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

**FIGURE 12-14: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**



**FIGURE 12-15: BROWN-OUT RESET TIMING**



**TABLE 12-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2000	—	—	ns	-40° to +85°C
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7*	18	33*	ms	VDD = 5.0V, -40° to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28*	72	132*	ms	VDD = 5.0V, -40° to +85°C
34	TIOZ	I/O hi-impedance from MCLR low	—	—	2.0	μs	
35	TBOR	Brown-out Reset Pulse Width	100*	—	—	μs	3.7V ≤ VDD ≤ 4.3V

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

# PIC16C62X

FIGURE 12-16: TIMER0 CLOCK TIMING

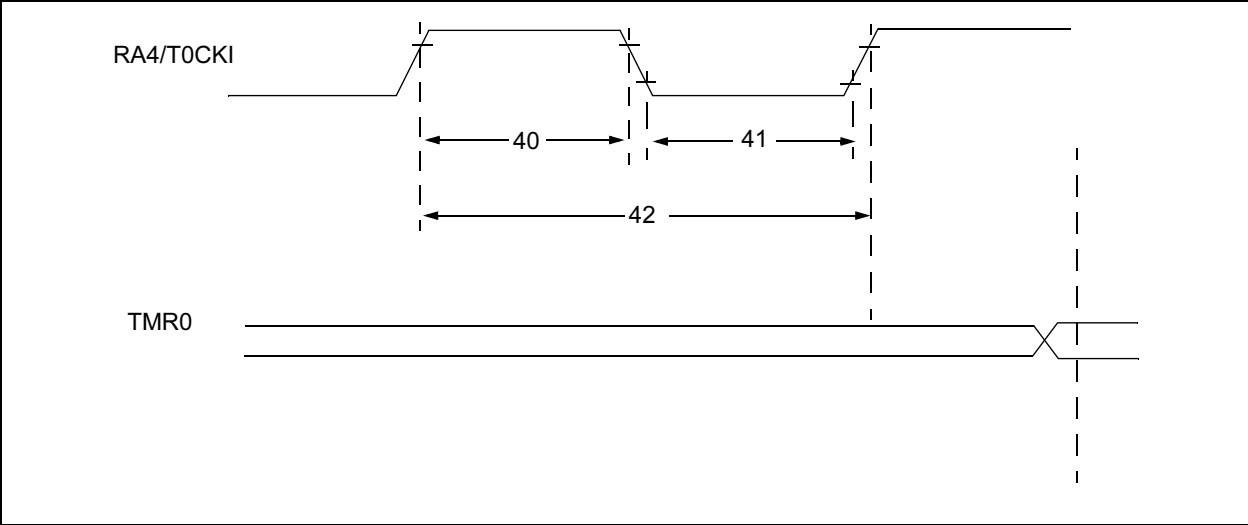


TABLE 12-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
			With Prescaler	$10^*$	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
			With Prescaler	$10^*$	—	—	ns	
42	Tt0P	T0CKI Period		$\frac{T_{CY} + 40^*}{N}$	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.



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