# E·XFL



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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c620at-04i-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 2.0 PIC16C62X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC16C62X Product Identification System section at the end of this data sheet. When placing orders, please use this page of the data sheet to specify the correct part number.

#### 2.1 UV Erasable Devices

The UV erasable version, offered in CERDIP package, is optimal for prototype development and pilot programs. This version can be erased and reprogrammed to any of the Oscillator modes.

Microchip's PICSTART<sup>®</sup> and PRO MATE<sup>®</sup> programmers both support programming of the PIC16C62X.

Note: Microchip does not recommend code protecting windowed devices.

#### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications. In addition to the program memory, the configuration bits must also be programmed.

#### 2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who chose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices, but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

#### 2.4 Serialized Quick-Turnaround-Production<sup>sm</sup> (SQTP<sup>sm</sup>) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry-code, password or ID number.

#### FIGURE 3-1: BLOCK DIAGRAM



## FIGURE 4-6: DATA MEMORY MAP FOR THE PIC16C620A/CR620A/621A

File Address	5		File Address				
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h				
01h	TMR0	OPTION	81h				
02h	PCL	PCL	82h				
03h	STATUS	STATUS	83h				
04h	FSR	FSR	84h				
05h	PORTA	TRISA	85h				
06h	PORTB	TRISB	86h				
07h			87h				
08h			88h				
09h			89h				
0Ah	PCLATH	PCLATH	8Ah				
0Bh	INTCON	INTCON	8Bh				
0Ch	PIR1	PIE1	8Ch				
0Dh			8Dh				
0Eh		PCON	8Eh				
0Fh			8Fh				
10h			90h				
11h			91h				
12h			92h				
13h			93h				
14h			94h				
15h			95h				
16h			96h				
17h			97h				
18h			98h				
19h			99h				
1Ah			9Ah				
1Bh			9Bh				
1Ch			9Ch				
1Dh			9Dh				
1Eh			9Eh				
1Fh	CMCON	VRCON	9Fh				
20h	General Purpose Register		A0h				
6Fh							
70h	General		F0h				
7011	Purpose	Accesses					
7Fh	Register	1011-1711	FFh				
	Bank 0	Bank 1					
Unimplemented data memory locations, read as '0'.							
Note 1:	Not a physical re	gister.					

#### FIGURE 4-7: DATA MEMORY MAP FOR THE PIC16C622A

File Address	;		File Address				
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h				
01h	TMR0	OPTION	81h				
02h	PCL	PCL	82h				
03h	STATUS	STATUS	83h				
04h	FSR	FSR	84h				
05h	PORTA	TRISA	85h				
06h	PORTB	TRISB	86h				
07h			87h				
08h			88h				
09h			89h				
0Ah	PCLATH	PCLATH	8Ah				
0Bh	INTCON	INTCON	8Bh				
0Ch	PIR1	PIE1	8Ch				
0Dh			8Dh				
0Eh		PCON	8Eh				
0Fh			8Fh				
10h			90h				
11h			91h				
12h			92h				
13h			93h				
14h			94h				
15h			95h				
16h			96h				
17h			97h				
18h			98h				
19h			99h				
1Ah			9Ah				
1Bh			9Bh				
1Ch			9Ch				
1Dn							
1En	014001		9En				
1Fn	CMCON	VRCON	9Fn				
20h	General	General	A0h				
	Purpose	Purpose					
	Register	Register	BFh				
			C0h				
			0011				
6Fh			– F0h				
70h	General	Accesses					
	Register	70h-7Fh	EEh				
/Fhl	Bank 0	Bank 1					
Unimp	elemented data me	mory locations, re	ead as '0'.				
Note 1: Not a physical register.							









#### EXAMPLE 8-1: VOLTAGE REFERENCE CONFIGURATION

MOVLW	0x02	; 4 Inputs Muxed
MOVWF	CMCON	; to 2 comps.
BSF	STATUS, RPO	; go to Bank 1
MOVLW	0x0F	; RA3-RA0 are
MOVWF	TRISA	; inputs
MOVLW	0xA6	; enable VREF
MOVWF	VRCON	; low range
		; set VR<3:0>=6
BCF	STATUS, RPO	; go to Bank O
CALL	DELAY10	; 10µs delay

#### 8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-1) keep VREF from approaching VSS or VDD. The voltage reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The tested absolute accuracy of the voltage reference can be found in Table 12-2.

#### 8.3 Operation During SLEEP

When the device wakes up from SLEEP through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the voltage reference should be disabled.

#### 8.4 Effects of a RESET

A device RESET disables the voltage reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

#### 8.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the voltage reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the voltage reference output for external connections to VREF. Figure 8-2 shows an example buffering technique.

# FIGURE 8-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE

#### TABLE 8-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR	Value On All Other RESETS
9Fh	VRCON	VREN	VROE	VRR		VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C10UT	_	-	CIS	CM2	CM1	CM0	00 0000	00 0000
85h	TRISA	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

**Note:** - = Unimplemented, read as "0"

#### 9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

#### REGISTER 9-1: CONFIGURATION WORD (ADDRESS 2007h)

CP1	CP0 (2)	CP1	CP0 (2)	CP1	CP0 (2)		BODEN	CP1	CP0 <sup>(2)</sup>	PWRTE	WDTE	F0SC1	F0SC0
bit 13							Į		ļ		<u> </u>	ļ	bit 0
bit 13-8 5-4:	<ul> <li>Code protection bit pairs <sup>(2)</sup></li> <li>Code protection for 2K program memory</li> <li>Program memory code protection off</li> <li>0 = 0400h-07FFh code protected</li> <li>0 = 0200h-07FFh code protected</li> <li>0 = 0000h-07FFh code protected</li> <li>Code protection for 1K program memory</li> <li>Program memory code protection off</li> <li>Program memory code protection off</li> <li>Program memory code protection off</li> <li>0 = Program memory code protection off</li> <li>0 = 0200h-03FFh code protected</li> <li>0 = 0000h-03FFh code protected</li> </ul>												
	Code protection for 0.5K program memory 11 = Program memory code protection off 10 = Program memory code protection off 01 = Program memory code protection off 00 = 0000h-01FFh code protected												
bit 7	Uniı	npleme	e <b>nted</b> : Re	ead as 'C	)'								
bit 6	BOI	DEN: Br	own-out	Reset E	nable bit	(1)							
	1 = 0 =	1 = BOR enabled 0 = BOR disabled											
bit 3	<b>PWI</b> 1 = 0 =	<b>PWRTE</b> : Power-up Timer Enable bit <sup>(1, 3)</sup> 1 = PWRT disabled 0 = PWRT enabled											
bit 2	<b>WD</b> 1 = ' 0 = '	WDTE: Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled											
bit 1-0	FOS	C1:FO	SCO: Oso	cillator S	election	bits							
	11 - 10 = 01 = 00 =	11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator											
	<ul> <li>Note 1: Enabling Brown-out Reset automatically enables Power-up Timer (PWRT) regardless of the value of bit PWRTE. Ensure the Power-up Timer is enabled anytime Brown-out Detect Reset is enabled.</li> <li>All of the OD states pairs have to be size at the size at the</li></ul>						the eset is						
	<ol> <li>All of the CP&lt;1:0&gt; pairs have to be given the same value to enable the code protection scheme listed.</li> <li>Unprogrammed parts default the Power-up Timer disabled.</li> </ol>												
Logond	1.												
R = Re	ı. adable b	it		W = 1	Writable	bit	U =	Unimple	emented	bit, read a	s '0'		

#### 9.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

#### 9.4.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level for proper operation. To take advantage of the POR, just tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce an internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting".

#### 9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, PWRTE can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

The Power-up Time delay will vary from chip-to-chip and due to VDD, temperature and process variation. See DC parameters for details.

#### 9.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

#### 9.4.4 BROWN-OUT RESET (BOR)

The PIC16C62X members have on-chip Brown-out Reset circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V refer to VBOR parameter D005 (VBOR) for greater than parameter (TBOR) in Table 12-5. The brown-out situation will RESET the chip. A RESET won't occur if VDD falls below 4.0V for less than parameter (TBOR).

On any RESET (Power-on, Brown-out, Watchdog, etc.) the chip will remain in RESET until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms.

If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-Up Timer will execute a 72 ms RESET. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 9-7 shows typical Brown-out situations.



#### FIGURE 9-7: BROWN-OUT SITUATIONS

#### 9.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit in the STATUS register is cleared, the TO bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSs with no external circuitry drawing current from the I/O pin and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSs for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

Note:	It should be noted that a RESET generated
	by a WDT time-out does not drive MCLR
	pin low.

#### 9.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- 1. External RESET input on MCLR pin
- 2. Watchdog Timer Wake-up (if WDT was enabled)
- 3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. PD bit, which is set on power-up, is cleared when SLEEP is invoked. TO bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction after the SLEEP instruction after the instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4	4 Q1	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
CLKOUT(4)	Tost(2	)/	\/	\/'\	'
INT pin		1	ı ı ı ı	1	I
INTE flag	\		I I		
(INTCON<1>)	·····/	Interrupt Latend	şy		
	<u>i</u>	(Note 2)	i		
(INTCON<7>)	Processor in	1		<u> </u>	<u> </u>
	SLEEP	1	I I	i	i i
INSTRUCTION FLOW		1	і і і і	1	1
PC X PC+1	X PC+2	X PC+2	X PC + 2	<u>x 0004h x</u>	0005h
$\begin{array}{c} \mbox{Instruction} \\ \mbox{fetched} \end{array} \Big\{ \begin{array}{c} \mbox{Inst}(\mbox{PC}) = \mbox{SLEEP} & \mbox{Inst}(\mbox{PC} + 1) \end{array} \right.$		Inst(PC + 2)	       	Inst(0004h)	Inst(0005h)
Instruction { Inst(PC - 1) SLEEP	1 1 1	Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)
Note 1: XT, HS or LP Oscillator mode 2: Tos⊤ = 1024Tosc (drawing n	e assumed. ot to scale) This	delay will not be	e there for RC	Osc mode.	

#### FIGURE 9-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT

**3:** GIE = '1' assumed. In this case, after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these Osc modes, but shown here for timing reference.

TABLE 10-2: PIC16C62X INSTRUCTION S
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Mnemonic,		Description	Cycles		14-Bit	Opcode	9	Status	Notes	
Operands				MSb			LSb	Affected		
BYTE-ORIENTED FILE REGISTER OPERATIONS										
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2	
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2	
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2	
CLRW	-	Clear W	1	00	0001	0000	0011	Z		
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2	
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2	
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3	
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2	
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3	
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2	
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2	
MOVWF	f	Move W to f	1	00	0000	lfff	ffff			
NOP	-	No Operation	1	00	0000	0xx0	0000			
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2	
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2	
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2	
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2	
XORWF	f, d Exclusive OR W with f		1	00	0110	dfff	ffff	Z	1,2	
BIT-ORIENT	ED FIL	E REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2	
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2	
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3	
LITERAL A	ND COI	NTROL OPERATIONS	-					-		
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z		
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z		
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk			
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD		
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk			
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z		
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk			
RETFIE	-	Return from interrupt	2	00	0000	0000	1001			
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk			
RETURN	-	Return from Subroutine	2	00	0000	0000	1000			
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD		
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z		
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z		

**Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

**3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

DECFSZ	Decrement f, Skip if 0
Syntax:	[label] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 $\rightarrow$ (dest); skip if result = 0
Status Affected:	None
Encoding:	00 1011 dfff ffff
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 0, the next instruc- tion, which is already fetched, is discarded. A NOP is executed instead making it a two-cycle instruction.
Words:	1
Cycles:	1(2)
Example	HERE DECFSZ CNT, 1 GOTO LOOP CONTINUE • • •
	After Instruction CNT = CNT - 1 if CNT = 0, PC = address CONTINUE if CNT ≠ 0, PC = address HERE+1
GOTO	Unconditional Branch
Syntax:	[ <i>label</i> ] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	k → PC<10:0> PCLATH<4:3> → PC<12:11>
Status Affected:	None
Encoding:	10 1kkk kkkk kkkk
Description:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two- cycle instruction.
Words:	1
Cycles:	2
Example	GOTO THERE
	After Instruction PC = Address THERE

INCF	Increment f						
Syntax:	[ <i>label</i> ] INCF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$						
Operation:	(f) + 1 $\rightarrow$ (dest)						
Status Affected:	Z						
Encoding:	00 1010 dfff ffff						
Description:	incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.						
Words:	1						
Cycles:	1						
Example	INCF CNT, 1						
	Before Instruction CNT = 0xFF Z = 0 After Instruction CNT = 0x00 Z = 1						

#### 11.14 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer, or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include analog input, push button switches and eight LEDs.

#### 11.15 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/ Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface, and a 16 x 2 LCD display. Also included is the book and CD-ROM *"TCP/IP Lean, Web Servers for Embedded Systems,"* by Jeremy Bentham

#### 11.16 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18-, 28-, and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs, and sample PIC18F452 and PIC16F877 FLASH microcontrollers.

#### 11.17 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

#### 11.18 PICDEM 4 8/14/18-Pin Demonstration Board

The PICDEM 4 can be used to demonstrate the capabilities of the 8-, 14-, and 18-pin PIC16XXXX and PIC18XXXX MCUs, including the PIC16F818/819, PIC16F87/88, PIC16F62XA and the PIC18F1320 family of microcontrollers. PICDEM 4 is intended to showcase the many features of these low pin count parts, including LIN and Motor Control using ECCP. Special provisions are made for low power operation with the supercapacitor circuit, and jumpers allow onboard hardware to be disabled to eliminate current draw in this mode. Included on the demo board are provisions for Crystal, RC or Canned Oscillator modes, a five volt regulator for use with a nine volt wall adapter or battery, DB-9 RS-232 interface, ICD connector for programming via ICSP and development with MPLAB ICD 2, 2x16 liquid crystal display, PCB footprints for H-Bridge motor driver, LIN transceiver and EEPROM. Also included are: header for expansion, eight LEDs, four potentiometers, three push buttons and a prototyping area. Included with the kit is a PIC16F627A and a PIC18F1320. Tutorial firmware is included along with the User's Guide.

#### 11.19 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board FLASH memory. A generous prototype area is available for user hardware expansion. NOTES:

#### 12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended)

PIC16C	62XA		Stan Oper	dard O ating te	perati empera	ng Con ature -4 -4	ditions (unless otherwise stated) $40^{\circ}C \leq TA \leq +85^{\circ}C$ for industrial and $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial and $40^{\circ}C \leq TA \leq +125^{\circ}C$ for extended		
PIC16LC62XA				tandard Operating Conditions (unless otherwise stated) operating temperature $-40^{\circ}$ C $\leq TA \leq +85^{\circ}$ C for industrial and $0^{\circ}$ C $\leq TA \leq +70^{\circ}$ C for commercial a $-40^{\circ}$ C $\leq TA \leq +125^{\circ}$ C for extended					
Param. No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions		
D001	Vdd	Supply Voltage	3.0	-	5.5	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5		
D001	Vdd	Supply Voltage	2.5	_	5.5	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	-	1.5*	_	V	Device in SLEEP mode		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	—	1.5*	—	V	Device in SLEEP mode		
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss	_	V	See section on Power-on Reset for details		
D003	VPOR	VDD start voltage to ensure Power-on Reset	-	Vss	_	V	See section on Power-on Reset for details		
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	_	-	V/ms	See section on Power-on Reset for details		
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	_	V/ms	See section on Power-on Reset for details		
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared		
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**6:** Commercial temperature range only.

## PIC16C62X

#### 12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended (CONT.)

PIC16C62XA				$\begin{tabular}{ c c c c c } \hline Standard Operating Conditions (unless otherwise stated) \\ Operating temperature & -40^\circ C & \leq TA \leq +85^\circ C \mbox{ for industrial and} \\ & 0^\circ C & \leq TA \leq +70^\circ C \mbox{ for commercial and} \\ & -40^\circ C & \leq TA \leq +125^\circ C \mbox{ for extended} \end{tabular}$					
PIC16LC62XA				$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions		
D022	ΔİWDT	WDT Current <sup>(5)</sup>	—	6.0	10 12	μA μA	VDD = 4.0V (125°C)		
D022A	$\Delta$ IBOR	Brown-out Reset Current <sup>(5)</sup>	—	75	125	μA	BOD enabled, VDD = 5.0V		
D023		Comparator Current for each Comparator <sup>(5)</sup>	_	30	60	μA	VDD = 4.0V		
D023A	ΔIVREF	VREF Current <sup>(3)</sup>	_	80	135	μA	VDD = 4.0V		
D022	$\Delta I$ WDT	WDT Current <sup>(5)</sup>	—	6.0	10	μΑ	VDD=4.0V		
DOODA	41	Descent Descet Operation (5)		75	12	μA	$\frac{(125^{\circ}C)}{200} = 5.0$		
D022A		Brown-out Reset Current <sup>(e)</sup>		75	125	μΑ	BOD enabled, $VDD = 5.0V$		
D023	AICOMP	Comparator Current for each		30	60	μΑ	VDD - 4.0V		
D023A	$\Delta$ IVREF	VREF Current <sup>(5)</sup>	_	80	135	μA	VDD = 4.0V		
1A	Fosc	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures		
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures		
		XT Oscillator Operating Frequency	0		4	MHz	All temperatures		
		HS Oscillator Operating Frequency	0	—	20	MHZ	All temperatures		
1A	Fosc	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures		
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures		
		HS Oscillator Operating Frequency	0	_	4 20	MHZ MHZ	All temperatures All temperatures		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

 $\overline{\text{MCLR}}$  = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

## PIC16C62X

#### 12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended)

PIC16C62X/C62XA/CR62XA				$\begin{tabular}{ c c c c c } \hline Standard Operating Conditions (unless otherwise stated) \\ Operating temperature & -40°C & \leq TA \leq +85°C \mbox{ for industrial and} \\ & 0°C & \leq TA \leq +70°C \mbox{ for commercial and} \\ & -40°C & \leq TA \leq +125°C \mbox{ for extended} \\ \hline \end{tabular}$					
PIC16LC62X/LC62XA/LCR62XA			<b>Standa</b> Operatir	Standard Operating Conditions (unless otherwise states)Operating temperature $-40^{\circ}$ C $\leq$ TA $\leq$ +85°C for industr $0^{\circ}$ C $\leq$ TA $\leq$ +70°C for commercian $-40^{\circ}$ C $\leq$ TA $\leq$ +125°C for exter					
Param. No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions		
	VIL	Input Low Voltage							
		I/O ports							
D030		with TTL buffer	Vss	—	0.8V 0.15 VDD	V	VDD = 4.5V to 5.5V otherwise		
D031		with Schmitt Trigger input	Vss		0.2 VDD	V			
D032		MCLR, RA4/T0CKI,OSC1 (in RC mode)	Vss	—	0.2 VDD	V	(Note 1)		
D033		OSC1 (in XT and HS)	Vss	—	0.3 VDD	V			
		OSC1 (in LP)	Vss	—	0.6 Vdd- 1.0	V			
	VIL	Input Low Voltage							
		I/O ports							
D030		with TTL buffer	Vss	-	0.8V 0.15 VDD	V	VDD = 4.5V to 5.5V otherwise		
D031		with Schmitt Trigger input	Vss	—	0.2 VDD	V			
D032		MCLR, RA4/T0CKI,OSC1 (in RC mode)	Vss	—	0.2 VDD	V	(Note 1)		
D033		OSC1 (in XT and HS)	Vss	—	0.3 VDD	V			
		OSC1 (in LP)	Vss	—	0.6 Vdd- 1.0	V			
	VIH	Input High Voltage							
		I/O ports							
D040		with TTL buffer	2.0V 0.25 VDD + 0.8V	_	Vdd Vdd	V	VDD = 4.5V to 5.5V otherwise		
D041		with Schmitt Trigger input	0.8 Vdd	_	VDD				
D042		MCLR RA4/T0CKI	0.8 Vdd	_	Vdd	V			
D043 D043A		OSC1 (XT, HS and LP) OSC1 (in RC mode)	0.7 Vdd 0.9 Vdd	—	Vdd	V	(Note 1)		

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

## 12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40<sup>(7)</sup> (Commercial) PIC16CR620A-40<sup>(7)</sup> (Commercial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial						
Param No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions		
D001	Vdd	Supply Voltage	3.0		5.5	V	Fosc = DC to 20 MHz		
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>		1.5*	_	V	Device in SLEEP mode		
D003	VPOR	VDD start voltage to ensure Power-on Reset	_	Vss		V	See section on Power-on Reset for details		
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05 *			V/ms	See section on Power-on Reset for details		
D005	VBOR	Brown-out Detect Voltage	3.65	4.0	4.35	V	BOREN configuration bit is cleared		
D010	IDD	Supply Current <sup>(2,4)</sup>	—	1.2	2.0	mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled, XT Osc mode, (Note 4)*		
			—	0.4	1.2	mA	Fosc = 4 MHz, VDD = 3.0V, WDT disabled, XT Osc mode. (Note 4)		
			—	1.0	2.0	mA	Fosc = 10 MHz, VDD = 3.0V, WDT disabled, HS Osc mode. (Note 6)		
			—	4.0	6.0	mA	Fosc = 20 MHz, VDD = 4.5V, WDT disabled,		
			—	4.0	7.0	mA	Fosc = 20 MHz, VDD = 5.5V, WDT disabled*,		
			—	35	70	μA	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP Osc mode		
D020	IPD	Power Down Current <sup>(3)</sup>		_	2.2	μA	VDD = 3.0V		
			—	—	5.0	μA	VDD = 4.5V*		
			—	—	9.0	μA	$V_{DD} = 5.5V$		
<b>D</b> 000			_	_	15	μΑ			
D022	AIWDI	WD1 Current <sup>(*)</sup>		6.0	10	μΑ	VDD = 4.0V (125°C)		
D022A	AIBOR	Brown-out Reset Current <sup>(5)</sup>	_	75	125	μΑ	$\frac{(123)}{123}$ Of BOD enabled, VDD = 5.0V		
D023		Comparator Current for each Comparator <sup>(5)</sup>	—	30	60	μA	VDD = 4.0V		
D023A	$\Delta$ IVREF	VREF Current <sup>(5)</sup>	_	80	135	μA	VDD = 4.0V		
	$\Delta$ IEE Write	Operating Current	_		3	mA	Vcc = 5.5V, SCL = 400 kHz		
	$\Delta \text{IEE} \ \text{Read}$	Operating Current	—		1	mA			
	$\Delta IEE$	Standby Current	—		30	μA	Vcc = 3.0V, EE VDD = Vcc		
	$\Delta IEE$	Standby Current	—		100	μA	VCC = 3.0V, EE VDD = VCC		
1A	Fosc	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures		
		XC Oscillator Operating Frequency	0	—	4	IVIHZ M⊔⊸			
		HS Oscillator Operating Frequency	0		- <del>-</del> 20	MHz	All temperatures		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption. The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD; WDT enabled/disabled as specified.
3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP

mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.
For RC OSC configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/ 2REXT (mA) with REXT in kΩ.

5: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

7: See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

#### TABLE 12-1: COMPARATOR SPECIFICATIONS

Operating Conditions: VDD range as described in Table 12-1, -40°C<TA<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Тур	Мах	Units	Comments
Input offset voltage			± 5.0	± 10	mV	
Input common mode voltage		0		Vdd - 1.5	V	
CMRR		+55*			δβ	
Response Time <sup>(1)</sup>			150*	400* 600*	ns ns	PIC16C62X(A) PIC16LC62X
Comparator mode change to output valid				10*	μS	

\* These parameters are characterized but not tested.

**Note 1:** Response time measured with one comparator input at (VDD - 1.5)/2, while the other input transitions from Vss to VDD.

#### TABLE 12-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions:VDD range as described in Table 12-1, -40°C<TA<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Тур	Мах	Units	Comments	
Resolution			Vdd/24 Vdd/32		LSB LSB	Low Range (VRR=1) High Range (VRR=0)	
Absolute Accuracy				<u>+</u> 1/4 <u>+</u> 1/2	LSB LSB	Low Range (VRR=1) High Range (VRR=0)	
Unit Resistor Value (R)			2K*		Ω	Figure 8-1	
Settling Time <sup>(1)</sup>				10*	μs		
* These parameters are characterized but not tested. <b>Note 1:</b> Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.							

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Parameter No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓ <sup>(1)</sup>		75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
11*	TosH2ck H	OSC1↑ to CLKOUT↑ <sup>(1)</sup>		75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
12*	TckR	CLKOUT rise time <sup>(1)</sup>		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
13*	TckF	CLKOUT fall time <sup>(1)</sup>		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
14*	TckL2ioV	CLKOUT $\downarrow$ to Port out valid <sup>(1)</sup>		—	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑ <sup>(1)</sup>	Tosc +200 ns Tosc +400 ns	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
16*	TckH2iol	Port in hold after CLKOUT $\uparrow^{(1)}$	0	—		ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	_	50	150 300	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
19*	TioV2osH	Port input valid to OSC1 <sup>↑</sup> (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time		10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
21*	TioF	Port output fall time		10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
22*	Tinp	RB0/INT pin high or low time	25 40	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
23	Trbp	RB<7:4> change interrupt high or low time	Тсү	—	_	ns	

#### TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

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