



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                     |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                              |
| Core Processor             | PIC                                                                                                                                                                 |
| Core Size                  | 8-Bit                                                                                                                                                               |
| Speed                      | 4MHz                                                                                                                                                                |
| Connectivity               | -                                                                                                                                                                   |
| Peripherals                | Brown-out Detect/Reset, POR, WDT                                                                                                                                    |
| Number of I/O              | 13                                                                                                                                                                  |
| Program Memory Size        | 1.75KB (1K x 14)                                                                                                                                                    |
| Program Memory Type        | OTP                                                                                                                                                                 |
| EEPROM Size                | -                                                                                                                                                                   |
| RAM Size                   | 80 x 8                                                                                                                                                              |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 6V                                                                                                                                                             |
| Data Converters            | -                                                                                                                                                                   |
| Oscillator Type            | External                                                                                                                                                            |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                   |
| Mounting Type              | Surface Mount                                                                                                                                                       |
| Package / Case             | 18-SOIC (0.295", 7.50mm Width)                                                                                                                                      |
| Supplier Device Package    | 18-SOIC                                                                                                                                                             |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c621-04i-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16c621-04i-so</a> |

## Table of Contents

|                                                |                                           |     |
|------------------------------------------------|-------------------------------------------|-----|
| 1.0                                            | General Description .....                 | 5   |
| 2.0                                            | PIC16C62X Device Varieties .....          | 7   |
| 3.0                                            | Architectural Overview .....              | 9   |
| 4.0                                            | Memory Organization .....                 | 13  |
| 5.0                                            | I/O Ports .....                           | 25  |
| 6.0                                            | Timer0 Module .....                       | 31  |
| 7.0                                            | Comparator Module .....                   | 37  |
| 8.0                                            | Voltage Reference Module .....            | 43  |
| 9.0                                            | Special Features of the CPU .....         | 45  |
| 10.0                                           | Instruction Set Summary .....             | 61  |
| 11.0                                           | Development Support .....                 | 75  |
| 12.0                                           | Electrical Specifications .....           | 81  |
| 13.0                                           | Device Characterization Information ..... | 109 |
| 14.0                                           | Packaging Information .....               | 113 |
| Appendix A: Enhancements .....                 |                                           | 119 |
| Appendix B: Compatibility .....                |                                           | 119 |
| Index .....                                    |                                           | 121 |
| On-Line Support .....                          |                                           | 123 |
| Systems Information and Upgrade Hot Line ..... |                                           | 123 |
| Reader Response .....                          |                                           | 124 |
| Product Identification System .....            |                                           | 125 |

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at [docerrors@mail.microchip.com](mailto:docerrors@mail.microchip.com) or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)
- The Microchip Corporate Literature Center; U.S. FAX: (480) 792-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

### Customer Notification System

Register on our web site at [www.microchip.com/cn](http://www.microchip.com/cn) to receive the most current information on all of our products.

# PIC16C62X

### 3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

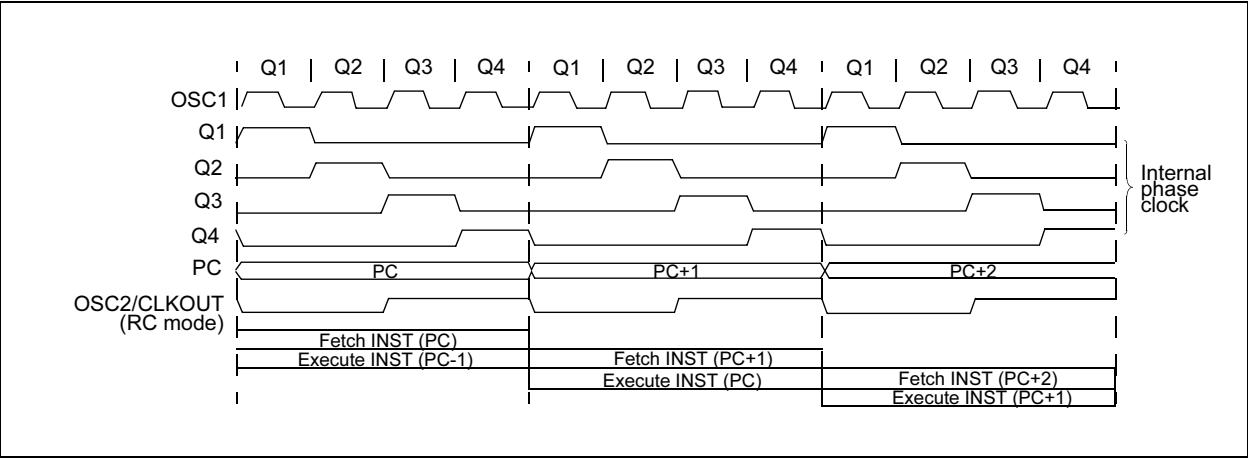
### 3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

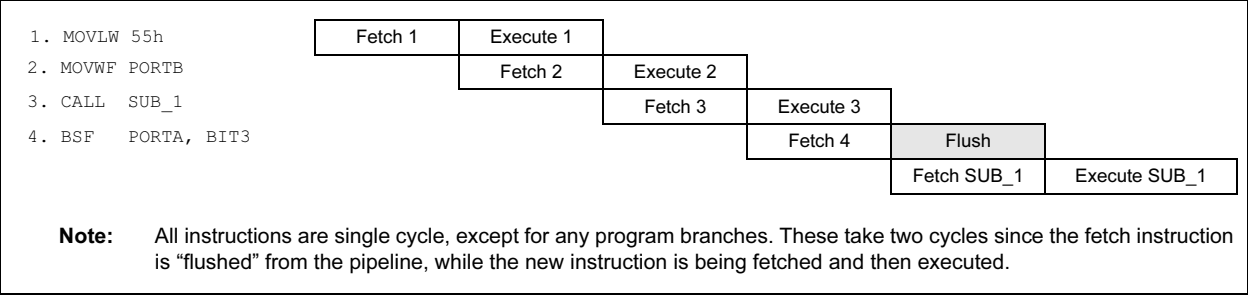
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register (IR)" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



## 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM.

The Special Function Registers can be classified into two sets (core and peripheral). The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

**TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C62X**

| Address       | Name          | Bit 7                                                                                          | Bit 6              | Bit 5  | Bit 4                                            | Bit 3            | Bit 2            | Bit 1            | Bit 0            | Value on POR Reset | Value on all other RESETS <sup>(1)</sup> |
|---------------|---------------|------------------------------------------------------------------------------------------------|--------------------|--------|--------------------------------------------------|------------------|------------------|------------------|------------------|--------------------|------------------------------------------|
| <b>Bank 0</b> |               |                                                                                                |                    |        |                                                  |                  |                  |                  |                  |                    |                                          |
| 00h           | INDF          | Addressing this location uses contents of FSR to address data memory (not a physical register) |                    |        |                                                  |                  |                  |                  |                  | xxxx xxxx          | xxxx xxxx                                |
| 01h           | TMR0          | Timer0 Module's Register                                                                       |                    |        |                                                  |                  |                  |                  |                  | xxxx xxxx          | uuuu uuuu                                |
| 02h           | PCL           | Program Counter's (PC) Least Significant Byte                                                  |                    |        |                                                  |                  |                  |                  |                  | 0000 0000          | 0000 0000                                |
| 03h           | STATUS        | IRP <sup>(2)</sup>                                                                             | RP1 <sup>(2)</sup> | RP0    | $\overline{TO}$                                  | $\overline{PD}$  | Z                | DC               | C                | 0001 1xxx          | 000q quuu                                |
| 04h           | FSR           | Indirect data memory address pointer                                                           |                    |        |                                                  |                  |                  |                  |                  | xxxx xxxx          | uuuu uuuu                                |
| 05h           | PORTA         | —                                                                                              | —                  | —      | $\overline{RA4}$                                 | $\overline{RA3}$ | $\overline{RA2}$ | $\overline{RA1}$ | RA0              | ---x 0000          | ---u 0000                                |
| 06h           | PORTB         | RB7                                                                                            | RB6                | RB5    | $\overline{RB4}$                                 | $\overline{RB3}$ | $\overline{RB2}$ | $\overline{RB1}$ | RB0              | xxxx xxxx          | uuuu uuuu                                |
| 07h-09h       | Unimplemented |                                                                                                |                    |        |                                                  |                  |                  |                  |                  | —                  | —                                        |
| 0Ah           | PCLATH        | —                                                                                              | —                  | —      | Write buffer for upper 5 bits of program counter |                  |                  |                  |                  | ---0 0000          | ---0 0000                                |
| 0Bh           | INTCON        | GIE                                                                                            | PEIE               | TOIE   | INTE                                             | RBIE             | TOIF             | INTF             | RBIF             | 0000 000x          | 0000 000u                                |
| 0Ch           | PIR1          | —                                                                                              | CMIF               | —      | —                                                | —                | —                | —                | —                | -0-- ----          | -0-- ----                                |
| 0Dh-1Eh       | Unimplemented |                                                                                                |                    |        |                                                  |                  |                  |                  |                  | —                  | —                                        |
| 1Fh           | CMCON         | C2OUT                                                                                          | C1OUT              | —      | —                                                | CIS              | CM2              | CM1              | CM0              | 00-- 0000          | 00-- 0000                                |
| <b>Bank 1</b> |               |                                                                                                |                    |        |                                                  |                  |                  |                  |                  |                    |                                          |
| 80h           | INDF          | Addressing this location uses contents of FSR to address data memory (not a physical register) |                    |        |                                                  |                  |                  |                  |                  | xxxx xxxx          | xxxx xxxx                                |
| 81h           | OPTION        | $\overline{RBPU}$                                                                              | INTEDG             | T0CS   | T0SE                                             | PSA              | PS2              | PS1              | PS0              | 1111 1111          | 1111 1111                                |
| 82h           | PCL           | Program Counter's (PC) Least Significant Byte                                                  |                    |        |                                                  |                  |                  |                  |                  | 0000 0000          | 0000 0000                                |
| 83h           | STATUS        | IRP <sup>(2)</sup>                                                                             | RP1 <sup>(2)</sup> | RP0    | $\overline{TO}$                                  | $\overline{PD}$  | Z                | DC               | C                | 0001 1xxx          | 000q quuu                                |
| 84h           | FSR           | Indirect data memory address pointer                                                           |                    |        |                                                  |                  |                  |                  |                  | xxxx xxxx          | uuuu uuuu                                |
| 85h           | TRISA         | —                                                                                              | —                  | —      | TRISA4                                           | TRISA3           | TRISA2           | TRISA1           | TRISA0           | ---1 1111          | ---1 1111                                |
| 86h           | TRISB         | TRISB7                                                                                         | TRISB6             | TRISB5 | TRISB4                                           | TRISB3           | TRISB2           | TRISB1           | TRISB0           | 1111 1111          | 1111 1111                                |
| 87h-89h       | Unimplemented |                                                                                                |                    |        |                                                  |                  |                  |                  |                  | —                  | —                                        |
| 8Ah           | PCLATH        | —                                                                                              | —                  | —      | Write buffer for upper 5 bits of program counter |                  |                  |                  |                  | ---0 0000          | ---0 0000                                |
| 8Bh           | INTCON        | GIE                                                                                            | PEIE               | TOIE   | INTE                                             | RBIE             | TOIF             | INTF             | RBIF             | 0000 000x          | 0000 000u                                |
| 8Ch           | PIE1          | —                                                                                              | CMIE               | —      | —                                                | —                | —                | —                | —                | -0-- ----          | -0-- ----                                |
| 8Dh           | Unimplemented |                                                                                                |                    |        |                                                  |                  |                  |                  |                  | —                  | —                                        |
| 8Eh           | PCON          | —                                                                                              | —                  | —      | —                                                | —                | —                | POR              | $\overline{BOR}$ | ---- -0x           | ---- -uq                                 |
| 8Fh-9Eh       | Unimplemented |                                                                                                |                    |        |                                                  |                  |                  |                  |                  | —                  | —                                        |
| 9Fh           | VRCON         | VREN                                                                                           | VROE               | VRR    | —                                                | VR3              | VR2              | VR1              | VR0              | 000- 0000          | 000- 0000                                |

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown,  
q = value depends on condition, shaded = unimplemented

**Note 1:** Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

**2:** IRP & RP1 bits are reserved; always maintain these bits clear.



# PIC16C62X

**TABLE 7-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE**

| Address | Name   | Bit 7 | Bit 6 | Bit 5 | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  | Value on POR | Value on All Other RESETS |
|---------|--------|-------|-------|-------|--------|--------|--------|--------|--------|--------------|---------------------------|
| 1Fh     | CMCON  | C2OUT | C1OUT | —     | —      | CIS    | CM2    | CM1    | CM0    | 00-- 0000    | 00-- 0000                 |
| 9Fh     | VRCON  | VREN  | VROE  | VRR   | —      | VR3    | VR2    | VR1    | VR0    | 000- 0000    | 000- 0000                 |
| 0Bh     | INTCON | GIE   | PEIE  | T0IE  | INTE   | RBIE   | T0IF   | INTF   | RBIF   | 0000 000x    | 0000 000u                 |
| 0Ch     | PIR1   | —     | CMIF  | —     | —      | —      | —      | —      | —      | -0-- ----    | -0-- ----                 |
| 8Ch     | PIE1   | —     | CMIE  | —     | —      | —      | —      | —      | —      | -0-- ----    | -0-- ----                 |
| 85h     | TRISA  | —     | —     | —     | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | ---1 1111    | ---1 1111                 |

Legend: x = unknown, u = unchanged, - = unimplemented, read as "0"

## 9.3 RESET

The PIC16C62X differentiates between various kinds of RESET:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$  Reset during normal operation
- $\overline{\text{MCLR}}$  Reset during SLEEP
- WDT Reset (normal operation)
- WDT wake-up (SLEEP)
- Brown-out Reset (BOR)

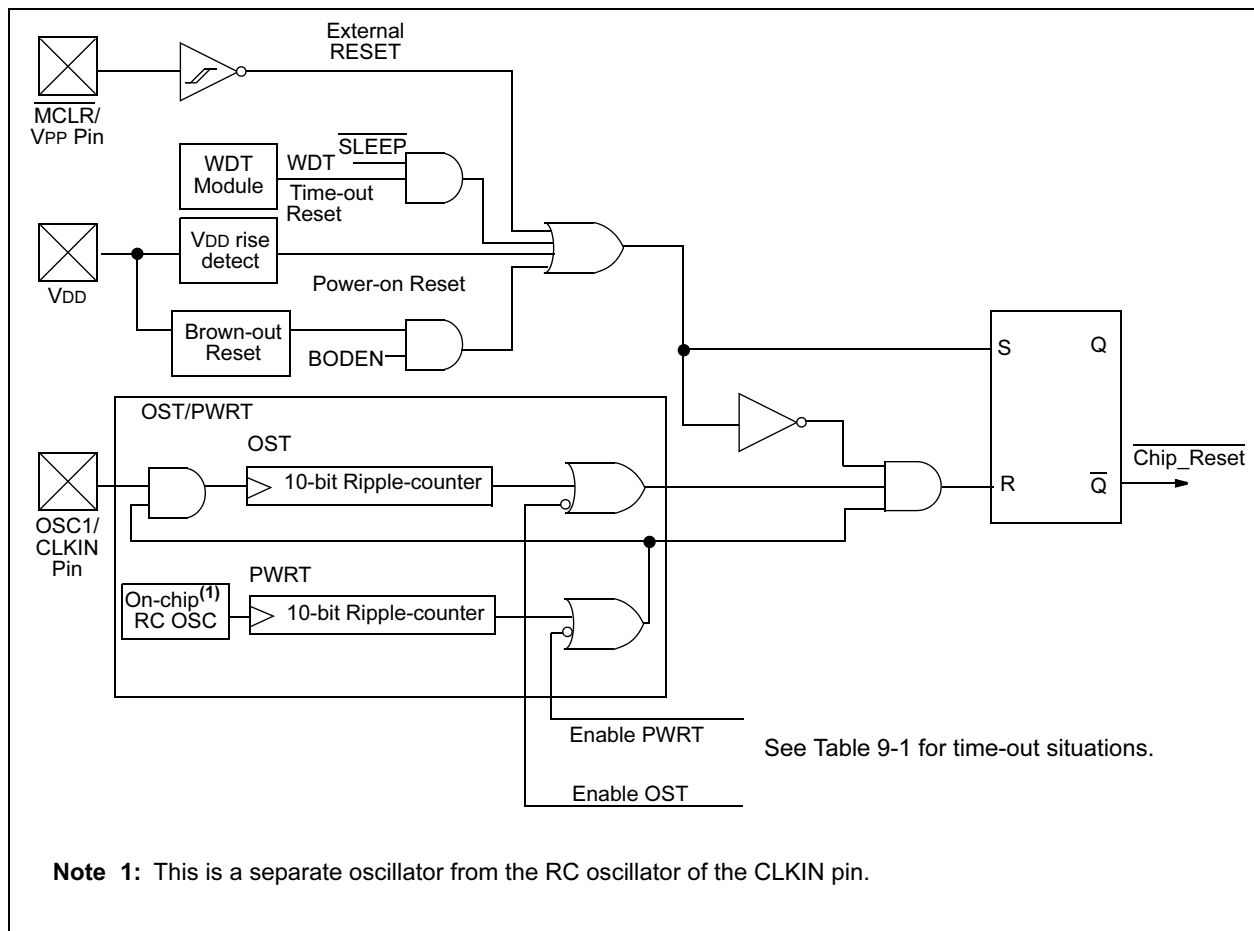
Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset,

$\overline{\text{MCLR}}$  Reset, WDT Reset and  $\overline{\text{MCLR}}$  Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation.  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are set or cleared differently in different RESET situations as indicated in Table 9-2. These bits are used in software to determine the nature of the RESET. See Table 9-5 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 9-6.

The  $\overline{\text{MCLR}}$  Reset path has a noise filter to detect and ignore small pulses. See Table 12-5 for pulse width specification.

**FIGURE 9-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**



# PIC16C62X

**TABLE 9-4: INITIALIZATION CONDITION FOR SPECIAL REGISTERS**

| Condition                          | Program Counter       | STATUS Register | PCON Register |
|------------------------------------|-----------------------|-----------------|---------------|
| Power-on Reset                     | 000h                  | 0001 1xxx       | ---- --0x     |
| MCLR Reset during normal operation | 000h                  | 000u uuuu       | ---- --uu     |
| MCLR Reset during SLEEP            | 000h                  | 0001 0uuu       | ---- --uu     |
| WDT Reset                          | 000h                  | 0000 uuuu       | ---- --uu     |
| WDT Wake-up                        | PC + 1                | uuu0 0uuu       | ---- --uu     |
| Brown-out Reset                    | 000h                  | 000x xuuu       | ---- --u0     |
| Interrupt Wake-up from SLEEP       | PC + 1 <sup>(1)</sup> | uuu1 0uuu       | ---- --uu     |

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

**TABLE 9-5: INITIALIZATION CONDITION FOR REGISTERS**

| Register | Address | Power-on Reset | <ul style="list-style-type: none"> <li>• MCLR Reset during normal operation</li> <li>• MCLR Reset during SLEEP</li> <li>• WDT Reset</li> <li>• Brown-out Reset <sup>(1)</sup></li> </ul> | <ul style="list-style-type: none"> <li>• Wake-up from SLEEP through interrupt</li> <li>• Wake-up from SLEEP through WDT time-out</li> </ul> |
|----------|---------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| W        | —       | xxxx xxxx      | uuuu uuuu                                                                                                                                                                                | uuuu uuuu                                                                                                                                   |
| INDF     | 00h     | —              | —                                                                                                                                                                                        | —                                                                                                                                           |
| TMR0     | 01h     | xxxx xxxx      | uuuu uuuu                                                                                                                                                                                | uuuu uuuu                                                                                                                                   |
| PCL      | 02h     | 0000 0000      | 0000 0000                                                                                                                                                                                | PC + 1 <sup>(3)</sup>                                                                                                                       |
| STATUS   | 03h     | 0001 1xxx      | 000q quuu <sup>(4)</sup>                                                                                                                                                                 | uuuq quuu <sup>(4)</sup>                                                                                                                    |
| FSR      | 04h     | xxxx xxxx      | uuuu uuuu                                                                                                                                                                                | uuuu uuuu                                                                                                                                   |
| PORTA    | 05h     | --x xxxx       | --u uuuu                                                                                                                                                                                 | --u uuuu                                                                                                                                    |
| PORTB    | 06h     | xxxx xxxx      | uuuu uuuu                                                                                                                                                                                | uuuu uuuu                                                                                                                                   |
| CMCON    | 1Fh     | 00-- 0000      | 00-- 0000                                                                                                                                                                                | uu-- uuuu                                                                                                                                   |
| PCLATH   | 0Ah     | ---0 0000      | ---0 0000                                                                                                                                                                                | ---u uuuu                                                                                                                                   |
| INTCON   | 0Bh     | 0000 000x      | 0000 000u                                                                                                                                                                                | uuuu uqqq <sup>(2)</sup>                                                                                                                    |
| PIR1     | 0Ch     | -0-- ----      | -0-- ----                                                                                                                                                                                | -q-- ---- <sup>(2,5)</sup>                                                                                                                  |
| OPTION   | 81h     | 1111 1111      | 1111 1111                                                                                                                                                                                | uuuu uuuu                                                                                                                                   |
| TRISA    | 85h     | ---1 1111      | ---1 1111                                                                                                                                                                                | ---u uuuu                                                                                                                                   |
| TRISB    | 86h     | 1111 1111      | 1111 1111                                                                                                                                                                                | uuuu uuuu                                                                                                                                   |
| PIE1     | 8Ch     | -0-- ----      | -0-- ----                                                                                                                                                                                | -u-- ----                                                                                                                                   |
| PCON     | 8Eh     | ---- --0x      | ---- --uq <sup>(1,6)</sup>                                                                                                                                                               | ---- --uu                                                                                                                                   |
| VRCON    | 9Fh     | 000- 0000      | 000- 0000                                                                                                                                                                                | uuu- uuuu                                                                                                                                   |

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 9-4 for RESET value for specific condition.

**5:** If wake-up was due to comparator input changing, then bit 6 = 1. All other interrupts generating a wake-up will cause bit 6 = u.

**6:** If RESET was due to brown-out, then bit 0 = 0. All other RESETS will cause bit 0 = u.

## 9.5 Interrupts

The PIC16C62X has 4 sources of interrupt:

- External interrupt RB0/INT
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB<7:4>)
- Comparator interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on RESET.

The “return from interrupt” instruction, RETFIE, exits interrupt routine, as well as sets the GIE bit, which re-enable RB0/INT interrupts.

The INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flag is contained in the special register PIR1. The corresponding interrupt enable bit is contained in special registers PIE1.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h.

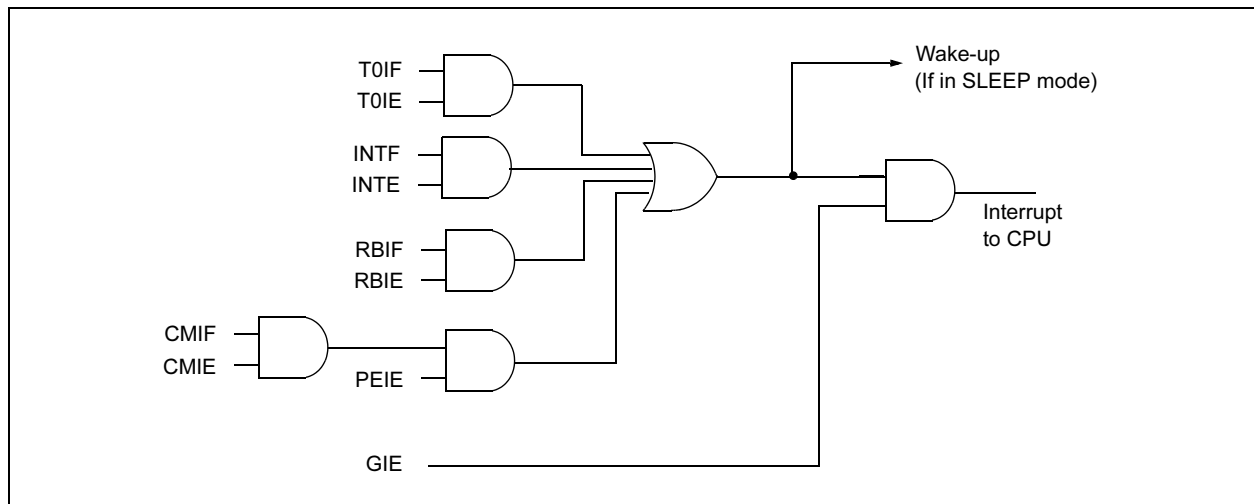
Once in the interrupt service routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid RB0/INT recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 9-16). The latency is the same for one or two cycle instructions. Once in the interrupt service routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

**Note 1:** Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

**2:** When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The CPU will execute a NOP in the cycle immediately following the instruction which clears the GIE bit. The interrupts which were ignored are still pending to be serviced when the GIE bit is set again.

**FIGURE 9-15: INTERRUPT LOGIC**



# PIC16C62X

## 9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

### 9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see

DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

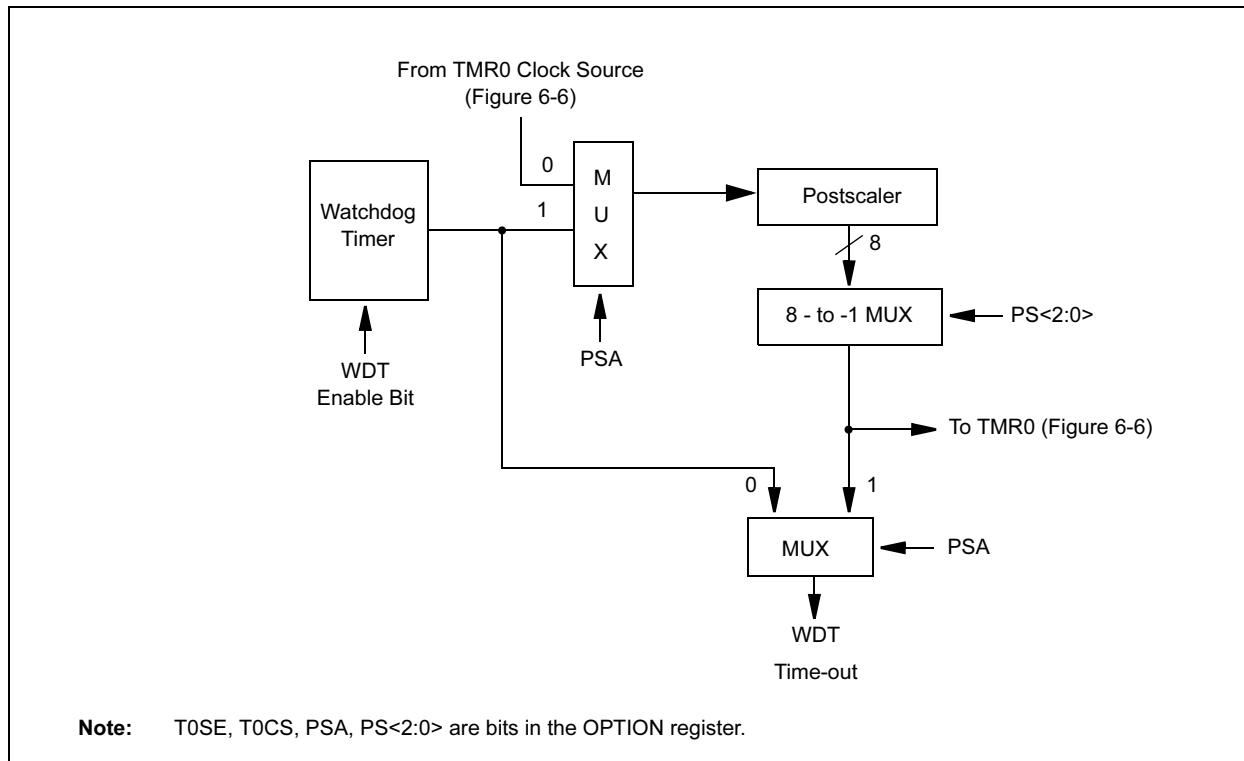
The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The  $\overline{\text{TO}}$  bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

### 9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

**FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM**



**TABLE 9-7: SUMMARY OF WATCHDOG TIMER REGISTERS**

| Address | Name         | Bit 7 | Bit 6  | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR Reset | Value on all other RESETS |
|---------|--------------|-------|--------|-------|-------|-------|-------|-------|-------|--------------------|---------------------------|
| 2007h   | Config. bits | —     | BODEN  | CP1   | CP0   | PWRTE | WDTE  | FOSC1 | FOSC0 | —                  | —                         |
| 81h     | OPTION       | RBPU  | INTEDG | T0CS  | T0SE  | PSA   | PS2   | PS1   | PS0   | 1111 1111          | 1111 1111                 |

Legend: Shaded cells are not used by the Watchdog Timer.

**Note:** — = Unimplemented location, read as “0”  
+ = Reserved for future use

## 9.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit in the STATUS register is cleared, the TO bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS with no external circuitry drawing current from the I/O pin and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

**Note:** It should be noted that a RESET generated by a WDT time-out does not drive MCLR pin low.

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The  $\overline{TO}$  and  $\overline{PD}$  bits in the STATUS register can be used to determine the cause of device RESET. PD bit, which is set on power-up, is cleared when SLEEP is invoked.  $\overline{TO}$  bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

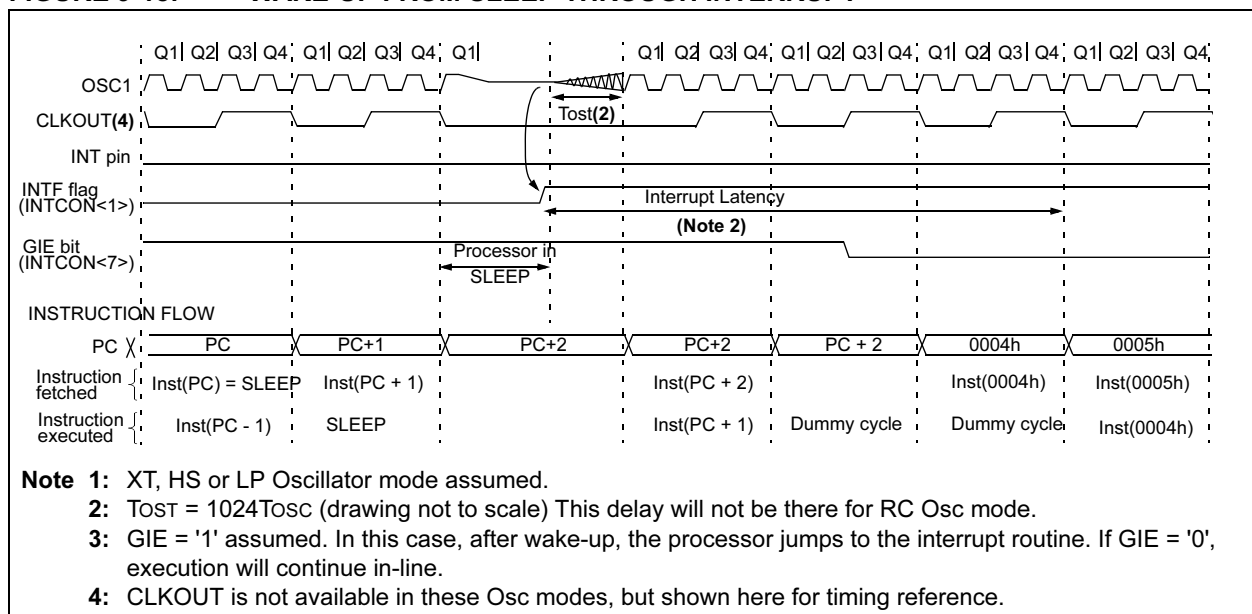
### 9.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External RESET input on MCLR pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

**FIGURE 9-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT**



# PIC16C62X

| BCF              |                                                                                                                                                        | Bit Clear f |      |  |    |      |      |      |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|--|----|------|------|------|
| Syntax:          | [ <i>label</i> ] BCF    f,b                                                                                                                            |             |      |  |    |      |      |      |
| Operands:        | $0 \leq f \leq 127$<br>$0 \leq b \leq 7$                                                                                                               |             |      |  |    |      |      |      |
| Operation:       | $0 \rightarrow (f<b>)$                                                                                                                                 |             |      |  |    |      |      |      |
| Status Affected: | None                                                                                                                                                   |             |      |  |    |      |      |      |
| Encoding:        | <table border="1"><tr><td>01</td><td>00bb</td><td>bfff</td><td>ffff</td></tr></table>                                                                  |             |      |  | 01 | 00bb | bfff | ffff |
| 01               | 00bb                                                                                                                                                   | bfff        | ffff |  |    |      |      |      |
| Description:     | Bit 'b' in register 'f' is cleared.                                                                                                                    |             |      |  |    |      |      |      |
| Words:           | 1                                                                                                                                                      |             |      |  |    |      |      |      |
| Cycles:          | 1                                                                                                                                                      |             |      |  |    |      |      |      |
| Example          | <div>BCF            FLAG_REG, 7</div> <div>Before Instruction</div> <div>FLAG_REG = 0xC7</div> <div>After Instruction</div> <div>FLAG_REG = 0x47</div> |             |      |  |    |      |      |      |

| BSF              |                                          | Bit Set f |      |      |  |
|------------------|------------------------------------------|-----------|------|------|--|
| Syntax:          | [ <i>label</i> ] BSF f,b                 |           |      |      |  |
| Operands:        | $0 \leq f \leq 127$<br>$0 \leq b \leq 7$ |           |      |      |  |
| Operation:       | $1 \rightarrow (f<b>)$                   |           |      |      |  |
| Status Affected: | None                                     |           |      |      |  |
| Encoding:        | 01                                       | 01bb      | bfff | ffff |  |
| Description:     | Bit 'b' in register 'f' is set.          |           |      |      |  |
| Words:           | 1                                        |           |      |      |  |
| Cycles:          | 1                                        |           |      |      |  |
| Example          | BSF FLAG_REG, 7                          |           |      |      |  |
|                  | Before Instruction                       |           |      |      |  |
|                  | FLAG_REG = 0x0A                          |           |      |      |  |
|                  | After Instruction                        |           |      |      |  |
|                  | FLAG_REG = 0x8A                          |           |      |      |  |

| BTFSC            |                                                                                                                                                                                                                                                             | Bit Test, Skip if Clear      |                            |      |  |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|----------------------------|------|--|
| Syntax:          | [ <i>label</i> ] BTFSC f,b                                                                                                                                                                                                                                  |                              |                            |      |  |
| Operands:        | $0 \leq f \leq 127$<br>$0 \leq b \leq 7$                                                                                                                                                                                                                    |                              |                            |      |  |
| Operation:       | skip if (f<b>) = 0                                                                                                                                                                                                                                          |                              |                            |      |  |
| Status Affected: | None                                                                                                                                                                                                                                                        |                              |                            |      |  |
| Encoding:        | 01                                                                                                                                                                                                                                                          | 10bb                         | bfff                       | ffff |  |
| Description:     | If bit 'b' in register 'f' is '0', then the next instruction is skipped.<br>If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction. |                              |                            |      |  |
| Words:           | 1                                                                                                                                                                                                                                                           |                              |                            |      |  |
| Cycles:          | 1(2)                                                                                                                                                                                                                                                        |                              |                            |      |  |
| Example          | HERE<br>FALSE<br>TRUE                                                                                                                                                                                                                                       | BTFSC<br>GOTO<br>•<br>•<br>• | FLAG,1<br>PROCESS_CO<br>DE |      |  |

Before Instruction  
PC = address HERE

After Instruction  
if FLAG<1> = 0,  
PC = address TRUE  
if FLAG<1> = 1,  
PC = address FALSE

| MOVF             |                                                                                                                                                                                                                                                         | Move f |      |  |    |      |      |      |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------|--|----|------|------|------|
| Syntax:          | [ <i>label</i> ] MOVF f,d                                                                                                                                                                                                                               |        |      |  |    |      |      |      |
| Operands:        | $0 \leq f \leq 127$<br>$d \in [0,1]$                                                                                                                                                                                                                    |        |      |  |    |      |      |      |
| Operation:       | (f) $\rightarrow$ (dest)                                                                                                                                                                                                                                |        |      |  |    |      |      |      |
| Status Affected: | Z                                                                                                                                                                                                                                                       |        |      |  |    |      |      |      |
| Encoding:        | <table border="1"><tr><td>00</td><td>1000</td><td>dfff</td><td>ffff</td></tr></table>                                                                                                                                                                   |        |      |  | 00 | 1000 | dfff | ffff |
| 00               | 1000                                                                                                                                                                                                                                                    | dfff   | ffff |  |    |      |      |      |
| Description:     | The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected. |        |      |  |    |      |      |      |
| Words:           | 1                                                                                                                                                                                                                                                       |        |      |  |    |      |      |      |
| Cycles:          | 1                                                                                                                                                                                                                                                       |        |      |  |    |      |      |      |
| Example          | MOVF FSR, 0                                                                                                                                                                                                                                             |        |      |  |    |      |      |      |
|                  | After Instruction                                                                                                                                                                                                                                       |        |      |  |    |      |      |      |
|                  | W = value in FSR                                                                                                                                                                                                                                        |        |      |  |    |      |      |      |
|                  | register                                                                                                                                                                                                                                                |        |      |  |    |      |      |      |
|                  | Z = 1                                                                                                                                                                                                                                                   |        |      |  |    |      |      |      |

| MOVWF            |                                            | Move W to f |      |      |  |
|------------------|--------------------------------------------|-------------|------|------|--|
| Syntax:          | [ <i>label</i> ] MOVWF f                   |             |      |      |  |
| Operands:        | $0 \leq f \leq 127$                        |             |      |      |  |
| Operation:       | (W) → (f)                                  |             |      |      |  |
| Status Affected: | None                                       |             |      |      |  |
| Encoding:        | 00                                         | 0000        | 1fff | ffff |  |
| Description:     | Move data from W register to register 'f'. |             |      |      |  |
| Words:           | 1                                          |             |      |      |  |
| Cycles:          | 1                                          |             |      |      |  |
| Example          | MOVWF OPTION                               |             |      |      |  |
|                  | Before Instruction                         |             |      |      |  |
|                  | OPTION                                     | =           | 0xFF |      |  |
|                  | W                                          | =           | 0x4F |      |  |
|                  | After Instruction                          |             |      |      |  |
|                  | OPTION                                     | =           | 0x4F |      |  |
|                  | W                                          | =           | 0x4F |      |  |

| NOP              | No Operation         |      |      |      |
|------------------|----------------------|------|------|------|
| Syntax:          | [ <i>label</i> ] NOP |      |      |      |
| Operands:        | None                 |      |      |      |
| Operation:       | No operation         |      |      |      |
| Status Affected: | None                 |      |      |      |
| Encoding:        | 00                   | 0000 | 0xx0 | 0000 |
| Description:     | No operation.        |      |      |      |
| Words:           | 1                    |      |      |      |
| Cycles:          | 1                    |      |      |      |
| Example          | NOP                  |      |      |      |

| OPTION           | Load Option Register                                                                                                                                                                                                                         |      |      |      |      |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| Syntax:          | [ <i>label</i> ] OPTION                                                                                                                                                                                                                      |      |      |      |      |
| Operands:        | None                                                                                                                                                                                                                                         |      |      |      |      |
| Operation:       | (W) → OPTION                                                                                                                                                                                                                                 |      |      |      |      |
| Status Affected: | None                                                                                                                                                                                                                                         |      |      |      |      |
| Encoding:        | <table><tr><td>00</td><td>0000</td><td>0110</td><td>0010</td></tr></table>                                                                                                                                                                   | 00   | 0000 | 0110 | 0010 |
| 00               | 0000                                                                                                                                                                                                                                         | 0110 | 0010 |      |      |
| Description:     | <p>The contents of the W register are loaded in the OPTION register.</p> <p>This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.</p> |      |      |      |      |
| Words:           | 1                                                                                                                                                                                                                                            |      |      |      |      |
| Cycles:          | 1                                                                                                                                                                                                                                            |      |      |      |      |
| Example          | <div><b>To maintain upward compatibility with future PICmicro<sup>®</sup> products, do not use this instruction.</b></div>                                                                                                                   |      |      |      |      |

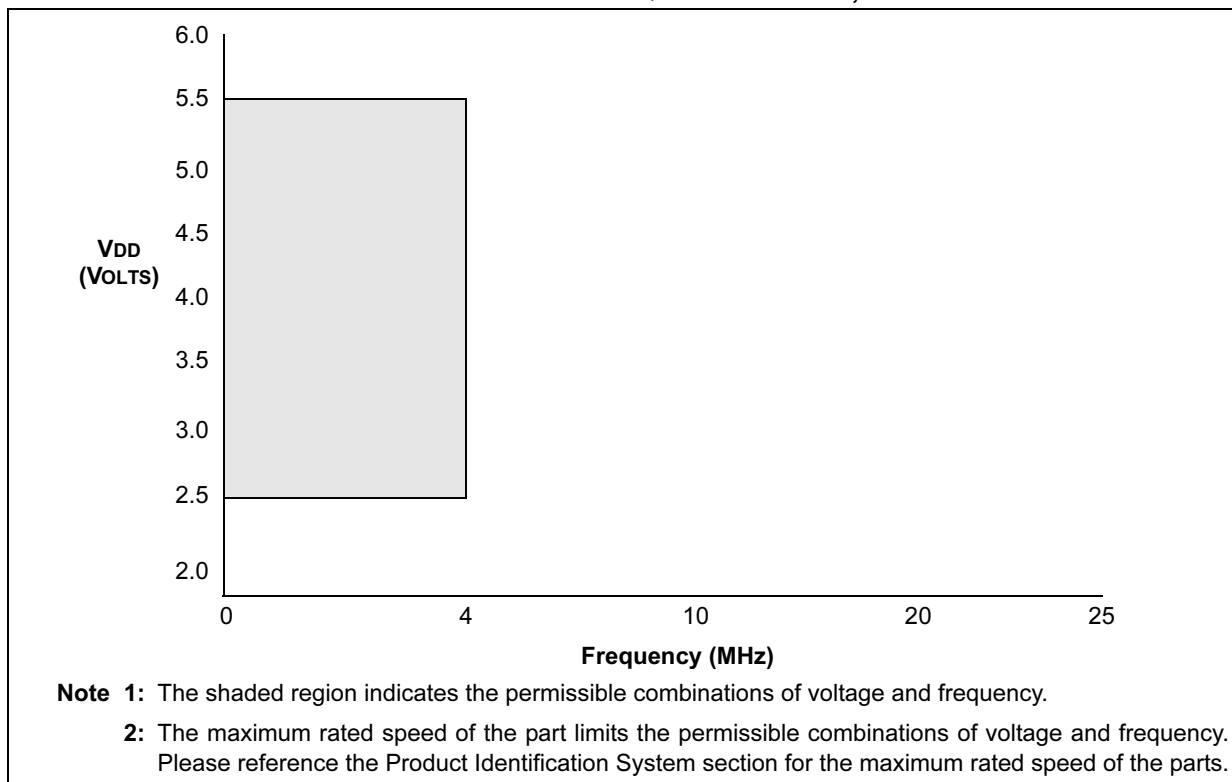
# PIC16C62X

---

NOTES:

# PIC16C62X

**FIGURE 12-9: PIC16LCR62XA VOLTAGE-FREQUENCY GRAPH,  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$**



# PIC16C62X

## 12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended)

| PIC16C62XA  |      | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and<br>$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended |       |      |      |       |                                              |
|-------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|-------|----------------------------------------------|
| PIC16LC62XA |      | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and<br>$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended |       |      |      |       |                                              |
| Param. No.  | Sym  | Characteristic                                                                                                                                                                                                                                                                                                   | Min   | Typ† | Max  | Units | Conditions                                   |
| D001        | VDD  | Supply Voltage                                                                                                                                                                                                                                                                                                   | 3.0   | —    | 5.5  | V     | See Figures 12-1, 12-2, 12-3, 12-4, and 12-5 |
| D001        | VDD  | Supply Voltage                                                                                                                                                                                                                                                                                                   | 2.5   | —    | 5.5  | V     | See Figures 12-1, 12-2, 12-3, 12-4, and 12-5 |
| D002        | VDR  | RAM Data Retention Voltage <sup>(1)</sup>                                                                                                                                                                                                                                                                        | —     | 1.5* | —    | V     | Device in SLEEP mode                         |
| D002        | VDR  | RAM Data Retention Voltage <sup>(1)</sup>                                                                                                                                                                                                                                                                        | —     | 1.5* | —    | V     | Device in SLEEP mode                         |
| D003        | VPOR | VDD start voltage to ensure Power-on Reset                                                                                                                                                                                                                                                                       | —     | VSS  | —    | V     | See section on Power-on Reset for details    |
| D003        | VPOR | VDD start voltage to ensure Power-on Reset                                                                                                                                                                                                                                                                       | —     | VSS  | —    | V     | See section on Power-on Reset for details    |
| D004        | SVDD | VDD rise rate to ensure Power-on Reset                                                                                                                                                                                                                                                                           | 0.05* | —    | —    | V/ms  | See section on Power-on Reset for details    |
| D004        | SVDD | VDD rise rate to ensure Power-on Reset                                                                                                                                                                                                                                                                           | 0.05* | —    | —    | V/ms  | See section on Power-on Reset for details    |
| D005        | VBOR | Brown-out Detect Voltage                                                                                                                                                                                                                                                                                         | 3.7   | 4.0  | 4.35 | V     | BOREN configuration bit is cleared           |
| D005        | VBOR | Brown-out Detect Voltage                                                                                                                                                                                                                                                                                         | 3.7   | 4.0  | 4.35 | V     | BOREN configuration bit is cleared           |

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

**4:** For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula:  $I_r = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.

**5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**6:** Commercial temperature range only.

# PIC16C62X

## 12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40<sup>(7)</sup> (Commercial) PIC16CR620A-40<sup>(7)</sup> (Commercial)

| DC CHARACTERISTICS |                   |                                                                            | Standard Operating Conditions (unless otherwise stated) |        |                                                |        |                                                                                                                               |
|--------------------|-------------------|----------------------------------------------------------------------------|---------------------------------------------------------|--------|------------------------------------------------|--------|-------------------------------------------------------------------------------------------------------------------------------|
|                    |                   |                                                                            | Operating temperature 0°C ≤ TA ≤ +70°C for commercial   |        |                                                |        |                                                                                                                               |
| Param No.          | Sym               | Characteristic                                                             | Min                                                     | Typ†   | Max                                            | Unit   | Conditions                                                                                                                    |
| D030               | V <sub>IL</sub>   | <b>Input Low Voltage</b><br>I/O ports<br>with TTL buffer                   | V <sub>SS</sub>                                         | —      | 0.8V<br>0.15V <sub>DD</sub>                    | V      | V <sub>DD</sub> = 4.5V to 5.5V, otherwise                                                                                     |
| D031               |                   | with Schmitt Trigger input                                                 | V <sub>SS</sub>                                         | —      | 0.2V <sub>DD</sub>                             | V      | (Note 1)                                                                                                                      |
| D032               |                   | MCLR, RA4/T0CKI, OSC1<br>(in RC mode)                                      | V <sub>SS</sub>                                         | —      | 0.2V <sub>DD</sub>                             | V      |                                                                                                                               |
| D033               |                   | OSC1 (in XT and HS)<br>OSC1 (in LP)                                        | V <sub>SS</sub><br>V <sub>SS</sub>                      | —<br>— | 0.3V <sub>DD</sub><br>0.6V <sub>DD</sub> - 1.0 | V<br>V |                                                                                                                               |
| D040               | V <sub>IH</sub>   | <b>Input High Voltage</b><br>I/O ports<br>with TTL buffer                  | 2.0V<br>0.25 V <sub>DD</sub> + 0.8                      | —      | V <sub>DD</sub><br>V <sub>DD</sub>             | V      | V <sub>DD</sub> = 4.5V to 5.5V, otherwise                                                                                     |
| D041               |                   | with Schmitt Trigger input                                                 | 0.8 V <sub>DD</sub>                                     | —      | V <sub>DD</sub>                                | V      | (Note 1)                                                                                                                      |
| D042               |                   | MCLR RA4/T0CKI                                                             | 0.8 V <sub>DD</sub>                                     | —      | V <sub>DD</sub>                                | V      |                                                                                                                               |
| D043               |                   | OSC1 (XT, HS and LP)                                                       | 0.7 V <sub>DD</sub>                                     | —      | V <sub>DD</sub>                                | V      |                                                                                                                               |
| D043A              |                   | OSC1 (in RC mode)                                                          | 0.9 V <sub>DD</sub>                                     | —      |                                                |        | (Note 1)                                                                                                                      |
| D070               | IPURB             | <b>PORTB Weak Pull-up Current</b>                                          | 50                                                      | 200    | 400                                            | μA     | V <sub>DD</sub> = 5.0V, V <sub>PIN</sub> = V <sub>SS</sub>                                                                    |
| D060               | I <sub>IL</sub>   | <b>Input Leakage Current</b> <sup>(2, 3)</sup><br>I/O ports (except PORTA) | —                                                       | —      | ±1.0                                           | μA     | V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , pin at hi-impedance                                                    |
| D061               |                   | PORTA                                                                      | —                                                       | —      | ±0.5                                           | μA     | V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , pin at hi-impedance                                                    |
| D063               |                   | RA4/T0CKI                                                                  | —                                                       | —      | ±1.0                                           | μA     | V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub>                                                                          |
|                    |                   | OSC1, MCLR                                                                 | —                                                       | —      | ±5.0                                           | μA     | V <sub>SS</sub> ≤ V <sub>PIN</sub> ≤ V <sub>DD</sub> , XT, HS and LP osc configuration                                        |
| D080               | V <sub>OL</sub>   | <b>Output Low Voltage</b><br>I/O ports                                     | —                                                       | —      | 0.6                                            | V      | I <sub>OL</sub> = 8.5 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C                                                               |
|                    |                   |                                                                            | —                                                       | —      | 0.6                                            | V      | I <sub>OL</sub> = 7.0 mA, V <sub>DD</sub> = 4.5V, +125°C                                                                      |
| D083               |                   | OSC2/CLKOUT (RC only)                                                      | —                                                       | —      | 0.6                                            | V      | I <sub>OL</sub> = 1.6 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C                                                               |
|                    |                   |                                                                            | —                                                       | —      | 0.6                                            | V      | I <sub>OL</sub> = 1.2 mA, V <sub>DD</sub> = 4.5V, +125°C                                                                      |
| D090               | V <sub>OH</sub>   | <b>Output High Voltage</b> <sup>(3)</sup><br>I/O ports (except RA4)        | V <sub>DD</sub> -0.7<br>V <sub>DD</sub> -0.7            | —<br>— | —<br>—                                         | V<br>V | I <sub>OH</sub> = -3.0 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C<br>I <sub>OH</sub> = -2.5 mA, V <sub>DD</sub> = 4.5V, +125°C |
| D092               |                   | OSC2/CLKOUT (RC only)                                                      | V <sub>DD</sub> -0.7<br>V <sub>DD</sub> -0.7            | —<br>— | —<br>—                                         | V<br>V | I <sub>OH</sub> = -1.3 mA, V <sub>DD</sub> = 4.5V, -40° to +85°C<br>I <sub>OH</sub> = -1.0 mA, V <sub>DD</sub> = 4.5V, +125°C |
| *D150              | V <sub>OD</sub>   | <b>Open Drain High Voltage</b>                                             |                                                         |        | 8.5                                            | V      | RA4 pin                                                                                                                       |
| D100               | C <sub>osc2</sub> | <b>Capacitive Loading Specs on Output Pins</b><br>OSC2 pin                 |                                                         |        | 15                                             | pF     | In XT, HS and LP modes when external clock used to drive OSC1.                                                                |
| D101               | C <sub>io</sub>   | All I/O pins/OSC2 (in RC mode)                                             |                                                         |        | 50                                             | pF     |                                                                                                                               |

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which V<sub>DD</sub> can be lowered in SLEEP mode without losing RAM data.

**Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I<sub>DD</sub> measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V<sub>DD</sub>, MCLR = V<sub>DD</sub>; WDT enabled/disabled as specified.

**Note 3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V<sub>DD</sub> or V<sub>SS</sub>.

**Note 4:** For RC osc configuration, current through R<sub>EXT</sub> is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD} / 2R_{EXT}$  (mA) with R<sub>EXT</sub> in kΩ.

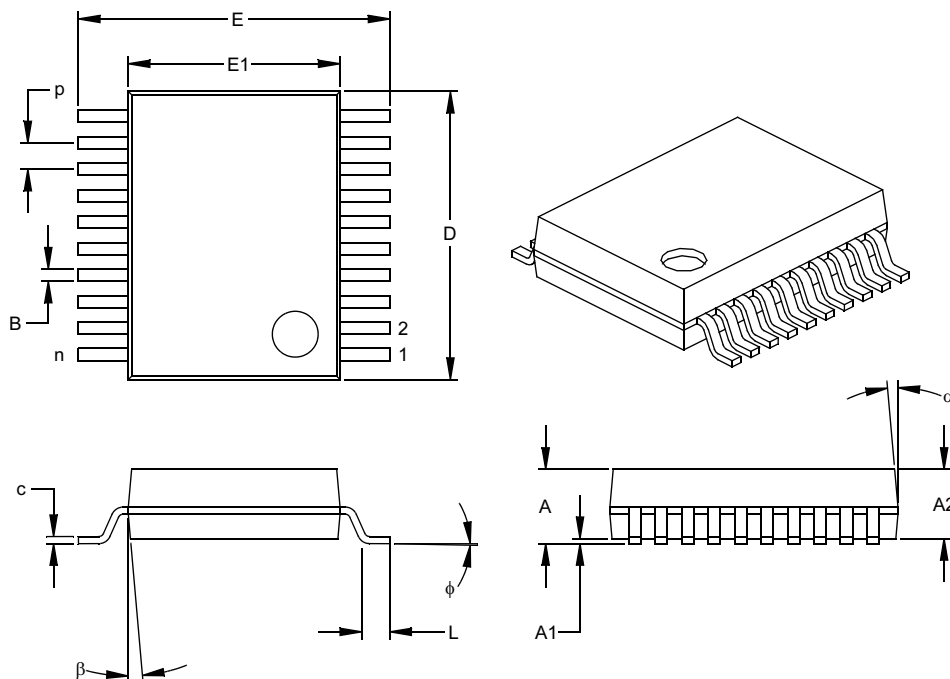
**Note 5:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I<sub>DD</sub> or I<sub>PD</sub> measurement.

**Note 6:** Commercial temperature range only.

**Note 7:** See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

# PIC16C62X

## 20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)



| Units                    |    | INCHES* |      |      | MILLIMETERS |        |        |
|--------------------------|----|---------|------|------|-------------|--------|--------|
| Dimension Limits         |    | MIN     | NOM  | MAX  | MIN         | NOM    | MAX    |
| Number of Pins           | n  |         | 20   |      |             | 20     |        |
| Pitch                    | p  |         | .026 |      |             | 0.65   |        |
| Overall Height           | A  | .068    | .073 | .078 | 1.73        | 1.85   | 1.98   |
| Molded Package Thickness | A2 | .064    | .068 | .072 | 1.63        | 1.73   | 1.83   |
| Standoff §               | A1 | .002    | .006 | .010 | 0.05        | 0.15   | 0.25   |
| Overall Width            | E  | .299    | .309 | .322 | 7.59        | 7.85   | 8.18   |
| Molded Package Width     | E1 | .201    | .207 | .212 | 5.11        | 5.25   | 5.38   |
| Overall Length           | D  | .278    | .284 | .289 | 7.06        | 7.20   | 7.34   |
| Foot Length              | L  | .022    | .030 | .037 | 0.56        | 0.75   | 0.94   |
| Lead Thickness           | c  | .004    | .007 | .010 | 0.10        | 0.18   | 0.25   |
| Foot Angle               | φ  | 0       | 4    | 8    | 0.00        | 101.60 | 203.20 |
| Lead Width               | B  | .010    | .013 | .015 | 0.25        | 0.32   | 0.38   |
| Mold Draft Angle Top     | α  | 0       | 5    | 10   | 0           | 5      | 10     |
| Mold Draft Angle Bottom  | β  | 0       | 5    | 10   | 0           | 5      | 10     |

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-150

Drawing No. C04-072

# PIC16C62X

---

## N

NOP Instruction..... 69

## O

One-Time-Programmable (OTP) Devices..... 7

OPTION Instruction..... 69

OPTION Register..... 19

Oscillator Configurations..... 47

Oscillator Start-up Timer (OST)..... 50

## P

Package Marking Information..... 117

Packaging Information..... 113

PCL and PCLATH..... 23

PCON Register..... 22

PICKit 1 FLASH Starter Kit..... 79

PICSTART Plus Development Programmer..... 77

PIE1 Register..... 21

PIR1 Register..... 21

Port RB Interrupt..... 56

PORTA..... 25

PORTB..... 28

Power Control/Status Register (PCON)..... 51

Power-Down Mode (SLEEP)..... 59

Power-On Reset (POR)..... 50

Power-up Timer (PWRT)..... 50

Prescaler..... 34

PRO MATE II Universal Device Programmer..... 77

Program Memory Organization..... 13

## Q

Quick-Turnaround-Production (QTP) Devices..... 7

## R

RC Oscillator..... 48

Reset..... 49

RETFIE Instruction..... 70

RETLW Instruction..... 70

RETURN Instruction..... 70

RLF Instruction..... 71

RRF Instruction..... 71

## S

Serialized Quick-Turnaround-Production (SQTP) Devices... 7

SLEEP Instruction..... 71

Software Simulator (MPLAB SIM)..... 76

Software Simulator (MPLAB SIM30)..... 76

Special Features of the CPU..... 45

Special Function Registers..... 17

Stack..... 23

Status Register..... 18

SUBLW Instruction..... 72

SUBWF Instruction..... 72

SWAPF Instruction..... 73

## T

Timer0

TIMER0..... 31

TIMER0 (TMR0) Interrupt..... 31

TIMER0 (TMR0) Module..... 31

TMR0 with External Clock..... 33

Timer1

Switching Prescaler Assignment..... 35

Timing Diagrams and Specifications..... 104

TMR0 Interrupt..... 56

TRIS Instruction..... 73

TRISA..... 25

TRISB..... 28

## V

Voltage Reference Module..... 43

VRCON Register..... 43

## W

Watchdog Timer (WDT)..... 58

WWW, On-Line Support..... 3

## X

XORLW Instruction..... 73

XORWF Instruction..... 73

## ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

### Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

**[www.microchip.com](http://www.microchip.com)**

The file transfer site is available by using an FTP service to connect to:

**<ftp://ftp.microchip.com>**

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

## SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

092002

# PIC16C62X

---

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager  
RE: Reader Response  
From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: PIC16C62X

Literature Number: DS30235J

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this document easy to follow? If not, why?

---

---

4. What additions to the document do you think would enhance the structure and subject?

---

---

5. What deletions from the document could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---