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#### Details

E-XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c621a-04-so

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## FIGURE 4-6: DATA MEMORY MAP FOR THE PIC16C620A/CR620A/621A

File Address	5		File Address		
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h		
01h	TMR0	OPTION	81h		
02h	PCL	PCL	82h		
03h	STATUS	STATUS	83h		
04h	FSR	FSR	84h		
05h	PORTA	TRISA	85h		
06h	PORTB	TRISB	86h		
07h			87h		
08h			88h		
09h			89h		
0Ah	PCLATH	PCLATH	8Ah		
0Bh	INTCON	INTCON	8Bh		
0Ch	PIR1	PIE1	8Ch		
0Dh			8Dh		
0Eh		PCON	8Eh		
0Fh			8Fh		
10h			90h		
11h			91h		
12h			92h		
13h			93h		
14h			94h		
15h			95h		
16h			96h		
17h			97h		
18h			98h		
19h			99h		
1Ah			9Ah		
1Bh			9Bh		
1Ch			9Ch		
1Dh			9Dh		
1Eh			9Eh		
1Fh	CMCON	VRCON	9Fh		
20h	General Purpose Register		A0h		
6Fh					
70h	General		F0h		
7011	Purpose	Accesses			
7Fh	Register	1011-1711	FFh		
	Bank 0	Bank 1			
Unimplemented data memory locations, read as '0'.					
Note 1:	<b>Note 1:</b> Not a physical register.				

#### FIGURE 4-7: DATA MEMORY MAP FOR THE PIC16C622A

File Address	;		File Address		
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h		
01h	TMR0	OPTION	81h		
02h	PCL	PCL	82h		
03h	STATUS	STATUS	83h		
04h	FSR	FSR	84h		
05h	PORTA	TRISA	85h		
06h	PORTB	TRISB	86h		
07h			87h		
08h			88h		
09h			89h		
0Ah	PCLATH	PCLATH	8Ah		
0Bh	INTCON	INTCON	8Bh		
0Ch	PIR1	PIE1	8Ch		
0Dh			8Dh		
0Eh		PCON	8Eh		
0Fh			8Fh		
10h			90h		
11h			91h		
12h			92h		
13h			93h		
14h			94h		
15h			95h		
16h			96h		
17h			97h		
18h			98h		
19h			99h		
1Ah			9Ah		
1Bh			9Bh		
1Ch			9Ch		
1Dn					
1En	014001		9En		
1Fn	CMCON	VRCON	9Fn		
20h	General	General	A0h		
	Purpose	Purpose			
	Register	Register	BFh		
			C0h		
			0011		
6Fh			– F0h		
70h	General	Accesses			
	Register	70h-7Fh	EEh		
/Fhl	Bank 0	Bank 1			
Unimplemented data memory locations, read as '0'.					
Note 1:	Note 1: Not a physical register.				

#### **OPTION Register** 4.2.2.2

The OPTION register is a readable and writable register, which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note:	To achieve a 1:1 prescaler assignment for
	TMR0, assign the prescaler to the WDT
	(PSA = 1).

REGISTER 4-2:	OPTION REGISTER (ADDRESS 81H)
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RBPU       INTEDG       TOCS       TOSE         bit 7         bit 7         RBPU: PORTB Pull-up Enable bit         1 = PORTB pull-ups are disabled         0 = PORTB pull-ups are enabled by individual por         bit 6         INTEDG: Interrupt Edge Select bit         1 = Interrupt on rising edge of RB0/INT pin         0 = Interrupt on falling edge of RB0/INT pin         0 = Interrupt on falling edge of RB0/INT pin         bit 5         TOCS: TMR0 Clock Source Select bit         1 = Transition on RA4/T0CKI pin         0 = Internal instruction cycle clock (CLKOUT)         bit 4         TOSE: TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3       PSA: Prescaler Assignment bit	PSA t latch va DCKI pin DCKI pin	PS2	PS1	PS0 bit 0
bit 7         RBPU: PORTB Pull-up Enable bit         1 = PORTB pull-ups are disabled         0 = PORTB pull-ups are enabled by individual por         bit 6         INTEDG: Interrupt Edge Select bit         1 = Interrupt on rising edge of RB0/INT pin         0 = Interrupt on falling edge of RB0/INT pin         0 = Interrupt on falling edge of RB0/INT pin         0 = Interrupt on RA4/T0CKI pin         0 = Internal instruction cycle clock (CLKOUT)         bit 4         TOSE: TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3	t latch va DCKI pin DCKI pin	alues		bit 0
bit 7       RBPU: PORTB Pull-up Enable bit         1 = PORTB pull-ups are disabled       0 = PORTB pull-ups are enabled by individual por         bit 6       INTEDG: Interrupt Edge Select bit         1 = Interrupt on rising edge of RB0/INT pin       0 = Interrupt on falling edge of RB0/INT pin         bit 5       TOCS: TMR0 Clock Source Select bit         1 = Transition on RA4/T0CKI pin       0 = Internal instruction cycle clock (CLKOUT)         bit 4       TOSE: TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3       PSA: Prescaler Assignment bit	t latch va DCKI pin DCKI pin	alues		
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<ul> <li>bit 6</li> <li>INTEDG: Interrupt Edge Select bit         <ol> <li>Interrupt on rising edge of RB0/INT pin</li> <li>Interrupt on falling edge of RB0/INT pin</li> <li>Interrupt on falling edge of RB0/INT pin</li> </ol> </li> <li>bit 5</li> <li>TOCS: TMR0 Clock Source Select bit         <ol> <li>Transition on RA4/T0CKI pin</li> <li>Internal instruction cycle clock (CLKOUT)</li> </ol> </li> <li>bit 4</li> <li>TOSE: TMR0 Source Edge Select bit         <ol> <li>Increment on high-to-low transition on RA4/T0</li> <li>Increment on low-to-high transition on RA4/T0</li> </ol> </li> <li>bit 3</li> </ul>	)CKI pin )CKI pin	alues		
bit 6       INTEDG: Interrupt Edge Select bit         1 = Interrupt on rising edge of RB0/INT pin         0 = Interrupt on falling edge of RB0/INT pin         bit 5       TOCS: TMR0 Clock Source Select bit         1 = Transition on RA4/T0CKI pin         0 = Internal instruction cycle clock (CLKOUT)         bit 4       TOSE: TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3       PSA: Prescaler Assignment bit	DCKI pin DCKI pin			
1 = Interrupt on rising edge of RB0/INT pin         0 = Interrupt on falling edge of RB0/INT pin         bit 5 <b>T0CS</b> : TMR0 Clock Source Select bit         1 = Transition on RA4/T0CKI pin         0 = Internal instruction cycle clock (CLKOUT)         bit 4 <b>T0SE</b> : TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3 <b>PSA</b> : Prescaler Assignment bit	)CKI pin )CKI pin			
<ul> <li>bit 5</li> <li><b>TOCS</b>: TMR0 Clock Source Select bit         <ol> <li>Transition on RA4/T0CKI pin</li> <li>Transition on RA4/T0CKI pin</li> <li>Internal instruction cycle clock (CLKOUT)</li> </ol> </li> <li>bit 4</li> <li><b>TOSE</b>: TMR0 Source Edge Select bit         <ol> <li>Increment on high-to-low transition on RA4/T0</li> <li>Increment on low-to-high transition on RA4/T0</li> </ol> </li> <li>bit 3</li> </ul>	)CKI pin )CKI pin			
bit 5 <b>TOCS</b> : TMR0 Clock Source Select bit         1 = Transition on RA4/T0CKI pin         0 = Internal instruction cycle clock (CLKOUT)         bit 4 <b>TOSE</b> : TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3 <b>PSA</b> : Prescaler Assignment bit	)CKI pin )CKI pin			
1 = Transition on RA4/T0CKI pin         0 = Internal instruction cycle clock (CLKOUT)         bit 4 <b>T0SE</b> : TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3 <b>PSA</b> : Prescaler Assignment bit	)CKI pin )CKI pin			
<ul> <li>0 = Internal instruction cycle clock (CLKOUT)</li> <li>bit 4 T0SE: TMR0 Source Edge Select bit         <ol> <li>1 = Increment on high-to-low transition on RA4/T0</li> <li>0 = Increment on low-to-high transition on RA4/T0</li> </ol> </li> <li>bit 3 PSA: Prescaler Assignment bit</li> </ul>	)CKI pin )CKI pin			
bit 4       TOSE: TMR0 Source Edge Select bit         1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3       PSA: Prescaler Assignment bit	)CKI pin )CKI pin			
1 = Increment on high-to-low transition on RA4/T0         0 = Increment on low-to-high transition on RA4/T0         bit 3 <b>PSA</b> : Prescaler Assignment bit	CKI pin CKI pin			
0 = Increment on low-to-high transition on RA4/T0         bit 3 <b>PSA</b> : Prescaler Assignment bit	OCKI pin			
bit 3 <b>PSA</b> : Prescaler Assignment bit				
1 = Prescaler is assigned to the WDT				
0 = Prescaler is assigned to the Timer0 module				
bit 2-0 <b>PS&lt;2:0&gt;</b> : Prescaler Rate Select bits				
Bit Value TMR0 Rate WDT Rate				
000 1:2 1:1				
001 1:4 1:2				
101 1:64 1:32				
110 1:128 1:64				
111 1:256 1:128				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### 6.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

#### 6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

#### 6.2.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the TMR0 is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.





#### 7.1 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON register is used to select the mode. Figure 7-1 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the Comparator

mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Table 12-2.

**Note:** Comparator interrupts should be disabled during a Comparator mode change otherwise a false interrupt may occur.





# PIC16C62X

#### **FIGURE 9-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR** SLOW VDD POWER-UP) Vdd Vdd D R R1 MCLR PIC16C62X С Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down. **2:** < 40 k $\Omega$ is recommended to make sure that voltage drop across R does not violate the device's electrical specification. **3:** R1 = $100\Omega$ to 1 k $\Omega$ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin

breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

#### FIGURE 9-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate RESET when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
  - **2:** Internal Brown-out Reset circuitry should be disabled when using this circuit.

#### FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



**3:** Resistors should be adjusted for the characteristics of the transistor.

#### FIGURE 9-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both high and low active RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

#### 9.5.1 RB0/INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered, either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the interrupt service routine before reenabling this interrupt. The RB0/INT interrupt can wake-up the processor from SLEEP, if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.8 for details on SLEEP and Figure 9-18 for timing of wakeup from SLEEP through RB0/INT interrupt.

#### 9.5.2 TMR0 INTERRUPT

An overflow (FFh  $\rightarrow$  00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 6.0.

#### 9.5.3 PORTB INTERRUPT

An input change on PORTB <7:4> sets the RBIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RBIE (INTCON<4>) bit. For operation of PORTB (Section 5.2).

Note:	If a change on the I/O pin should occur					
	when the read operation is being executed					
	(start of the Q2 cycle), then the RBIF					
	interrupt flag may not get set.					

#### 9.5.4 COMPARATOR INTERRUPT

See Section 7.6 for complete description of comparator interrupts.



#### FIGURE 9-16: INT PIN INTERRUPT TIMING

BTFSS	Bit Test f, Skip if Set	CALL	Call Subroutine	
Syntax:	[ <i>label</i> ]BTFSS f,b	Syntax:	[ <i>label</i> ] CALL k	
Operands:	$0 \leq f \leq 127$	Operands:	$0 \leq k \leq 2047$	
Operation:	0 ≤ b < 7 skip if (f <b>) = 1</b>	Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>	
Encoding:		Status Affected:	None	
Encouring.	If hit 'h' in register 'f' is '1', then the	Encoding:	10 Okkk kkkk kkkk	
Description.	next instruction is skipped. If bit 'b' is '1', then the next instruc- tion fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.	Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immedi- ate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is	
Words:	1		a two-cycle instruction.	
Cycles:	1(2)	vvords:	1	
Example	HERE BTFSS FLAG,1	Cycles:	2	
	TRUE · DE	Example	HERE CALL THER E	
	Before Instruction PC = address HERE After Instruction if FLAG<1> = 0, PC = address FALSE if FLAG<1> = 1, PC = address TRUE		PC = Address HERE After Instruction PC = Address THERE TOS = Address HERE+1	
		CLRF	Clear f	
		Syntax:	[ <i>label</i> ] CLRF f	
		Operands:	$0 \le f \le 127$	
		Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$	
		Status Affected:	Z	
		Encoding:	00 0001 1fff ffff	
		Description:	The contents of register 'f' are cleared and the Z bit is set.	
		Words:	1	
		Cycles:	1	
		Example	CLRF FLAG_REG	
			Before Instruction FLAG_REG = 0x5A After Instruction FLAG_REG = 0x00 Z = 1	

MOVF	Move f					
Syntax:	[ <i>label</i> ] MOVF f,d					
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$					
Operation:	$(f) \rightarrow (dest)$					
Status Affected:	Z					
Encoding:	00 1000 dfff ffff					
Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$ , destination is W register. If $d = 1$ , the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.					
Words:	1					
Cycles:	1					
Example	MOVF FSR, <b>0</b>					
	W = value in FSR register Z = 1					
MOVWF	Move W to f					
Syntax:	[ <i>label</i> ] MOVWF f					
Operands:	$0 \leq f \leq 127$					
Operation:	$(W) \rightarrow (f)$					
Status Affected:	None					
Encoding:	00 0000 1fff ffff					
Description:	Move data from W register to reg- ister 'f'.					
Words:	1					
Cycles:	1					
Example	MOVWF OPTION					
	Before Instruction OPTION = 0xFF W = 0x4F					
	Atter Instruction OPTION = 0x4F W = 0x4F					

NOP	No Operation			
Syntax:	[ label ]	NOP		
Operands:	None			
Operation:	No operation			
Status Affected:	None			
Encoding:	00	0000	0xx0	0000
Description:	No operation.			
Words:	1			
Cycles:	1			
Example	NOP			

OPTION	Load Option Register			
Syntax:	[label]	OPTION	1	
Operands:	None			
Operation:	$(W) \rightarrow OPTION$			
Status Affected:	None			
Encoding:	00	0000	0110	0010
Description: Words:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a read- able/writable register, the user can directly address it. 1			
Cycles:	1			
Example				
	To maintain upward compatibil- ity with future PICmicro <sup>®</sup> products, do not use this instruction.			

RLF	Rotate	Left f th	roug	h Car	ry			
Syntax:	[ label ]	RLF	f,d			I		
Operands:	0 ≤ f ≤ 1 d ∈ [0,1	27 ]						
Operation:	See des	scription	belo	w				
Status Affected:	С							
Encoding:	00	1101	d	fff	ffff	]		
Description:	rotated the Carr is place 1, the re register	one bit to ry Flag. I d in the V esult is si 'f'.	regis o the f 'd' is N reg corec Regi	left th s 0, the gister. I back	are irough e result If 'd' is in			
Words:	1							
Cycles:	1							
Example	RLF	REG1,	0					
	Before	Before Instruction						
		REG1	=	111	0 0110			
	After In	C	=	0				
		REG1	=	111	0 0110			
		W	=	110	0 1100			
		C	=	1				

RRF	Rotate R	ight f th	roug	gh Ca	irry				
Syntax:	[label] RRF f,d								
Operands:	$0 \le f \le 127$ $d \in [0,1]$								
Operation:	See description below								
Status Affected:	С								
Encoding:	00	1100	df	ff	ffff				
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.								
			Regis	ter f	┠╸				
Words:	1								
Cycles:	1								
Example	RRF REG1, 0								
	Before In	structior	ı						
		REG1	=	1110	0110				
	After Inst	ruction	=	U					
		REG1	=	1110	0110				
		W	=	0111	0011				
		C	=	0					

SLEEP

Syntax:	[ lahal	SI FFF	)					
Gyntax.	]	OLLLI						
Operands:	None							
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \text{ prescaler}, \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow PD \end{array}$							
Status Affected:	TO, PD							
Encoding:	00	0000	0110	0011				
Description:	The power-down STATUS bit, PD is cleared. Time-out STATUS bit, TO is set. Watch- dog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 9.8 for more details							
Words:	1							
Cycles:	1							
Example:	SLEEP							

SWAPF	Swap Nibbles in f						
Syntax:	[label]	SWAPF	f,d				
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$						
Operation:	(f<3:0>) → (dest<7:4>), (f<7:4>) → (dest<3:0>)						
Status Affected:	None						
Encoding:	00	1110	dfff	Ē	ffff		
Description:	register 'f' are exchanged. If 'd' is 0, the result is placed in W register. If 'd' is 1, the result is placed in register 'f'.						
Words:	1						
Cycles:	1						
Example	SWAPF	REG,	0				
	Before In	struction					
		REG1	=	0xA5			
	After Inst	ruction					
		REG1 W	= =	0xA5 0x5A			

TRIS	Load TRIS Register					
Syntax:	[ <i>label</i> ] TRIS f					
Operands:	$5 \le f \le 7$					
Operation:	(W) $\rightarrow$ TRIS register f;					
Status Affected:	None					
Encoding:	00 0000 0110 Offf					
Description.	code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.					
Words:	1					
Cycles:	1					
Example						
	To maintain upward compatibil- ity with future PICmicro <sup>®</sup> prod- ucts, do not use this instruction.					

XORLW	Exclusive OR Literal with W						
Syntax:	[ <i>label</i> XORLW k ]						
Operands:	$0 \leq k \leq 255$						
Operation:	(W) .XOR. $k \rightarrow (W)$						
Status Affected:	Z						
Encoding:	11 1010 kkkk kkkk						
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.						
Words:	1						
Cycles:	1						
Example:	XORLW 0xAF						
	Before Instruction						
	W = 0xB5						
	After Instruction						
	W = 0x1A						
XORWF	Exclusive OR W with f						
Syntax:	[ <i>label</i> ] XORWF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$						
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)						
Status Affected:	Z						
Encoding:	00 0110 dfff ffff						
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Example	XORWF REG 1						
	Before Instruction						
	REG = 0xAF W = 0xB5						
	After Instruction						
	REG = 0x1A W = 0xB5						

#### 11.14 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer, or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include analog input, push button switches and eight LEDs.

#### 11.15 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/ Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface, and a 16 x 2 LCD display. Also included is the book and CD-ROM *"TCP/IP Lean, Web Servers for Embedded Systems,"* by Jeremy Bentham

#### 11.16 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18-, 28-, and 40-pin microcontrollers, including PIC16F87X and PIC18FXX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs, and sample PIC18F452 and PIC16F877 FLASH microcontrollers.

#### 11.17 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

#### 11.18 PICDEM 4 8/14/18-Pin Demonstration Board

The PICDEM 4 can be used to demonstrate the capabilities of the 8-, 14-, and 18-pin PIC16XXXX and PIC18XXXX MCUs, including the PIC16F818/819, PIC16F87/88, PIC16F62XA and the PIC18F1320 family of microcontrollers. PICDEM 4 is intended to showcase the many features of these low pin count parts, including LIN and Motor Control using ECCP. Special provisions are made for low power operation with the supercapacitor circuit, and jumpers allow onboard hardware to be disabled to eliminate current draw in this mode. Included on the demo board are provisions for Crystal, RC or Canned Oscillator modes, a five volt regulator for use with a nine volt wall adapter or battery, DB-9 RS-232 interface, ICD connector for programming via ICSP and development with MPLAB ICD 2, 2x16 liquid crystal display, PCB footprints for H-Bridge motor driver, LIN transceiver and EEPROM. Also included are: header for expansion, eight LEDs, four potentiometers, three push buttons and a prototyping area. Included with the kit is a PIC16F627A and a PIC18F1320. Tutorial firmware is included along with the User's Guide.

#### 11.19 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board FLASH memory. A generous prototype area is available for user hardware expansion.

#### 11.20 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/De-multiplexed and 16-bit Memory modes. The board includes 2 Mb external FLASH memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

#### 11.21 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PICmicro microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 FLASH microcontroller serves as the master. All three micro-controllers are programmed with firmware to provide LIN bus communication.

#### 11.22 PICkit<sup>™</sup> 1 FLASH Starter Kit

A complete "development system in a box", the PICkit FLASH Starter Kit includes a convenient multi-section board for programming, evaluation, and development of 8/14-pin FLASH PIC<sup>®</sup> microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the user's guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB<sup>®</sup> IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin FLASH PIC<sup>®</sup> Microcontrollers" Handbook and a USB Interface Cable. Supports all current 8/14-pin FLASH PIC microcontrollers, as well as many future planned devices.

#### 11.23 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

#### 11.24 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip's HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/ calibration kits
- IrDA<sup>®</sup> development kit
- microID development and rfLab<sup>™</sup> development software
- SEEVAL<sup>®</sup> designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high power IR driver, delta sigma ADC, and flow rate sensor

Check the Microchip web page and the latest Product Line Card for the complete list of demonstration and evaluation kits. NOTES:



FIGURE 12-8: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH, -40°C  $\leq$  TA  $\leq$  0°C, +70°C  $\leq$  TA  $\leq$  +125°C



#### 12.1 DC Characteristics: PIC16C62X-04 (Commercial, Industrial, Extended) PIC16C62X-20 (Commercial, Industrial, Extended) PIC16LC62X-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62X			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}$ C $\leq TA \leq +85^{\circ}$ C for industrial and $0^{\circ}$ C $\leq TA \leq +70^{\circ}$ C for commercial and $-40^{\circ}$ C $\leq TA \leq +125^{\circ}$ C for extendedStandard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}$ C $\leq TA \leq +85^{\circ}$ C for industrial and $0^{\circ}$ C $\leq TA \leq +85^{\circ}$ C for industrial and $0^{\circ}$ C $\leq TA \leq +70^{\circ}$ C for commercial and					
				ating vo	oltage V	-4 VDD ran	$0^{\circ}C \le TA \le +125^{\circ}C$ for extended ge is the PIC16C62X range.	
Param . No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions	
D022 D022A D023 D023A D022A D022A D022A D023A	ΔIWDT ΔIBOR ΔICOM P ΔIVREF ΔIWDT ΔIBOR ΔICOM P	WDT Current <sup>(5)</sup> Brown-out Reset Current <sup>(5)</sup> Comparator Current for each Comparator <sup>(5)</sup> VREF Current <sup>(5)</sup> WDT Current <sup>(5)</sup> Brown-out Reset Current <sup>(5)</sup> Comparator Current for each Comparator <sup>(5)</sup> VREF Current <sup>(5)</sup>		6.0 350 — 6.0 350 — —	20 25 425 100 300 15 425 100 300	μΑ μΑ μΑ μΑ μΑ μΑ μΑ μΑ	$V_{DD}=4.0V$ $(125^{\circ}C)$ $BOD \text{ enabled, } V_{DD} = 5.0V$ $V_{DD} = 4.0V$ $V_{DD} = 4.0V$ $V_{DD}=3.0V$ $BOD \text{ enabled, } V_{DD} = 5.0V$ $V_{DD} = 3.0V$ $V_{DD} = 3.0V$	
1A 1A	Fosc	LP Oscillator Operating Frequency RC Oscillator Operating Frequency XT Oscillator Operating Frequency HS Oscillator Operating Frequency LP Oscillator Operating Frequency RC Oscillator Operating Frequency	0 0 0 0		200 4 4 20 200 4	kHz MHz MHz MHz kHz MHz	All temperatures All temperatures All temperatures All temperatures All temperatures All temperatures	
		HS Oscillator Operating Frequency	0	_	4 20	MHz	All temperatures	

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The  $\Delta$  current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

#### 12.8 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. TppS

F F F			
т			
F	Frequency	Т	Time
Lowerca	ase subscripts (pp) and their meanings:		
рр			
ck	CLKOUT	osc	OSC1
io	I/O port	tO	ТОСКІ
mc	MCLR		
Upperca	ase letters and their meanings:		
S			
F	Fall	Р	Period
н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-Impedance

#### FIGURE 12-11: LOAD CONDITIONS







### 13.0 DEVICE CHARACTERIZATION INFORMATION

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution, while "max" or "min" represents (mean +  $3\sigma$ ) and (mean -  $3\sigma$ ) respectively, where  $\sigma$  is standard deviation.



FIGURE 13-1: IDD VS. FREQUENCY (XT MODE, VDD = 5.5V)

FIGURE 13-2: PIC16C622A IPD VS. VDD (WDT DISABLE)



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# PIC16C62X









18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



	Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		18			18		
Pitch	р		.100			2.54		
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32	
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	Е	.300	.313	.325	7.62	7.94	8.26	
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60	
Overall Length	D	.890	.898	.905	22.61	22.80	22.99	
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78	
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56	
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-007