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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c621a-04e-so

Email: info@E-XFL.COM

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# **PIC16C62X**

## **EPROM-Based 8-Bit CMOS Microcontrollers**

#### Devices included in this data sheet:

Referred to collectively as PIC16C62X.

- PIC16C620 PIC16C620A
- PIC16C621 PIC16C621A
- PIC16C622 PIC16C622A
- PIC16CR620A

#### **High Performance RISC CPU:**

- Only 35 instructions to learn
- All single cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
  - DC 40 MHz clock input
  - DC 100 ns instruction cycle

Device	Program Memory	Data Memory
PIC16C620	512	80
PIC16C620A	512	96
PIC16CR620A	512	96
PIC16C621	1K	80
PIC16C621A	1K	96
PIC16C622	2K	128
PIC16C622A	2K	128

· Interrupt capability

- 16 special function hardware registers
- 8-level deep hardware stack
- Direct, Indirect and Relative addressing modes

#### **Peripheral Features:**

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
- Two analog comparators
- Programmable on-chip voltage reference (VREF) module
- Programmable input multiplexing from device inputs and internal voltage reference
- Comparator outputs can be output signals
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

#### Pin Diagrams

#### PDIP, SOIC, Windowed CERDIP



#### **Special Microcontroller Features:**

- · Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- · Programmable code protection
- · Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Four user programmable ID locations

#### **CMOS Technology:**

- Low power, high speed CMOS EPROM technology
- Fully static design
- · Wide operating range
  - 2.5V to 5.5V
- Commercial, industrial and extended temperature range
- Low power consumption
  - < 2.0 mA @ 5.0V, 4.0 MHz
  - 15 μA typical @ 3.0V, 32 kHz
  - < 1.0 μA typical standby current @ 3.0V

NOTES:

## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C62X uses a Harvard architecture, in which, program and data are accessed from separate memories using separate busses. This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C620(A) and PIC16CR620A address 512 x 14 on-chip program memory. The PIC16C621(A) addresses  $1K \times 14$  program memory. The PIC16C622(A) addresses  $2K \times 14$  program memory. All program memory is internal.

The PIC16C62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C62X has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any Addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

#### 6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to WDT.)

#### EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

	-	
1.BCF	STATUS, RPO	;Skip if already in ;Bank 0
2.CLRWDT		;Clear WDT
3.CLRF	TMR0	;Clear TMR0 & Prescaler
4.BSF	STATUS, RPO	;Bank 1
5.MOVLW	'00101111'b;	;These 3 lines (5, 6, 7)
6.MOVWF	OPTION	;are required only if ;desired PS<2:0> are
7.CLRWDT		;000 or 001
8.MOVLW	'00101xxx'b	;Set Postscaler to
9.MOVWF	OPTION	;desired WDT rate
10.BCF	STATUS, RPO	;Return to Bank 0

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 6-2. This precaution must be taken even if the WDT is disabled.

#### EXAMPLE 6-2:

#### CHANGING PRESCALER (WDT→TIMER0)

	•	
CLRWDT		;Clear WDT and
		;prescaler
BSF	STATUS, RPO	
MOVLW	b'xxxx0xxx'	;Select TMR0, new
		prescale value and
		, plock gourgo
		,CIOCK SOULCE
MOVWF	OPTION REG	
BCF	STATUS, RPO	

#### TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
01h	TMR0	Timer0	module regi	ister						XXXX XXXX	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	_	_		TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown

**Note:** Shaded bits are not used by TMR0 module.

### 7.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with the RA0 through RA3 pins. The On-Chip Voltage Reference (Section 8.0) can also be an input to the comparators.

The CMCON register, shown in Register 7-1, controls the comparator input and output multiplexers. A block diagram of the comparator is shown in Figure 7-1.

#### REGISTER 7-1: CMCON REGISTER (ADDRESS 1Fh)

	R-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0		
	C2OUT	C10UT	—	—	CIS	CM2	CM1	CM0		
	bit 7							bit 0		
bit 7	<b>C2OUT</b> : Comparator 2 output 1 = C2 VIN+ > C2 VIN- 0 = C2 VIN+ < C2 VIN-									
bit 6	<b>C1OUT</b> : Comparator 1 output 1 = C1 VIN+ > C1 VIN- 0 = C1 VIN+ < C1 VIN-									
bit 5-4	Unimplem	ented: Read	d as '0'							
bit 3	CIS: Comparator Input Switch When CM<2:0>: = 001: 1 = C1 VIN- connects to RA3 0 = C1 VIN- connects to RA0 When CM<2:0> = 010: 1 = C1 VIN- connects to RA3 C2 VIN- connects to RA2 0 = C1 VIN- connects to RA2 0 = C1 VIN- connects to RA2									
bit 2-0	CM<2:0>: (	Comparator	mode.							
	Logondi									

L	.egend:			
F	R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-	n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The code example in Example 7-1 depicts the steps required to configure the comparator module. RA3 and RA4 are configured as digital output. RA0 and RA1 are configured as the V- inputs and RA2 as the V+ input to both comparators.

#### EXAMPLE 7-1: INITIALIZING COMPARATOR MODULE

MOVLW	0x03	;Init comparator mode
MOVWF	CMCON	;CM<2:0> = 011
CLRF	PORTA	;Init PORTA
BSF	STATUS, RPO	;Select Bank1
MOVLW	0x07	;Initialize data direction
MOVWF	TRISA	;Set RA<2:0> as inputs
		;RA<4:3> as outputs
		;TRISA<7:5> always read `0'
BCF	STATUS, RPO	;Select Bank 0
CALL	DELAY 10	;10µs delay
MOVF	CMCON,F	;Read CMCONtoend change condition
BCF	PIR1,CMIF	;Clear pending interrupts
BSF	STATUS, RPO	;Select Bank 1
BSF	PIE1,CMIE	;Enable comparator interrupts
BCF	STATUS, RPO	;Select Bank 0
BSF	INTCON, PEIE	;Enable peripheral interrupts
BSF	INTCON, GIE	;Global interrupt enable

### 7.2 Comparator Operation

A single comparator is shown in Figure 7-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 7-2 represent the uncertainty due to input offsets and response time.

#### 7.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator Operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (Figure 7-2).





#### 7.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSs and VDD, and can be applied to either pin of the comparator(s).

#### 7.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 10, Instruction Sets, contains a detailed description of the Voltage Reference Module that provides this signal. The internal reference signal is used when the comparators are in mode CM<2:0>=010 (Figure 7-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

#### 8.0 **VOLTAGE REFERENCE** MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Register 8-1. The block diagram is given in Figure 8-1.

#### 8.1 **Configuring the Voltage Reference**

The Voltage Reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 0: VREF = (VDD x 1/4) + (VR<3:0>/32) x VDD

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 12-1). Example 8-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	VREN	VROE	Vrr	_	VR3	VR2	VR1	Vr0
	bit 7							bit 0
bit 7	VREN: VREI 1 = VREF C	F Enable ircuit power	ed on					
	0 = VREF C	ircuit powere	ed down, no	IDD drain				
bit 6	VROE: VRE	F Output En	able					
	1 = VREF IS 0 = VREF IS	s output on F s disconnect	cA2 pin ed from RA2	2 pin				
bit 5	VRR: VREF	Range sele	ction	•				
	1 = Low Ra	ange						
hit 1		ange	d aa '0'					
DIC 4	Unimplem	ented: Rea	das U					
bit 3-0	VR<3:0>: \	/REF value s	election $0 \leq$	VR [3:0] ≤ 1	5			
	when VRR	= 1: VREF =	(VR<3:0>/ 2	4) * VDD	0) + ) /			
	when VRR	= 0: VREF =	1/4 ^ VDD +	(VR<3:0>/ 3	2) ^ VDD			
	Legend:							
	R = Reada	ıble bit	W = W	/ritable bit	U = Unin	nplemented	bit, read as	'0'
	- n = Value	at POR	'1' = B	it is set	'0' = Bit i	s cleared	x = Bit is u	Inknown
8-1:	VOLTAGE			K DIAGR	۸M			
			16 \$	Stages				
$\sim$	T			∕		_		
$\rightarrow$	-여드 <sub>8R</sub>	R	R	R	R			
			ΔΔΔ .	۸ ۸ ۸	A A A			

#### **REGISTER 8-1:** VRCON REGISTER(ADDRESS 9Fh)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented I	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### **FIGURE 8-**



#### EXAMPLE 8-1: VOLTAGE REFERENCE CONFIGURATION

MOVLW	0x02	; 4 Inputs Muxed
MOVWF	CMCON	; to 2 comps.
BSF	STATUS, RPO	; go to Bank 1
MOVLW	0x0F	; RA3-RA0 are
MOVWF	TRISA	; inputs
MOVLW	0xA6	; enable VREF
MOVWF	VRCON	; low range
		; set VR<3:0>=6
BCF	STATUS, RPO	; go to Bank O
CALL	DELAY10	; 10µs delay

#### 8.2 Voltage Reference Accuracy/Error

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 8-1) keep VREF from approaching VSS or VDD. The voltage reference is VDD derived and therefore, the VREF output changes with fluctuations in VDD. The tested absolute accuracy of the voltage reference can be found in Table 12-2.

#### 8.3 Operation During SLEEP

When the device wakes up from SLEEP through an interrupt or a Watchdog Timer time-out, the contents of the VRCON register are not affected. To minimize current consumption in SLEEP mode, the voltage reference should be disabled.

#### 8.4 Effects of a RESET

A device RESET disables the voltage reference by clearing bit VREN (VRCON<7>). This reset also disconnects the reference from the RA2 pin by clearing bit VROE (VRCON<6>) and selects the high voltage range by clearing bit VRR (VRCON<5>). The VREF value select bits, VRCON<3:0>, are also cleared.

#### 8.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RA2 pin if the TRISA<2> bit is set and the VROE bit, VRCON<6>, is set. Enabling the voltage reference output onto the RA2 pin with an input signal present will increase current consumption. Connecting RA2 as a digital output with VREF enabled will also increase current consumption.

The RA2 pin can be used as a simple D/A output with limited drive capability. Due to the limited drive capability, a buffer must be used in conjunction with the voltage reference output for external connections to VREF. Figure 8-2 shows an example buffering technique.

# FIGURE 8-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE

#### TABLE 8-1: REGISTERS ASSOCIATED WITH VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR	Value On All Other RESETS
9Fh	VRCON	VREN	VROE	VRR		VR3	VR2	VR1	VR0	000- 0000	000- 0000
1Fh	CMCON	C2OUT	C10UT	_	-	CIS	CM2	CM1	CM0	00 0000	00 0000
85h	TRISA	_	_	_	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111

**Note:** - = Unimplemented, read as "0"

## 9.0 SPECIAL FEATURES OF THE CPU

Special circuits to deal with the needs of real-time applications are what sets a microcontroller apart from other processors. The PIC16C62X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection.

These are:

- 1. OSC selection
- 2. RESET Power-on Reset (POR) Power-up Timer (PWRT) Oscillator Start-up Timer (OST) Brown-out Reset (BOR)
- 3. Interrupts
- 4. Watchdog Timer (WDT)
- 5. SLEEP
- 6. Code protection
- 7. ID Locations
- 8. In-Circuit Serial Programming™

The PIC16C62X devices have a Watchdog Timer which is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to RESET the device if a brown-out occurs, which provides at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer wake-up or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

#### 9.2 Oscillator Configurations

#### 9.2.1 OSCILLATOR TYPES

The PIC16C62X devices can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

## 9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 9-1). The PIC16C62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 9-2).

#### FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 9-1 and Table 9-2 for recommended values of C1 and C2.

**Note:** A series resistor may be required for AT strip cut crystals.

#### FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC



## TABLE 9-1:CAPACITOR SELECTION FOR<br/>CERAMIC RESONATORS

R	~[]						
Mode	Freq	<b>OSC2(C2)</b>					
ХТ	455 kHz 2.0 MHz 4.0 MHz	22 - 100 pF 15 - 68 pF 15 - 68 pF	82 - 100 pF 15 - 68 pF 15 - 68 pF				
HS	8.0 MHz 16.0 MHz 🔨	10-68 bF 10-22 pF	10 - 68 pF 10 - 22 pF				
Higher capacitance increases the stability of the oscil- lator but also increases the start-up time. These webes are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components							

#### TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	Freq OSC1(C1)					
LP	32 kHz	68 - 100 pF	68 - 100 pF				
	200 kHz	15 - 30 pF	15 - 30 pF				
хт	100 kHz	68 - 150 pF	150 - 300 pF				
	2 MHz	15 - 30 pF	15 - 30 pF				
	4 MHz	15 - 30 pF	15 - 30 pF				
HS	8 MHz	15-30 pF	<sup>V</sup> 15 - 30 pF				
	10 MHz	15-30 pF	15 - 30 pF				
	20 MHz 🔨	15-30 pF	15 - 30 pF				
Higher capacitance, increases the stability of the oscillator build also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.							

#### 9.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance or one with parallel resonance.

Figure 9-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 k $\Omega$  resistor provides the negative feedback for stability. The 10 k $\Omega$  potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

#### FIGURE 9-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 9-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a  $180^{\circ}$  phase shift in a series resonant oscillator circuit. The 330 k $\Omega$  resistors provide the negative feedback to bias the inverters in their linear region.

#### FIGURE 9-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



#### 9.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 9-5 shows how the R/C combination is connected to the PIC16C62X. For REXT values below 2.2 k $\Omega$ , the oscillator operation may become unstable or stop completely. For very high REXT values (e.g., 1 M $\Omega$ ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep REXT between 3 k $\Omega$  and 100 k $\Omega$ .

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 13.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 13.0 for variation of oscillator frequency due to VDD for given REXT/CEXT values, as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

#### FIGURE 9-5: RC OSCILLATOR MODE



# PIC16C62X

#### **FIGURE 9-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR** SLOW VDD POWER-UP) Vdd VDD D R R1 MCLR PIC16C62X С Note 1: External Power-on Reset circuit is required only if VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down. **2:** < 40 k $\Omega$ is recommended to make sure that voltage drop across R does not violate the device's electrical specification. **3:** R1 = $100\Omega$ to 1 k $\Omega$ will limit any current flowing into MCLR from external capacitor C in the event of MCLR/VPP pin

breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

#### FIGURE 9-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



- Note 1: This circuit will activate RESET when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.
  - **2:** Internal Brown-out Reset circuitry should be disabled when using this circuit.

#### FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



**3:** Resistors should be adjusted for the characteristics of the transistor.

#### FIGURE 9-14: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both high and low active RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

#### 9.8 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the PD bit in the STATUS register is cleared, the TO bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSs with no external circuitry drawing current from the I/O pin and the comparators and VREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSs for lowest current consumption. The contribution from on chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC).

Note:	It should be noted that a RESET generated
	by a WDT time-out does not drive MCLR
	pin low.

#### 9.8.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- 1. External RESET input on MCLR pin
- 2. Watchdog Timer Wake-up (if WDT was enabled)
- 3. Interrupt from RB0/INT pin, RB Port change, or the Peripheral Interrupt (Comparator).

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. PD bit, which is set on power-up, is cleared when SLEEP is invoked. TO bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction after the SLEEP instruction after the instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

**Note:** If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4	4 Q1	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
CLKOUT(4)	Tost(2	)/	\/	\/'\	'
INT pin		1	ı ı ı ı	1	I
INTE flag	\		I I		
(INTCON<1>)	·····/	Interrupt Latend	şy		
	<u>i</u>	(Note 2)	i		
(INTCON<7>)	Processor in	1		<u> </u>	<u> </u>
	SLEEP	1	I I	i	i i
INSTRUCTION FLOW		1	і і і і	1	1
PC X PC+1	X PC+2	X PC+2	X PC + 2	<u>x 0004h x</u>	0005h
$\begin{array}{c} \mbox{Instruction} \\ \mbox{fetched} \end{array} \Big\{ \begin{array}{c} \mbox{Inst}(\mbox{PC}) = \mbox{SLEEP} & \mbox{Inst}(\mbox{PC} + 1) \end{array} \right.$		Inst(PC + 2)	       	Inst(0004h)	Inst(0005h)
Instruction { Inst(PC - 1) SLEEP		Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)
Note 1: XT, HS or LP Oscillator mode 2: Tos⊤ = 1024Tosc (drawing n	e assumed. ot to scale) This	delay will not be	e there for RC	Osc mode.	

#### FIGURE 9-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT

**3:** GIE = '1' assumed. In this case, after wake-up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these Osc modes, but shown here for timing reference.

#### 9.9 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip	does	not	recommend	code
	protecting	windov	ved d	evices.	

#### 9.10 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify. Only the Least Significant 4 bits of the ID locations are used.

#### 9.11 In-Circuit Serial Programming™

The PIC16C62X microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RB6 and RB7 pins low, while raising the MCLR (VPP) pin from VIL to VIHH (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After RESET, to place the device into Programming/ Verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16C6X/7X/9XX Programming Specification (DS30228).

A typical In-Circuit Serial Programming connection is shown in Figure 9-19.

# FIGURE 9-19:

#### TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



## **10.1** Instruction Descriptions

ADDLW	Add Literal and W								
Syntax:	[ <i>label</i> ] ADDLW k								
Operands:	$0 \le k \le 255$								
Operation:	$(W) + k \to (W)$								
Status Affected:	C, DC, Z								
Encoding:	11 111x kkkk kkkk								
Description:	added to the eight bit literal 'k' and the result is placed in the W register.								
Cycles:	1								
Example	ADDLW 0x15								
	Before Instruction W = 0x10 After Instruction W = 0x25								

ANDLW	AND Literal with W								
Syntax:	[ <i>label</i> ] ANDLW k								
Operands:	$0 \le k \le 255$								
Operation:	(W) .AND. (k) $\rightarrow$ (W)								
Status Affected:	Z								
Encoding:	11 1001 kkkk kkkk								
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ANDLW 0x5F								
	Before Instruction W = 0xA3 After Instruction W = 0x03								
ANDWF	AND W with f								

Add W and f								
[ <i>label</i> ] ADDWF f,d								
$0 \le f \le 127$ $d \in [0,1]$								
(W) + (f) $\rightarrow$ (dest)								
C, DC, Z								
00 0111 dfff ffff								
Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
1								
1								
ADDWF FSR, <b>O</b>								
Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0xD9 FSR = 0xC2								

ANDWF	AND W with f								
Syntax:	[ <i>label</i> ] ANDWF f,d								
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$								
Operation:	(W) .AND. (f) $\rightarrow$ (dest)								
Status Affected:	Z								
Encoding:	00 0101 dfff ffff								
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example	ANDWF FSR, 1								
	Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0x17 FSR = 0x02								

## 11.0 DEVELOPMENT SUPPORT

The PICmicro<sup>®</sup> microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM<sup>™</sup> Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK<sup>™</sup> Object Linker/ MPLIB<sup>™</sup> Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- MPLAB dsPIC30 Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD 2
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART<sup>®</sup> Plus Development Programmer
- Low Cost Demonstration Boards
  - PICDEM<sup>™</sup> 1 Demonstration Board
  - PICDEM.net<sup>™</sup> Demonstration Board
  - PICDEM 2 Plus Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 4 Demonstration Board
  - PICDEM 17 Demonstration Board
  - PICDEM 18R Demonstration Board
  - PICDEM LIN Demonstration Board
  - PICDEM USB Demonstration Board
- Evaluation Kits
  - KEELOQ®
  - PICDEM MSC
  - microID®
  - CAN
  - PowerSmart®
  - Analog

#### 11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows<sup>®</sup> based application that contains:

- · An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- · A full-featured editor with color coded context
- · A multiple project manager
- Customizable data windows with direct edit of contents
- · High level source code debugging
- Mouse over variable inspection
- Extensive on-line help
- The MPLAB IDE allows you to:
- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files (assembly or C)
  - absolute listing file (mixed assembly and C)
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

#### 11.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel<sup>®</sup> standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- · User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

#### 12.3 DC CHARACTERISTICS: PIC16CR62XA-04 (Commercial, Industrial, Extended) PIC16CR62XA-20 (Commercial, Industrial, Extended) PIC16LCR62XA-04 (Commercial, Industrial, Extended)

PIC16CR62XA-04 PIC16CR62XA-20				Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}$ C $\leq$ TA $\leq$ +85°C for industrial and $0^{\circ}$ C $\leq$ TA $\leq$ +70°C for commercial and $-40^{\circ}$ C $\leq$ TA $\leq$ +125°C for extended							
PIC16LCR62XA-04				Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}$ C $\leq$ TA $\leq$ +85°C for industrial and0°C $\leq$ TA $\leq$ +70°C for commercial and $-40^{\circ}$ C $\leq$ TA $\leq$ +125°C for extended							
Param. No.	Sym	Characteristic	Min	Тур†	Мах	Units	Conditions				
D001	Vdd	Supply Voltage	3.0	_	5.5	V	See Figures 12-7, 12-8, 12-9				
D001	Vdd	Supply Voltage	2.5	—	5.5	V	See Figures 12-7, 12-8, 12-9				
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	-	1.5*	—	V	Device in SLEEP mode				
D002	Vdr	RAM Data Retention Voltage <sup>(1)</sup>	-	1.5*	_	V	Device in SLEEP mode				
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss		V	See section on Power-on Reset for details				
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss		V	See section on Power-on Reset for details				
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	_	V/ms	See section on Power-on Reset for details				
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	_	_	V/ms	See section on Power-on Reset for details				
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared				
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.35	V	BOREN configuration bit is cleared				
D010	IDD	Supply Current <sup>(2)</sup>	-	1.2	1.7	mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)*				
			_	500	900	μA	Fosc = 4 MHz, VDD = 3.0V, WDT disabled, XT mode, (Note 4)				
			-	1.0	2.0	mA	Fosc = 10 MHz, VDD = 3.0V, WDT disabled, HS mode, (Note 6)				
				4.0	7.0	mA	FOSC = 20 MHz, VDD = 5.5V, WD1 disabled <sup>*</sup> , HS				
				3.0	0.0 70		Fose = 20 MHz Vpp = 4 5V WDT disabled HS mode				
				55	10	μΛ	Fose = $32 \text{ kHz}$ , VDD = $3.0\text{V}$ , WDT disabled, LP mode				
D010	IDD	Supply Current <sup>(2)</sup>	-	1.2	1.7	mA	Fosc = 4.0 MHz, VDD = 5.5V, WDT disabled, XT mode, ( <b>Note 4</b> )*				
			-	400	800	μA	Fosc = 4.0 MHz, VDD = 2.5V, WDT disabled, XT mode (Note 4)				
			-	35	70	μA	Fosc = 32 kHz, VDD = 2.5V, WDT disabled, LP mode				

#### 12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended) (CONT.)

PIC16C	$\begin{array}{llllllllllllllllllllllllllllllllllll$									
PIC16LC62X/LC62XA/LCR62XA			$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param. No.	Sym	Characteristic	Min Typ† Max Units Conditions							
D040	Vih	Input High Voltage I/O ports with TTL buffer	2.0V	_	1/22	V	VDD = 4.5V to 5.5V			
D041		with Schmitt Trigger input	0.25 VDD + 0.8V		VDD VDD		otherwise			
D041			0.8 VDD	_	VDD	v				
D043 D043A		OSC1 (XT, HS and LP) OSC1 (in RC mode)	0.7 Vdd 0.9 Vdd	—	VDD	V	(Note 1)			
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS			
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	VDD = 5.0V, VPIN = VSS			
	lı∟	Input Leakage Current <sup>(2, 3)</sup> I/O ports (Except PORTA)			±1.0	μA	Vss $\leq$ VPIN $\leq$ VDD, pin at hi-impedance			
D060		PORTA	_	_	±0.5	μA	Vss $\leq$ VPIN $\leq$ VDD, pin at hi-impedance			
D061		RA4/T0CKI	_	_	±1.0	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$			
D063		OSC1, MCLR			±5.0	μΑ	Vss $\leq$ VPIN $\leq$ VDD, XT, HS and LP osc configuration			
	lı∟	Input Leakage Current <sup>(2, 3)</sup>								
					±1.0	μΑ	$Vss \leq V PIN \leq V DD, \ pin \ at \ hi\text{-impedance}$			
D060		PORTA	—	—	±0.5	μA	$Vss \le VPIN \le VDD$ , pin at hi-impedance			
D061		RA4/T0CKI	—	—	±1.0	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$			
D063		OSC1, MCLR	-		±5.0	μA	Vss $\leq$ VPIN $\leq$ VDD, XT, HS and LP osc configuration			
	Vol	Output Low Voltage								
D080		I/O ports	—	—	0.6	V	$IOL = 8.5 \text{ mA}, \text{ VDD} = 4.5 \text{V}, -40^{\circ} \text{ to } +85^{\circ}\text{C}$			
			—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, +125°C			
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	$IOL = 1.6 \text{ mA}, \text{ VDD} = 4.5 \text{V}, -40^{\circ} \text{ to } +85^{\circ}\text{C}$			
			_	—	0.6	V	Iol = 1.2 mA, VDD = 4.5V, +125°C			

These parameters are characterized but not tested.

Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not t tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

## PIC16C62X

#### 12.9 Timing Diagrams and Specifications

#### FIGURE 12-12: EXTERNAL CLOCK TIMING



#### TABLE 12-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
1A	Fosc	External CLKIN Frequency <sup>(1)</sup>	DC	—	4	MHz	XT and RC Osc mode, VDD=5.0V
			DC	—	20	MHz	HS Osc mode
			DC	_	200	kHz	LP Osc mode
		Oscillator Frequency <sup>(1)</sup>	DC	—	4	MHz	RC Osc mode, VDD=5.0V
			0.1	_	4	MHz	XT Osc mode
			1	_	20	MHz	HS Osc mode
			DC	_	200	kHz	LP Osc mode
1	Tosc	External CLKIN Period <sup>(1)</sup>	250	_		ns	XT and RC Osc mode
			50	_		ns	HS Osc mode
			5	—	_	μS	LP Osc mode
		Oscillator Period <sup>(1)</sup>	250	—		ns	RC Osc mode
			250	_	10,000	ns	XT Osc mode
			50	_	1,000	ns	HS Osc mode
			5	_		μS	LP Osc mode
2	Тсү	Instruction Cycle Time <sup>(1)</sup>	1.0	Fosc/4	DC	μS	Tcys=Fosc/4
3*	TosL,	External Clock in (OSC1) High or	100*	—		ns	XT oscillator, Tosc L/H duty cycle
	TosH	Low Time	2*	_		μS	LP oscillator, Tosc L/H duty cycle
			20*	_		ns	HS oscillator, Tosc L/H duty cycle
4*	TosR,	External Clock in (OSC1) Rise or	25*	_		ns	XT oscillator
	TosF	Fall Time	50*	—	—	ns	LP oscillator
			15*	_	_	ns	HS oscillator

**2:** \* These parameters are characterized but not tested.

3: † Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

# **PIC16C62X**

20-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP)



	Units	nits INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	р		.026			0.65	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MO-150 Drawing No. C04-072

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