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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E-XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c621a-04i-so

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C62X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C62X uses a Harvard architecture, in which, program and data are accessed from separate memories using separate busses. This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory. Separating program and data memory further allows instructions to be sized differently than 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (35) execute in a single cycle (200 ns @ 20 MHz) except for program branches.

The PIC16C620(A) and PIC16CR620A address 512 x 14 on-chip program memory. The PIC16C621(A) addresses $1K \times 14$ program memory. The PIC16C622(A) addresses $2K \times 14$ program memory. All program memory is internal.

The PIC16C62X can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C62X has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any Addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C62X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C62X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, bit in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with a description of the device pins in Table 3-1.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral functions for controlling the desired operation of the device (Table 4-1). These registers are static RAM. The Special Function Registers can be classified into two sets (core and peripheral). The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS ⁽¹⁾
Bank 0											
00h	INDF	Addressin register)	ig this locat	on uses co	ntents of FS	SR to addre	ess data me	mory (not a	a physical	XXXX XXXX	XXXX XXXX
01h	TMR0	Timer0 Mo	odule's Reg	ister						xxxx xxxx	uuuu uuuu
02h	PCL	Program (Counter's (F	PC) Least S	Significant B	yte				0000 0000	0000 0000
03h	STATUS	IRP ⁽²⁾	RP1 ⁽²⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h	FSR	Indirect da	ata memory	address po	ointer					xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h-09h	Unimplemented									_	_
0Ah	PCLATH	—	—	—	Write buffe	er for upper	5 bits of pr	ogram coui	nter	0 0000	0 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0	-0
0Dh-1Eh	Unimplemented									_	_
1Fh	CMCON	C2OUT	C10UT	—	—	CIS	CM2	CM1	CM0	00 0000	00 0000
Bank 1											
80h	INDF	Addressin register)	g this locat	ion uses co	ntents of FS	SR to addre	ess data me	mory (not a	a physical	xxxx xxxx	xxxx xxxx
81h	OPTION	RBPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Program (Counter's (F	PC) Least S	ignificant B	yte				0000 0000	0000 0000
83h	STATUS	IRP ⁽²⁾	RP1 ⁽²⁾	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
84h	FSR	Indirect da	ata memory	address po	ointer					xxxx xxxx	uuuu uuuu
85h	TRISA	-	-	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1 1111	1 1111
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
87h-89h	Unimplemented									_	_
8Ah	PCLATH	-	-	—	Write buffe	er for upper	5 bits of pr	ogram coui	nter	0 0000	0 0000
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0	-0
8Dh	Unimplemented									_	_
8Eh	PCON	_	_	_	_	—	—	POR	BOR	0x	uq
8Fh-9Eh	Unimplemented						-		-	_	_
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000

TABLE 4-1: SPECIAL REGISTERS FOR THE PIC16C62X

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown,

 ${\rm q}$ = value depends on condition, shaded = unimplemented

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

2: IRP & RP1 bits are reserved; always maintain these bits clear.

TABLE 5-1:PORTA FUNCTIONS

Name	Bit #	Buffer Type	Function
RA0/AN0	bit0	ST	Input/output or comparator input
RA1/AN1	bit1	ST	Input/output or comparator input
RA2/AN2/VREF	bit2	ST	Input/output or comparator input or VREF output
RA3/AN3	bit3	ST	Input/output or comparator input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0 or comparator output. Output is open drain type.

Legend: ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
05h	PORTA		_		RA4	RA3	RA2	RA1	RA0	x 0000	u 0000
85h	TRISA	_	_	_	TRISA 4	TRISA 3	TRISA 2	TRISA 1	TRISA 0	1 1111	1 1111
1Fh	CMCON	C2OUT	C1OUT	_	_	CIS	CM2	CM1	CM0	00 0000	00 0000
9Fh	VRCON	VREN	VROE	VRR	_	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown

Note: Shaded bits are not used by PORTA.

5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Reading the port register reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-2 shows the effect of two sequential read-modify-write instructions (ex., ${\tt BCF}\,,\;\;{\tt BSF},\; etc.)$ on an I/O port

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-2: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

; Initial PORT settings:	PORTB<7:4> Inpu	ıts					
;	PORTB<3:0> Outp	puts					
; PORTB<7:6> have external ; connected to other circu	. pull-up and are uitry	not					
;							
;	PORT latch PO	ORT pins					
;							
	-						
BCF PORTB, 7	;01pp pppp 11	ipp pppp					
BCF PORTB, 6	;10pp pppp 11	lpp pppp					
BSF STATUS, RPO	;						
BCF TRISB, 7	;10pp pppp 11	lpp pppp					
BCF TRISB, 6	;10pp pppp 10)pp pppp					
;							
; Note that the user may have expected the pin							
; values to be 00pp pppp.	The 2nd BCF cause	ed					
; RB7 to be latched as the	e pin value (High)).					

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-7). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



FIGURE 5-7: SUCCESSIVE I/O OPERATION

6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.



FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

7.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with the RA0 through RA3 pins. The On-Chip Voltage Reference (Section 8.0) can also be an input to the comparators.

The CMCON register, shown in Register 7-1, controls the comparator input and output multiplexers. A block diagram of the comparator is shown in Figure 7-1.

REGISTER 7-1: CMCON REGISTER (ADDRESS 1Fh)

	R-0	R-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
	C2OUT	C10UT	—	—	CIS	CM2	CM1	CM0	
	bit 7							bit 0	
bit 7	C2OUT : Comparator 2 output 1 = C2 VIN+ > C2 VIN- 0 = C2 VIN+ < C2 VIN-								
bit 6	C1OUT : Comparator 1 output 1 = C1 VIN+ > C1 VIN- 0 = C1 VIN+ < C1 VIN-								
bit 5-4	Unimplem	ented: Read	d as '0'						
bit 3	CIS: Comparator Input Switch When CM<2:0>: = 001: 1 = C1 VIN- connects to RA3 0 = C1 VIN- connects to RA0 When CM<2:0> = 010: 1 = C1 VIN- connects to RA3 C2 VIN- connects to RA2 0 = C1 VIN- connects to RA2 0 = C1 VIN- connects to RA0 C2 VIN- connects to RA1								
bit 2-0	CM<2:0>: (Comparator	mode.						
	Logondi								

L	.egend:			
F	R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-	n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

8.0 **VOLTAGE REFERENCE** MODULE

The Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of VREF values and has a power-down function to conserve power when the reference is not being used. The VRCON register controls the operation of the reference as shown in Register 8-1. The block diagram is given in Figure 8-1.

8.1 **Configuring the Voltage Reference**

The Voltage Reference can output 16 distinct voltage levels for each range. The equations used to calculate the output of the Voltage Reference are as follows:

if VRR = 0: VREF = (VDD x 1/4) + (VR<3:0>/32) x VDD

The setting time of the Voltage Reference must be considered when changing the VREF output (Table 12-1). Example 8-1 shows an example of how to configure the Voltage Reference for an output voltage of 1.25V with VDD = 5.0V.

	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	VREN	VROE	Vrr	_	VR3	VR2	VR1	Vr0
	bit 7							bit 0
bit 7	VREN: VREI 1 = VREF C	F Enable ircuit power	ed on					
	0 = VREF C	ircuit powere	ed down, no	IDD drain				
bit 6	VROE: VRE	F Output En	able					
	1 = VREF IS 0 = VREF IS	s output on F s disconnect	cA2 pin ed from RA2	2 pin				
bit 5	VRR: VREF	Range sele	ction	•				
	1 = Low Ra	ange						
hit 1		ange	d aa '0'					
DIC 4	Unimplem	ented: Rea	das U					
bit 3-0	VR<3:0>: \	/REF value s	election $0 \leq$	VR [3:0] ≤ 1	5			
	when VRR	= 1: VREF =	(VR<3:0>/ 2	4) * VDD	0) +) /			
	when VRR	= 0: VREF =	1/4 ^ VDD +	(VR<3:0>/ 3	2) ^ VDD			
	Legend:							
	R = Reada	ıble bit	W = W	/ritable bit	U = Unin	nplemented	bit, read as	'0'
	- n = Value	at POR	'1' = B	it is set	'0' = Bit i	s cleared	x = Bit is u	Inknown
8-1:	VOLTAGE			K DIAGR	۸M			
			16 \$	Stages				
\sim	T			∕		_		
\rightarrow	-여드 _{8R}	R	R	R	R			
			ΔΔΔ .	۸ ۸ ۸	A A A			

REGISTER 8-1: VRCON REGISTER(ADDRESS 9Fh)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented I	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 8-



9.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

9.4.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level for proper operation. To take advantage of the POR, just tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details.

The POR circuit does not produce an internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting".

9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, PWRTE can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

The Power-up Time delay will vary from chip-to-chip and due to VDD, temperature and process variation. See DC parameters for details.

9.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-Up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

9.4.4 BROWN-OUT RESET (BOR)

The PIC16C62X members have on-chip Brown-out Reset circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V refer to VBOR parameter D005 (VBOR) for greater than parameter (TBOR) in Table 12-5. The brown-out situation will RESET the chip. A RESET won't occur if VDD falls below 4.0V for less than parameter (TBOR).

On any RESET (Power-on, Brown-out, Watchdog, etc.) the chip will remain in RESET until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms.

If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-Up Timer will execute a 72 ms RESET. The Power-up Timer should always be enabled when Brown-out Reset is enabled. Figure 9-7 shows typical Brown-out situations.



FIGURE 9-7: BROWN-OUT SITUATIONS

9.4.5 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after POR has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and <u>PWRTE</u> bit status. For example, in RC mode with <u>PWRTE</u> bit erased (<u>PWRT</u> disabled), there will be no time-out at all. Figure 9-8, Figure 9-9 and Figure 9-10 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC16C62X device operating in parallel.

Table 9-4 shows the RESET conditions for some special registers, while Table 9-5 shows the RESET conditions for all the registers.

9.4.6 POWER CONTROL (PCON)/ STATUS REGISTER

The power control/STATUS register, PCON (address 8Eh), has two bits.

Bit0 is $\overline{\text{BOR}}$ (Brown-out). $\overline{\text{BOR}}$ is unknown on Poweron Reset. It must then be set by the user and checked on subsequent RESETS to see if $\overline{\text{BOR}} = 0$, indicating that a brown-out has occurred. The $\overline{\text{BOR}}$ STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (VDD may have gone too low).

Oscillator Configuration	Powe	er-up	Brown-out Reset	Wake-up	
	PWRTE = 0	PWRTE = 1	Brown out Rooot	from SLEEP	
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc	
RC	72 ms		72 ms	_	

TABLE 9-1: TIME-OUT IN VARIOUS SITUATIONS

	TABLE 9-2 :	STATUS/PCON BITS AND THEIR SIGNIFICANCE
--	--------------------	---

POR	BOR	то	PD	
0	Х	1	1	Power-on Reset
0	Х	0	Х	Illegal, TO is set on POR
0	Х	Х	0	Illegal, PD is set on POR
1	0	Х	Х	Brown-out Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown

TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 Value on POR Reset		Value on all other RESETS ⁽¹⁾
83h	STATUS				TO	PD				0001 1xxx	000q quuu
8Eh	PCON		_				_	POR	BOR	0x	uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

TABLE 10-2: PIC16C62X INSTRUCTION S

Mnemonic,		Description	Cycles		14-Bit	Opcode	9	Status	Notes
Operands				MSb			LSb	Affected	
BYTE-ORIE	NTED I	FILE REGISTER OPERATIONS							
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0000	0011	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENT	ED FIL	E REGISTER OPERATIONS	_					-	-
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL A	ND COI	NTROL OPERATIONS	-	-				-	
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO,PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO,PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

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BCF	Bit Clear f	BTFSC	Bit Test, Skip if Clear					
Syntax:	[<i>label</i>]BCF f,b	Syntax:	[<i>label</i>]BTFSC f,b					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$	Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$					
Operation:	$0 \rightarrow (f \le b >)$	Operation:	skip if (f) = 0					
Status Affected:	None	Status Affected:	None					
Encoding:	01 00bb bfff ffff	Encoding:	01 10bb bfff ffff					
Description:	Bit 'b' in register 'f' is cleared.	Description:	If bit 'b' in register 'f' is '0', then the					
Words:	1		next instruction is skipped. If bit 'b' is '0', then the next instruc- tion fetched during the current					
Cycles:	1							
Example	BCF FLAG_REG, 7		instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction.					
	Before Instruction FLAG REG = 0xC7							
	After Instruction	Words:	1					
	FLAG REG = 0x47	Cycles:	1(2)					
	_	Example	HERE BTFSC FLAG,1					
BSF	Bit Set f		TRUE • DE					
Syntax:	[<i>label</i>]BSF f,b		•					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$		Before Instruction PC = address HERE					
Operation:	$1 \rightarrow (f \le b >)$		After Instruction					
Status Affected:	None		PC = address TRUE					
Encoding:	01 01bb bfff ffff		if FLAG<1>=1,					
Description:	Bit 'b' in register 'f' is set.		PC = address FALSE					
Words:	1							
Cycles:	1							
Example	BSF FLAG_REG, 7							

Before Instruction FLAG_REG = 0x0A After Instruction

FLAG_REG = 0x8A

BTFSS	Bit Test f, Skip if Set	CALL	Call Subroutine			
Syntax:	[<i>label</i>]BTFSS f,b	Syntax:	[<i>label</i>] CALL k			
Operands:	$0 \leq f \leq 127$	Operands:	$0 \leq k \leq 2047$			
Operation:	0 ≤ b < 7 skip if (f) = 1 None	Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>			
Encoding:	01 11bb bfff ffff	Status Affected:	None			
Description:	If bit 'b' in register 'f' is '1' then the	Encoding:	10 Okkk kkkk kkkk			
	next instruction is skipped. If bit 'b' is '1', then the next instruc- tion fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.	Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immedi- ate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is			
Words:	1		a two-cycle instruction.			
Cycles:	1(2)	Words:	1			
Example	HERE BTFSS FLAG,1	Cycles:	2			
	TRUE • DE •	Example	HERE CALL THER E			
	Before Instruction PC = address HERE After Instruction if FLAG<1> = 0, PC = address FALSE if FLAG<1> = 1, PC = address TBUE		PC = Address HERE After Instruction PC = Address THERE TOS = Address HERE+1			
	IC- address TRUE	CLRF	Clear f			
		Syntax:	[<i>label</i>] CLRF f			
		Operands:	$0 \le f \le 127$			
		Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$			
		Status Affected:	Z			
		Encoding:	00 0001 1fff ffff			
		Description:	The contents of register 'f' are cleared and the Z bit is set.			
		Words:	1			
		Cycles:	1			
		Example	CLRF FLAG_REG			
			Before Instruction FLAG_REG = 0x5A After Instruction FLAG_REG = 0x00 Z = 1			

11.9 MPLAB ICE 2000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft[®] Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.10 MPLAB ICE 4000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for highend PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICD 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory, and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low cost, run-time development tool, connecting to the host PC via an RS-232 or high speed USB interface. This tool is based on the FLASH PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming[™] (ICSP[™]) protocol, offers cost effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

11.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-Alone mode, the PRO MATE II device programmer can read, verify, and program PICmicro devices without a PC connection. It can also set code protection in this mode.

11.13 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

NOTES:



12.2 DC Characteristics: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LC62XA-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62XA				$ \begin{array}{ c c c c c } \hline \textbf{Standard Operating Conditions (unless otherwise stated)} \\ \hline \textbf{Operating temperature} & -40^{\circ}\text{C} & \leq \text{TA} \leq +85^{\circ}\text{C} \text{ for industrial and} \\ & 0^{\circ}\text{C} & \leq \text{TA} \leq +70^{\circ}\text{C} \text{ for commercial and} \\ & -40^{\circ}\text{C} & \leq \text{TA} \leq +125^{\circ}\text{C} \text{ for extended} \\ \hline \end{array} $							
PIC16LC62XA				$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions				
D010	IDD	Supply Current ^(2, 4)	_	1.2 0.4	2.0 1.2	mA mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)* Fosc = 4 MHz, VDD = 3.0V, WDT disabled, XT mode (Note 4)*				
				1.0 4.0	2.0 6.0	mA mA	Fosc = 10 MHz, VDD = 3.0V, WDT dis- abled, HS mode, (Note 6) Fosc = 20 MHz, VDD = 4.5V, WDT dis-				
			-	4.0 35	7.0 70	mA μA	abled, HS mode Fosc = 20 MHz, VDD = 5.5V, WDT dis- abled*, HS mode Fosc = 32 kHz, VDD = 3.0V, WDT dis- abled. LP mode				
D010	IDD	Supply Current ⁽²⁾	_	1.2	2.0 1.1	mA mA	Fosc = 4 MHz, VDD = 5.5V, WDT disabled, XT mode, (Note 4)* Fosc = 4 MHz, VDD = 2.5V, WDT disabled, XT mode, (Note 4)				
			_	35	70	μA	Fosc = 32 kHz, VDD = 2.5V, WDT dis- abled, LP mode				
D020	IPD	Power-down Current ⁽³⁾	 		2.2 5.0 9.0 15	μΑ μΑ μΑ μΑ	VDD = 3.0V VDD = 4.5V* VDD = 5.5V VDD = 5.5V VDD = 5.5V Extended Temp.				
D020	IPD	Power-down Current ⁽³⁾	 	 	2.0 2.2 9.0 15	μΑ μΑ μΑ μΑ	VDD = 2.5V VDD = 3.0V* VDD = 5.5V VDD = 5.5V Extended Temp.				

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

12.6 DC Characteristics:

PIC16C620A/C621A/C622A-40⁽³⁾ (Commercial) PIC16CR620A-40⁽³⁾ (Commercial)

DC CHARACTERISTICS Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial					
Characteristic	Sym	Min	Тур ⁽¹⁾	Max	Units	Conditions	
Supply Voltage	Vdd	4.5	_	5.5	V	HS Option from 20 - 40 MHz	
Supply Current ⁽²⁾	IDD	_	5.5 7.7	11.5 16	mA mA	Fosc = 40 MHz, VDD = 4.5V, HS mode Fosc = 40 MHz, VDD = 5.5V, HS mode	
HS Oscillator Operating Frequency	Fosc	20	_	40	MHz	OSC1 pin is externally driven, OSC2 pin not connected	
Input Low Voltage OSC1	Vi∟	Vss	_	0.2VDD	V	HS mode, OSC1 externally driven	
Input High Voltage OSC1	Vih	0.8Vdd	_	Vdd	V	HS mode, OSC1 externally driven	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to Vss,

T0CKI = VDD, MCLR = VDD; WDT disabled, HS mode with OSC2 not connected.

3: For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

12.7 AC Characteristics: PIC16C620A/C621A/C622A-40⁽²⁾ (Commercial) PIC16CR620A-40⁽²⁾ (Commercial)

AC CHARACTERISTICS All Pins Except Power Supply Pir		Standard Operating Conditions (unless otherwise stated)Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial					
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions	
External CLKIN Frequency	Fosc	20	_	40	MHz	HS mode, OSC1 externally driven	
External CLKIN Period	Tosc	25		50	ns	HS mode (40), OSC1 externally driven	
Clock in (OSC1) Low or High Time	TosL, TosH	6			ns	HS mode, OSC1 externally driven	
Clock in (OSC1) Rise or Fall Time	TosR, TosF	_	—	6.5	ns	HS mode, OSC1 externally driven	
OSC1↑ (Q1 cycle) to Port out valid	TosH2IoV	_		100	ns	—	
OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TosH2iol	50	_	—	ns		

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: For device operation between DC and 20 MHz. See Table 12-1 and Table 12-2.

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FIGURE 12-16: TIMER0 CLOCK TIMING



TABLE 12-6: TIMER0 CLOCK REQUIREMENTS	TABLE 12-6:	TIMER0 CLOCK REQUIREMENTS
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Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions	
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 Tcy + 20*	—	—	ns	
			With Prescaler	10*	—		ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 Tcy + 20*	—	-	ns	
			With Prescaler	10*	—	-	ns	
42	Tt0P	T0CKI Period		$\frac{\text{TCY} + 40}{\text{N}}^*$	-		ns	N = prescale value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

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NOTES:

APPENDIX A: ENHANCEMENTS

The following are the list of enhancements over the PIC16C5X microcontroller family:

- Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (4K now as opposed to 512 before) and register file (up to 128 bytes now versus 32 bytes before).
- 2. A PC high latch register (PCLATH) is added to handle program memory paging. PA2, PA1, PA0 bits are removed from STATUS register.
- 3. Data memory paging is slightly redefined. STATUS register is modified.
- Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW.
 Two instructions TRIS and OPTION are being phased out, although they are kept for compatibility with PIC16C5X.
- 5. OPTION and TRIS registers are made addressable.
- 6. Interrupt capability is added. Interrupt vector is at 0004h.
- 7. Stack size is increased to 8 deep.
- 8. RESET vector is changed to 0000h.
- RESET of all registers is revisited. Five different RESET (and wake-up) types are recognized. Registers are reset differently.
- 10. Wake-up from SLEEP through interrupt is added.
- 11. Two separate timers, Oscillator Start-up Timer (OST) and Power-up Timer (PWRT) are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
- 12. PORTB has weak pull-ups and interrupt-onchange feature.
- 13. Timer0 clock input, T0CKI pin is also a port pin (RA4/T0CKI) and has a TRIS bit.
- 14. FSR is made a full 8-bit register.
- 15. "In-circuit programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).
- PCON STATUS register is added with a Poweron-Reset (POR) STATUS bit and a Brown-out Reset STATUS bit (BOD).
- 17. Code protection scheme is enhanced such that portions of the program memory can be protected, while the remainder is unprotected.
- 18. PORTA inputs are now Schmitt Trigger inputs.
- 19. Brown-out Reset reset has been added.
- 20. Common RAM registers F0h-FFh implemented in bank1.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16CXX, the user should take the following steps:

- 1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any data memory page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to 0000h.