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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	96 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c621a-20-ss

EPROM-Based 8-Bit CMOS Microcontrollers

Devices included in this data sheet:

Referred to collectively as PIC16C62X.

- PIC16C620 • PIC16C620A
- PIC16C621 • PIC16C621A
- PIC16C622 • PIC16C622A
- PIC16CR620A

High Performance RISC CPU:

- Only 35 instructions to learn
- All single cycle instructions (200 ns), except for program branches which are two-cycle
- Operating speed:
 - DC - 40 MHz clock input
 - DC - 100 ns instruction cycle

Device	Program Memory	Data Memory
PIC16C620	512	80
PIC16C620A	512	96
PIC16CR620A	512	96
PIC16C621	1K	80
PIC16C621A	1K	96
PIC16C622	2K	128
PIC16C622A	2K	128

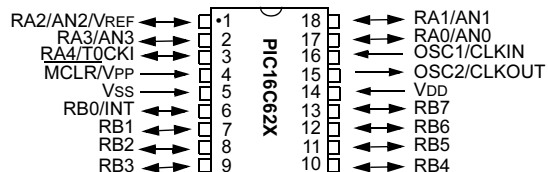
- Interrupt capability
- 16 special function hardware registers
- 8-level deep hardware stack
- Direct, Indirect and Relative addressing modes

Peripheral Features:

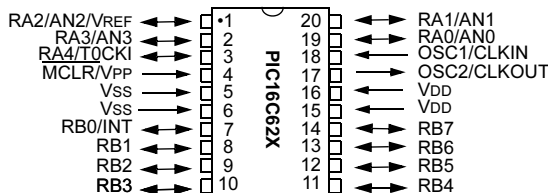
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
 - Two analog comparators
 - Programmable on-chip voltage reference (VREF) module
 - Programmable input multiplexing from device inputs and internal voltage reference
 - Comparator outputs can be output signals
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler

Pin Diagrams

PDIP, SOIC, Windowed Cerdip



SSOP



Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial in-circuit programming (via two pins)
- Four user programmable ID locations

CMOS Technology:

- Low power, high speed CMOS EPROM technology
- Fully static design
- Wide operating range
 - 2.5V to 5.5V
- Commercial, industrial and extended temperature range
- Low power consumption
 - < 2.0 mA @ 5.0V, 4.0 MHz
 - 15 μ A typical @ 3.0V, 32 kHz
 - < 1.0 μ A typical standby current @ 3.0V

PIC16C62X

NOTES:

TABLE 3-1: PIC16C62X PINOUT DESCRIPTION

Name	DIP/SOIC Pin #	SSOP Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	18	I	ST/CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an Active Low Reset to the device.
RA0/AN0	17	19	I/O	ST	PORTA is a bi-directional I/O port. Analog comparator input Analog comparator input Analog comparator input or VREF output Analog comparator input /output Can be selected to be the clock input to the Timer0 timer/counter or a comparator output. Output is open drain type.
RA1/AN1	18	20	I/O	ST	
RA2/AN2/VREF	1	1	I/O	ST	
RA3/AN3	2	2	I/O	ST	
RA4/T0CKI	3	3	I/O	ST	
RB0/INT	6	7	I/O	TTL/ST ⁽¹⁾	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0/INT can also be selected as an external interrupt pin. Interrupt-on-change pin. Interrupt-on-change pin. Interrupt-on-change pin. Serial programming clock. Interrupt-on-change pin. Serial programming data.
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL/ST ⁽²⁾	
RB7	13	14	I/O	TTL/ST ⁽²⁾	
Vss	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: O = output I/O = input/output P = power
 — = Not used I = Input ST = Schmitt Trigger input
 TTL = TTL input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

PIC16C62X

5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The `BCF` and `BSF` instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a `BSF` operation on bit5 of `PORTB` will cause all eight bits of `PORTB` to be read into the CPU. Then the `BSF` operation takes place on bit5 and `PORTB` is written to the output latches. If another bit of `PORTB` is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and re-written to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Reading the port register reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. `BCF`, `BSF`, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-2 shows the effect of two sequential read-modify-write instructions (ex., `BCF`, `BSF`, etc.) on an I/O port.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

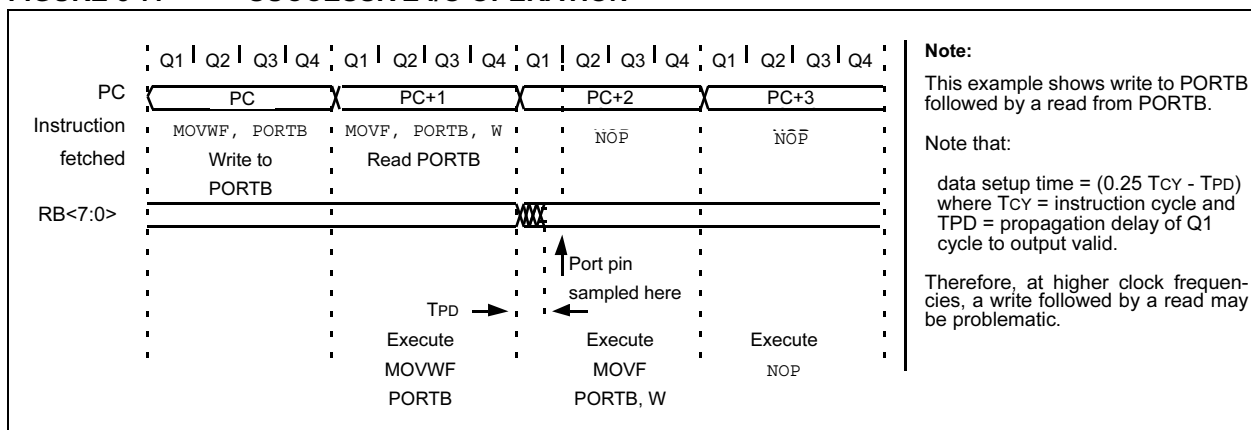
EXAMPLE 5-2: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings:   PORTB<7:4> Inputs
;
;                           PORTB<3:0> Outputs
; PORTB<7:6> have external pull-up and are not
; connected to other circuitry
;
;                           PORT latch  PORT pins
;                           -----  -
;
; BCF PORTB, 7             ; 01pp pppp   11pp pppp
; BCF PORTB, 6             ; 10pp pppp   11pp pppp
; BSF STATUS,RP0           ;
; BCF TRISB, 7             ; 10pp pppp   11pp pppp
; BCF TRISB, 6             ; 10pp pppp   10pp pppp
;
; Note that the user may have expected the pin
; values to be 00pp pppp. The 2nd BCF caused
; RB7 to be latched as the pin value (High).
```

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-7). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

FIGURE 5-7: SUCCESSIVE I/O OPERATION



6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the TMR0 will increment every instruction cycle (without prescaler). If Timer0 is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to TMR0.

Counter mode is selected by setting the T0CS bit. In this mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale value of 1:2, 1:4, ..., 1:256 are selectable. Section 6.3 details the operation of the prescaler.

6.1 TIMER0 Interrupt

Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP, since the timer is shut off during SLEEP. See Figure 6-4 for Timer0 interrupt timing.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM

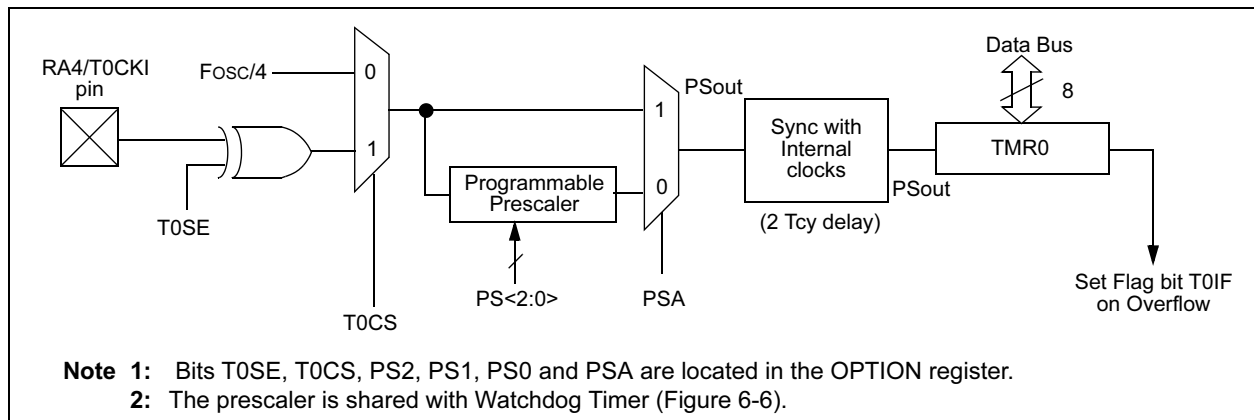
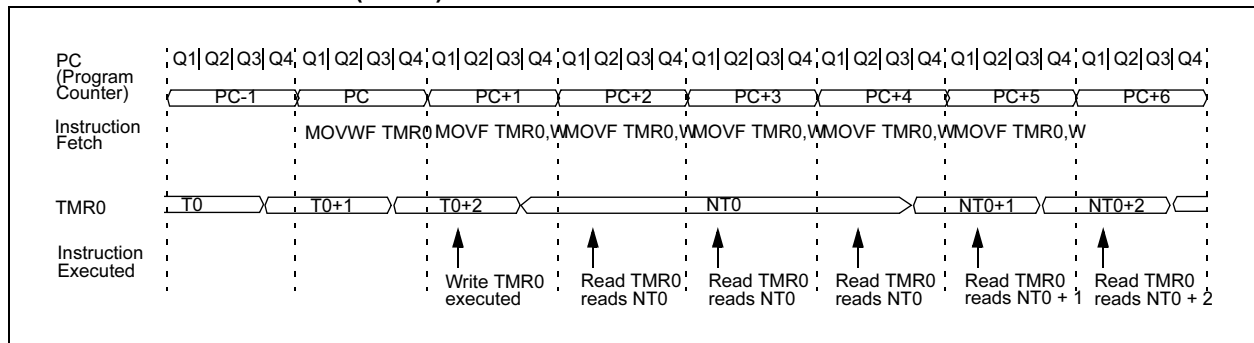


FIGURE 6-2: TIMER0 (TMR0) TIMING: INTERNAL CLOCK/NO PRESCALER



PIC16C62X

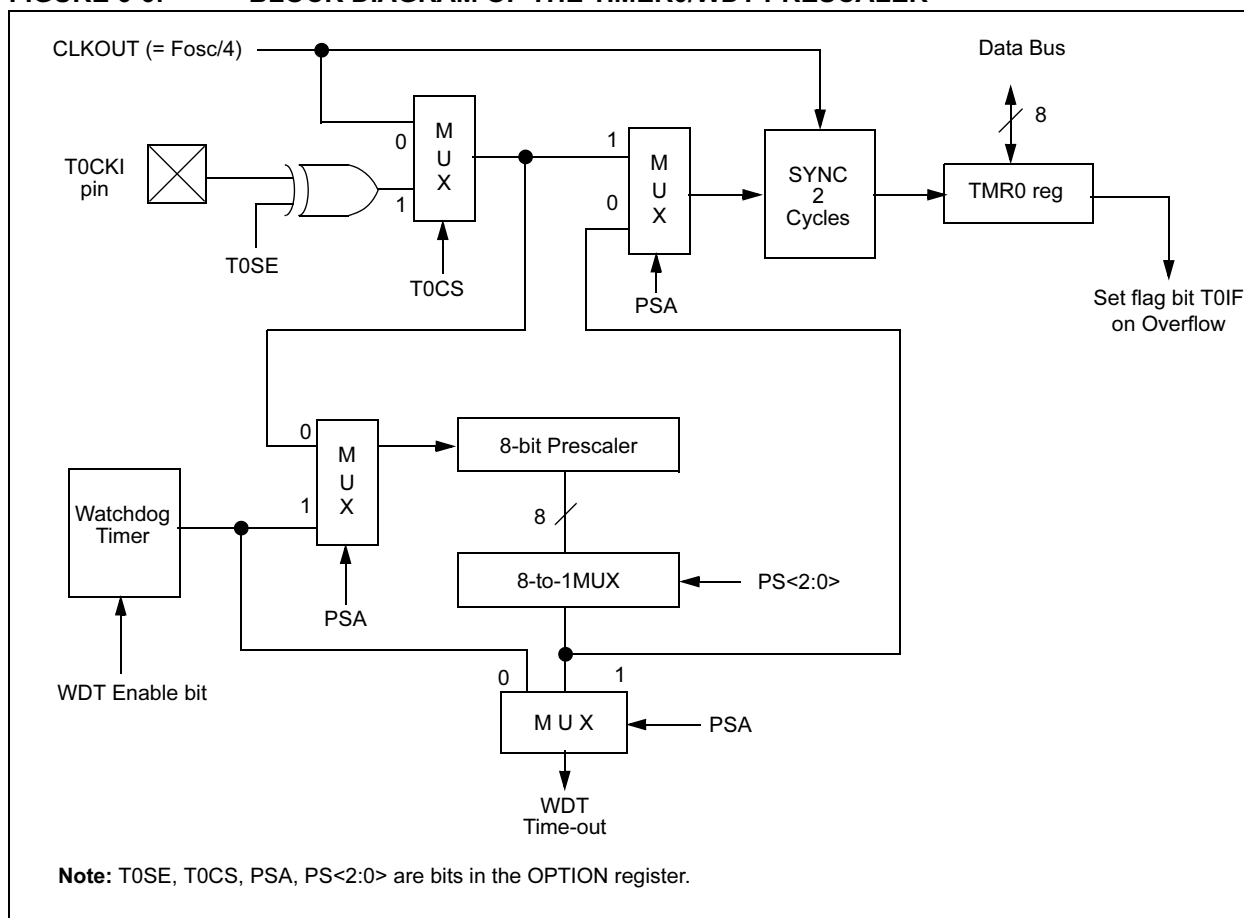
6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscale for the Watchdog Timer, respectively (Figure 6-6). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x...etc.`) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



PIC16C62X

TABLE 7-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
1Fh	CMCON	C2OUT	C1OUT	—	—	CIS	CM2	CM1	CM0	00-- 0000	00-- 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	—	—	—	—	—	-0-- ----	-0-- ----
8Ch	PIE1	—	CMIE	—	—	—	—	—	—	-0-- ----	-0-- ----
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as "0"

PIC16C62X

9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the CLKIN pin. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see

DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The $\overline{\text{TO}}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 9-17: WATCHDOG TIMER BLOCK DIAGRAM

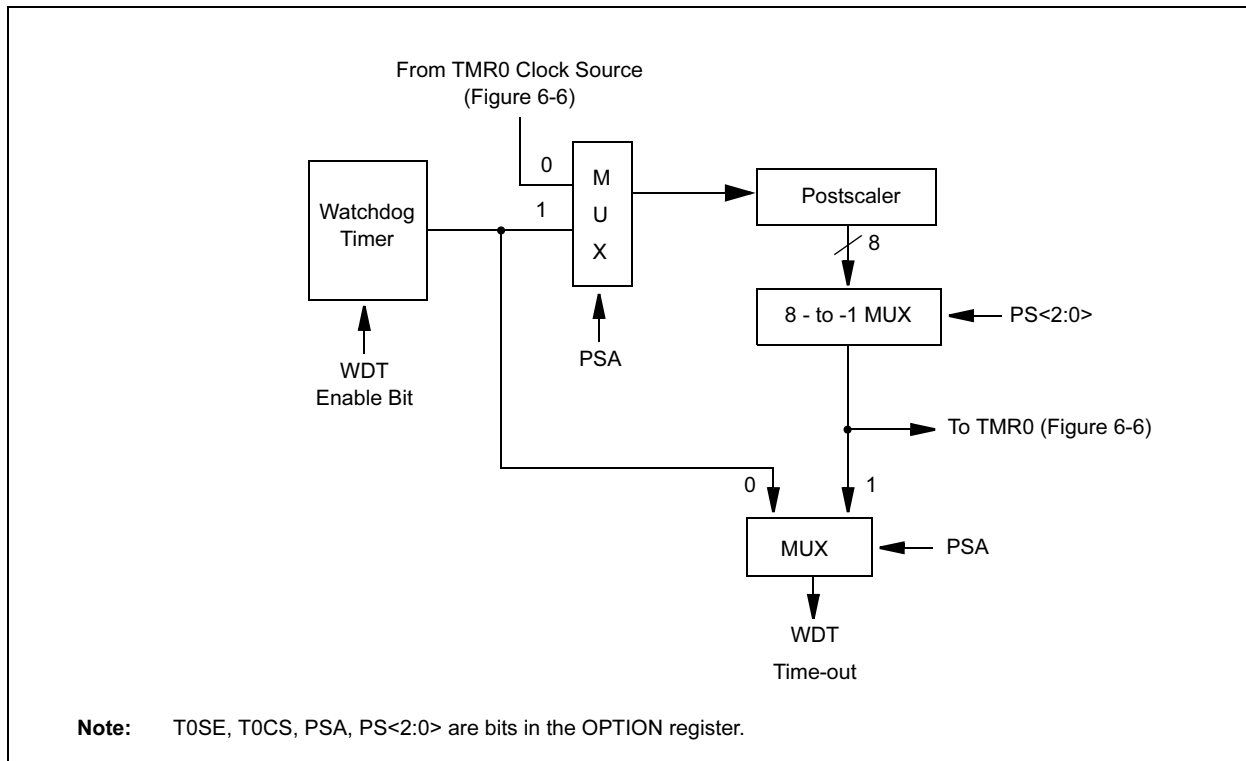


TABLE 9-7: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS
2007h	Config. bits	—	BODEN	CP1	CP0	PWRTE	WDTE	FOSC1	FOSC0	—	—
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: Shaded cells are not used by the Watchdog Timer.

Note: — = Unimplemented location, read as “0”
+ = Reserved for future use

10.1 Instruction Descriptions

ADDLW		Add Literal and W							
Syntax:	[<i>label</i>] ADDLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	$(W) + k \rightarrow (W)$								
Status Affected:	C, DC, Z								
Encoding:	<table><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>					11	111x	kkkk	kkkk
11	111x	kkkk	kkkk						
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.								
Words:	1								
Cycles:	1								
Example	ADDLW 0x15								
	Before Instruction								
	W = 0x10								
	After Instruction								
	W = 0x25								

ADDWF		Add W and f							
Syntax:	[<i>label</i>] ADDWF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	$(W) + (f) \rightarrow (\text{dest})$								
Status Affected:	C, DC, Z								
Encoding:	<table border="1"><tr><td>00</td><td>0111</td><td>dfff</td><td>ffff</td></tr></table>					00	0111	dfff	ffff
00	0111	dfff	ffff						
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.								
Words:	1								
Cycles:	1								
Example	ADDWF FSR, 0								
	Before Instruction								
	W = 0x17								
	FSR = 0xC2								
	After Instruction								
	W = 0xD9								
	FSR = 0xC2								

ANDLW		AND Literal with W						
Syntax:	[<i>label</i>] ANDLW k							
Operands:	$0 \leq k \leq 255$							
Operation:	$(W) .\text{AND}. (k) \rightarrow (W)$							
Status Affected:	Z							
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>				11	1001	kkkk	kkkk
11	1001	kkkk	kkkk					
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.							
Words:	1							
Cycles:	1							
Example	ANDLW 0x5F							
	Before Instruction							
	W = 0xA3							
	After Instruction							
	W = 0x03							

ANDWF		AND W with f						
Syntax:	[<i>label</i>] ANDWF f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	(W) .AND. (f) \rightarrow (dest)							
Status Affected:	Z							
Encoding:	<table border="1"><tr><td>00</td><td>0101</td><td>dfff</td><td>ffff</td></tr></table>				00	0101	dfff	ffff
00	0101	dfff	ffff					
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.							
Words:	1							
Cycles:	1							
Example	ANDWF FSR, 1							
Before Instruction								
W = 0x17								
FSR = 0xC2								
After Instruction								
W = 0x17								
FSR = 0x02								

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of pre-compiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command-line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities, and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, time-keeping, and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high level source debugging with the MPLAB IDE.

11.6 MPLAB ASM30 Assembler, Linker, and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

11.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

11.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high speed simulator is designed to debug, analyze and optimize time intensive DSP routines.

11.9 MPLAB ICE 2000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.10 MPLAB ICE 4000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory, and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low cost, run-time development tool, connecting to the host PC via an RS-232 or high speed USB interface. This tool is based on the FLASH PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

11.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-Alone mode, the PRO MATE II device programmer can read, verify, and program PICmicro devices without a PC connection. It can also set code protection in this mode.

11.13 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

PIC16C62X

FIGURE 12-1: PIC16C62X VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

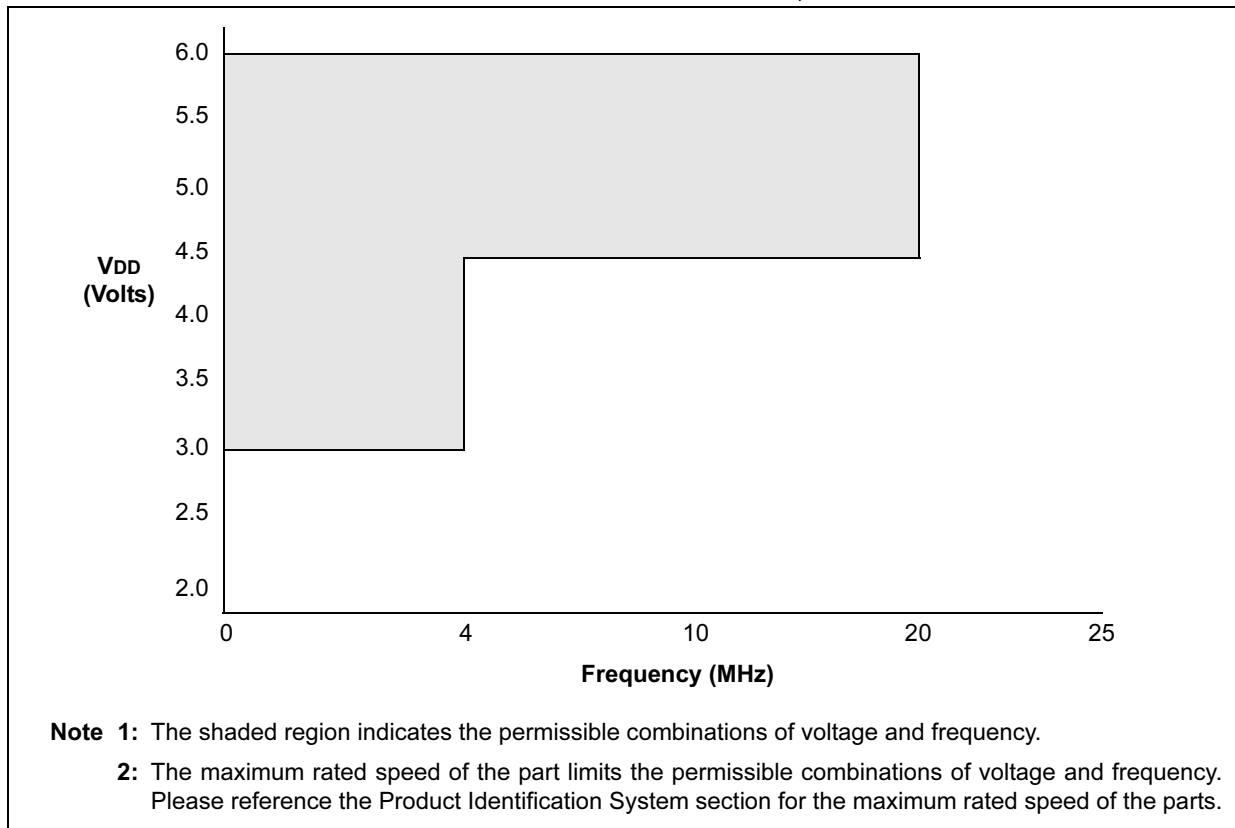


FIGURE 12-2: PIC16LC62X VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

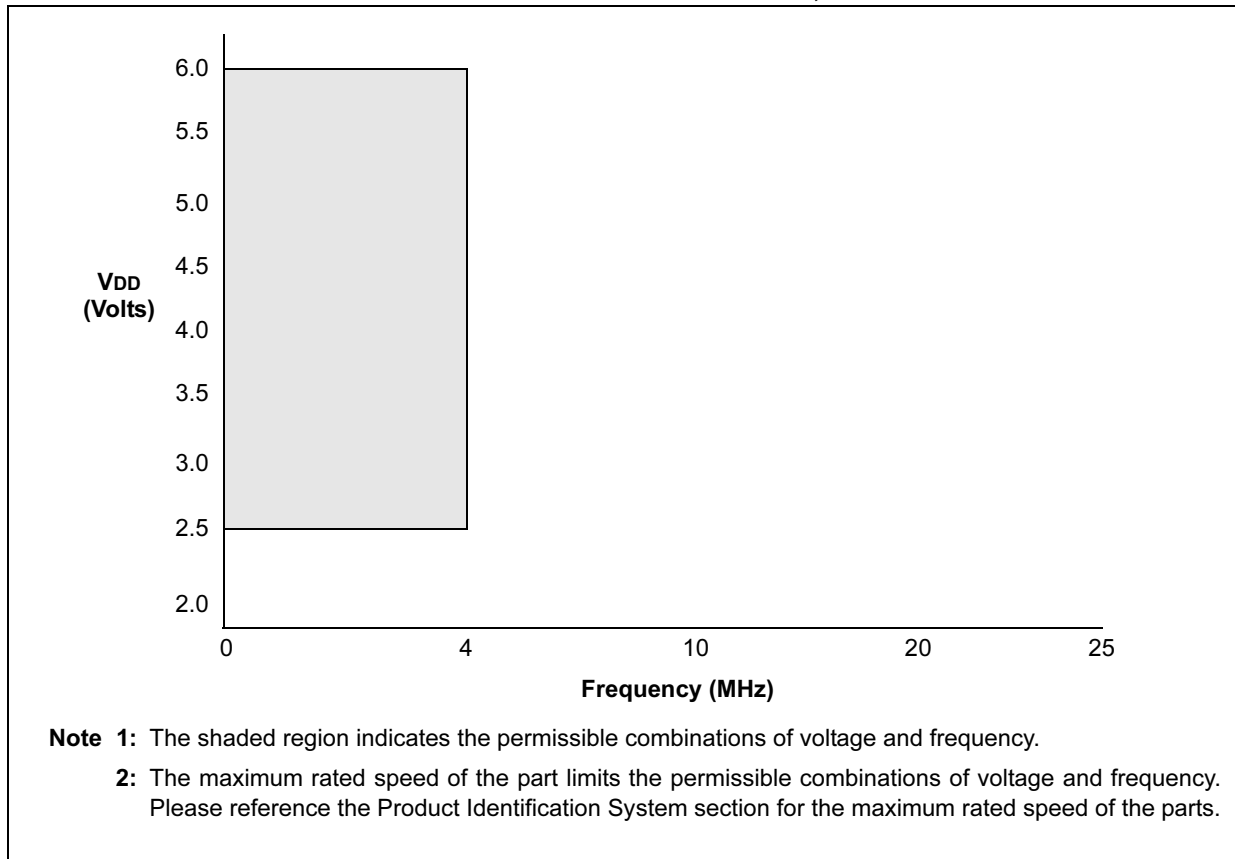


FIGURE 12-7: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

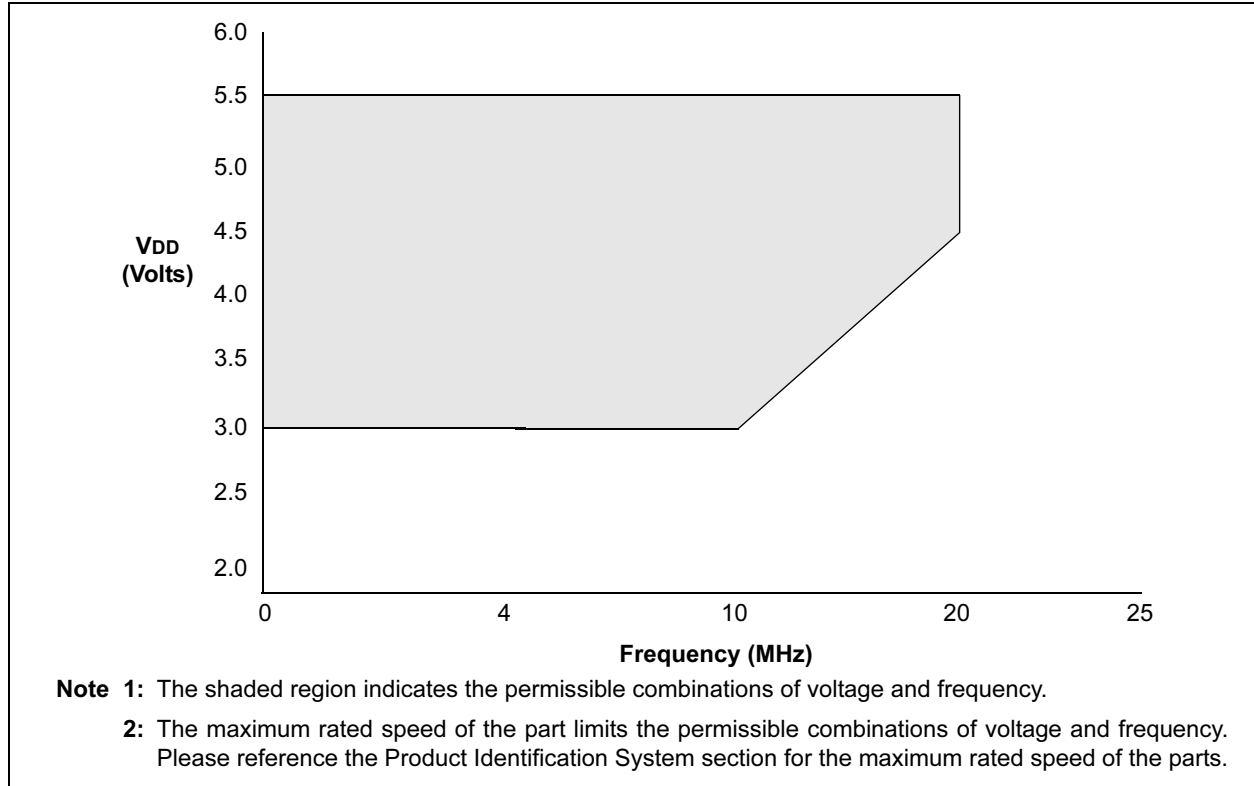
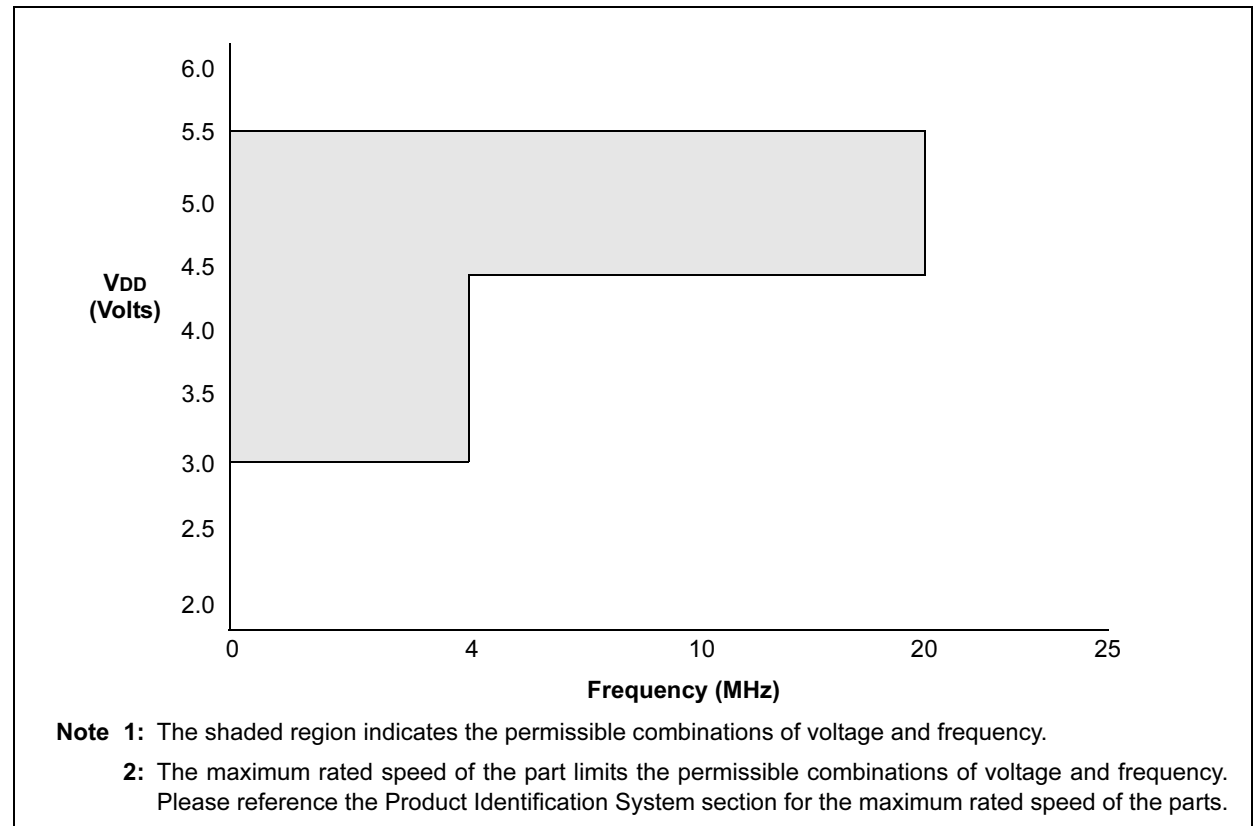


FIGURE 12-8: PIC16CR62XA VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq 0^{\circ}\text{C}$, $+70^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



12.3 DC CHARACTERISTICS: PIC16C62XA-04 (Commercial, Industrial, Extended) PIC16C62XA-20 (Commercial, Industrial, Extended) PIC16LCR62XA-04 (Commercial, Industrial, Extended) (CONT.)

PIC16C62XA-04 PIC16C62XA-20		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
PIC16LCR62XA-04		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D020	IPD	Power-down Current ⁽³⁾	—	200 0.400 0.600 5.0	950 1.8 2.2 9.0	nA μA μA μA	VDD = 3.0V VDD = 4.5V* VDD = 5.5V VDD = 5.5V Extended Temp.
D020	IPD	Power-down Current ⁽³⁾	—	200 200 0.600 5.0	850 950 2.2 9.0	nA nA μA μA	VDD = 2.5V VDD = 3.0V* VDD = 5.5V VDD = 5.5V Extended
D022	ΔI _{WDT}	WDT Current ⁽⁵⁾	—	6.0	10	μA	VDD=4.0V (125°C)
D022A	ΔI _{BOR}	Brown-out Reset Current ⁽⁵⁾	—	75	125	μA	BOD enabled, VDD = 5.0V
D023	ΔI _{COMP}	Comparator Current for each Comparator ⁽⁵⁾	—	30	60	μA	VDD = 4.0V
D023A	ΔI _{VREF}	VREF Current ⁽⁵⁾	—	80	135	μA	VDD = 4.0V
D022	ΔI _{WDT}	WDT Current ⁽⁵⁾	—	6.0	10	μA	VDD=4.0V (125°C)
D022A	ΔI _{BOR}	Brown-out Reset Current ⁽⁵⁾	—	75	125	μA	BOD enabled, VDD = 5.0V
D023	ΔI _{COMP}	Comparator Current for each Comparator ⁽⁵⁾	—	30	60	μA	VDD = 4.0V
D023A	ΔI _{VREF}	VREF Current ⁽⁵⁾	—	80	135	μA	VDD = 4.0V
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures
1A	FOSC	LP Oscillator Operating Frequency	0	—	200	kHz	All temperatures
		RC Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		XT Oscillator Operating Frequency	0	—	4	MHz	All temperatures
		HS Oscillator Operating Frequency	0	—	20	MHz	All temperatures

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: $I_r = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

6: Commercial temperature range only.

12.4 DC Characteristics: PIC16C62X/C62XA/CR62XA (Commercial, Industrial, Extended) PIC16LC62X/LC62XA/LCR62XA (Commercial, Industrial, Extended) (CONT.)

PIC16C62X/C62XA/CR62XA			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
PIC16LC62X/LC62XA/LCR62XA			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D040	V _{IH}	Input High Voltage I/O ports with TTL buffer	2.0V 0.25 V _{DD} + 0.8V	—	V _{DD} V _{DD}	V	V _{DD} = 4.5V to 5.5V otherwise
D041		with Schmitt Trigger input	0.8 V _{DD}	—	V _{DD}		
D042		$\overline{\text{MCLR}}$ RA4/T0CKI	0.8 V _{DD}	—	V _{DD}	V	
D043 D043A		OSC1 (XT, HS and LP) OSC1 (in RC mode)	0.7 V _{DD} 0.9 V _{DD}	—	V _{DD}	V	(Note 1)
D070	I _{PURB}	PORTB weak pull-up current	50	200	400	μA	V _{DD} = 5.0V, V _{PIN} = V _{SS}
D070	I _{PURB}	PORTB weak pull-up current	50	200	400	μA	V _{DD} = 5.0V, V _{PIN} = V _{SS}
D060	I _{IL}	Input Leakage Current ^(2, 3) I/O ports (Except PORTA)			±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D061		PORTA	—	—	±0.5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D063		RA4/T0CKI	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
D063		OSC1, $\overline{\text{MCLR}}$	—	—	±5.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP osc configuration
D060	I _{IL}	Input Leakage Current ^(2, 3) I/O ports (Except PORTA)			±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D061		PORTA	—	—	±0.5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D063		RA4/T0CKI	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
D063		OSC1, $\overline{\text{MCLR}}$	—	—	±5.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP osc configuration
D080	V _{OL}	Output Low Voltage I/O ports	—	—	0.6	V	I _{OL} = 8.5 mA, V _{DD} = 4.5V, -40° to $+85^{\circ}\text{C}$
			—	—	0.6	V	I _{OL} = 7.0 mA, V _{DD} = 4.5V, $+125^{\circ}\text{C}$
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	I _{OL} = 1.6 mA, V _{DD} = 4.5V, -40° to $+85^{\circ}\text{C}$
			—	—	0.6	V	I _{OL} = 1.2 mA, V _{DD} = 4.5V, $+125^{\circ}\text{C}$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. It is not recommended that the PIC16C62X(A) be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

PIC16C62X

12.5 DC CHARACTERISTICS: PIC16C620A/C621A/C622A-40⁽⁷⁾ (Commercial) PIC16CR620A-40⁽⁷⁾ (Commercial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions
D030	V _{IL}	Input Low Voltage I/O ports with TTL buffer	V _{SS}	—	0.8V 0.15V _{DD}	V	V _{DD} = 4.5V to 5.5V, otherwise
D031		with Schmitt Trigger input	V _{SS}	—	0.2V _{DD}	V	(Note 1)
D032		MCLR, RA4/T0CKI, OSC1 (in RC mode)	V _{SS}	—	0.2V _{DD}	V	
D033		OSC1 (in XT and HS) OSC1 (in LP)	V _{SS} V _{SS}	— —	0.3V _{DD} 0.6V _{DD} - 1.0	V V	
D040	V _{IH}	Input High Voltage I/O ports with TTL buffer	2.0V 0.25 V _{DD} + 0.8	—	V _{DD} V _{DD}	V	V _{DD} = 4.5V to 5.5V, otherwise
D041		with Schmitt Trigger input	0.8 V _{DD}	—	V _{DD}	V	(Note 1)
D042		MCLR RA4/T0CKI	0.8 V _{DD}	—	V _{DD}	V	
D043		OSC1 (XT, HS and LP)	0.7 V _{DD}	—	V _{DD}	V	
D043A		OSC1 (in RC mode)	0.9 V _{DD}	—			(Note 1)
D070	IPURB	PORTB Weak Pull-up Current	50	200	400	μA	V _{DD} = 5.0V, V _{PIN} = V _{SS}
D060	I _{IL}	Input Leakage Current ^(2, 3) I/O ports (except PORTA)	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D061		PORTA	—	—	±0.5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , pin at hi-impedance
D063		RA4/T0CKI	—	—	±1.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
		OSC1, MCLR	—	—	±5.0	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP osc configuration
D080	V _{OL}	Output Low Voltage I/O ports	—	—	0.6	V	I _{OL} = 8.5 mA, V _{DD} = 4.5V, -40° to +85°C
			—	—	0.6	V	I _{OL} = 7.0 mA, V _{DD} = 4.5V, +125°C
D083		OSC2/CLKOUT (RC only)	—	—	0.6	V	I _{OL} = 1.6 mA, V _{DD} = 4.5V, -40° to +85°C
			—	—	0.6	V	I _{OL} = 1.2 mA, V _{DD} = 4.5V, +125°C
D090	V _{OH}	Output High Voltage ⁽³⁾ I/O ports (except RA4)	V _{DD} -0.7 V _{DD} -0.7	— —	— —	V V	I _{OH} = -3.0 mA, V _{DD} = 4.5V, -40° to +85°C I _{OH} = -2.5 mA, V _{DD} = 4.5V, +125°C
D092		OSC2/CLKOUT (RC only)	V _{DD} -0.7 V _{DD} -0.7	— —	— —	V V	I _{OH} = -1.3 mA, V _{DD} = 4.5V, -40° to +85°C I _{OH} = -1.0 mA, V _{DD} = 4.5V, +125°C
*D150	V _{OD}	Open Drain High Voltage			8.5	V	RA4 pin
D100	C _{osc2}	Capacitive Loading Specs on Output Pins OSC2 pin			15	pF	In XT, HS and LP modes when external clock used to drive OSC1.
D101	C _{io}	All I/O pins/OSC2 (in RC mode)			50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in Active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

Note 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} or V_{SS}.

Note 4: For RC osc configuration, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD} / 2R_{EXT}$ (mA) with R_{EXT} in kΩ.

Note 5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} or I_{PD} measurement.

Note 6: Commercial temperature range only.

Note 7: See Section 12.1 and Section 12.3 for 16C62X and 16CR62X devices for operation between 20 MHz and 40 MHz for valid modified characteristics.

PIC16C62X

TABLE 12-1: COMPARATOR SPECIFICATIONS

Operating Conditions: VDD range as described in Table 12-1, -40°C<TA<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Typ	Max	Units	Comments
Input offset voltage			± 5.0	± 10	mV	
Input common mode voltage		0		VDD - 1.5	V	
CMRR		+55*			dB	
Response Time ⁽¹⁾			150*	400* 600*	ns ns	PIC16C62X(A) PIC16LC62X
Comparator mode change to output valid				10*	μs	
* These parameters are characterized but not tested.						
Note 1: Response time measured with one comparator input at (VDD - 1.5)/2, while the other input transitions from VSS to VDD.						

TABLE 12-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: VDD range as described in Table 12-1, -40°C<TA<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Typ	Max	Units	Comments
Resolution			VDD/24 VDD/32		LSB LSB	Low Range (VRR=1) High Range (VRR=0)
Absolute Accuracy				±1/4 ±1/2	LSB LSB	Low Range (VRR=1) High Range (VRR=0)
Unit Resistor Value (R)			2K*		Ω	Figure 8-1
Settling Time ⁽¹⁾				10*	μs	
* These parameters are characterized but not tested.						
Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.						

PIC16C62X

TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	— —	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
11*	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	— —	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
12*	TckR	CLKOUT rise time ⁽¹⁾	— —	35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
13*	TckF	CLKOUT fall time ⁽¹⁾	— —	35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
14*	TckL2ioV	CLKOUT ↓ to Port out valid ⁽¹⁾	—	—	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑ ⁽¹⁾	Tosc +200 ns Tosc +400 ns	— —	— —	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
16*	TckH2iol	Port in hold after CLKOUT ↑ ⁽¹⁾	0	—	—	ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	— —	50	150 300	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	— —	— —	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port output rise time	— —	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
21*	TioF	Port output fall time	— —	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
22*	Tinp	RB0/INT pin high or low time	25 40	— —	— —	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
23	Trbp	RB<7:4> change interrupt high or low time	Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

13.0 DEVICE CHARACTERIZATION INFORMATION

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution, while "max" or "min" represents (mean + 3 σ) and (mean - 3 σ) respectively, where σ is standard deviation.

FIGURE 13-1: I_{DD} VS. FREQUENCY (XT MODE, V_{DD} = 5.5V)

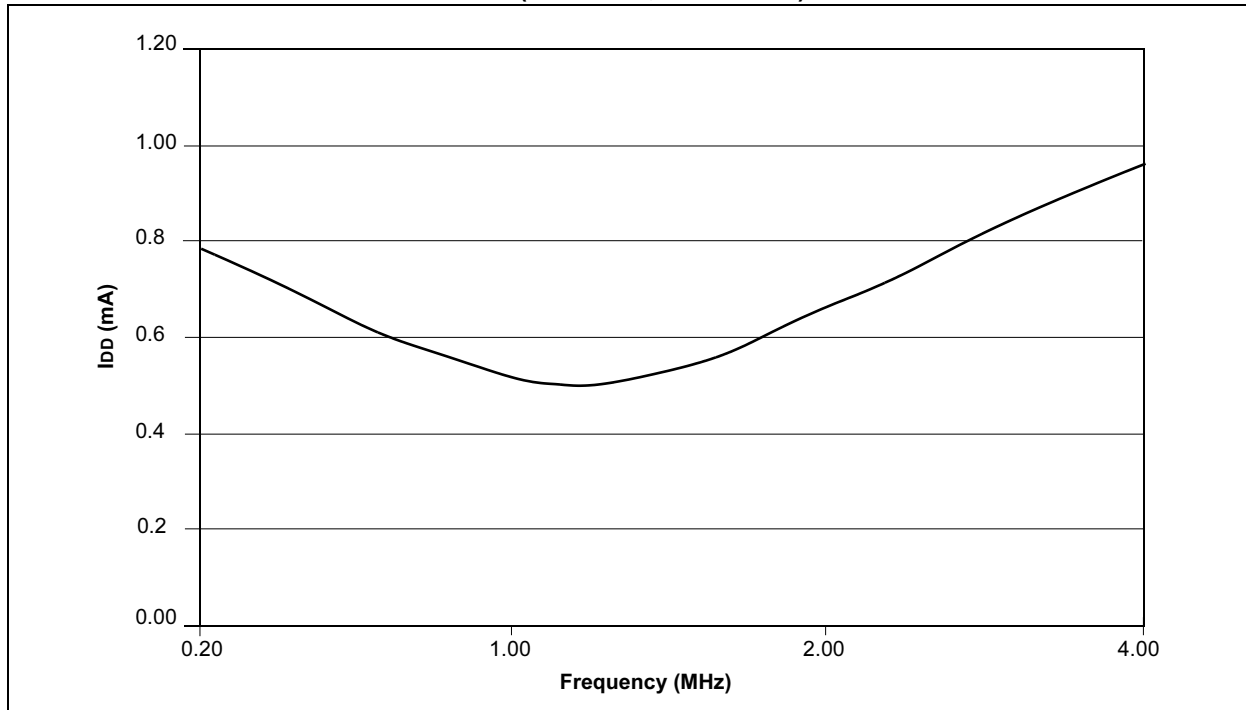
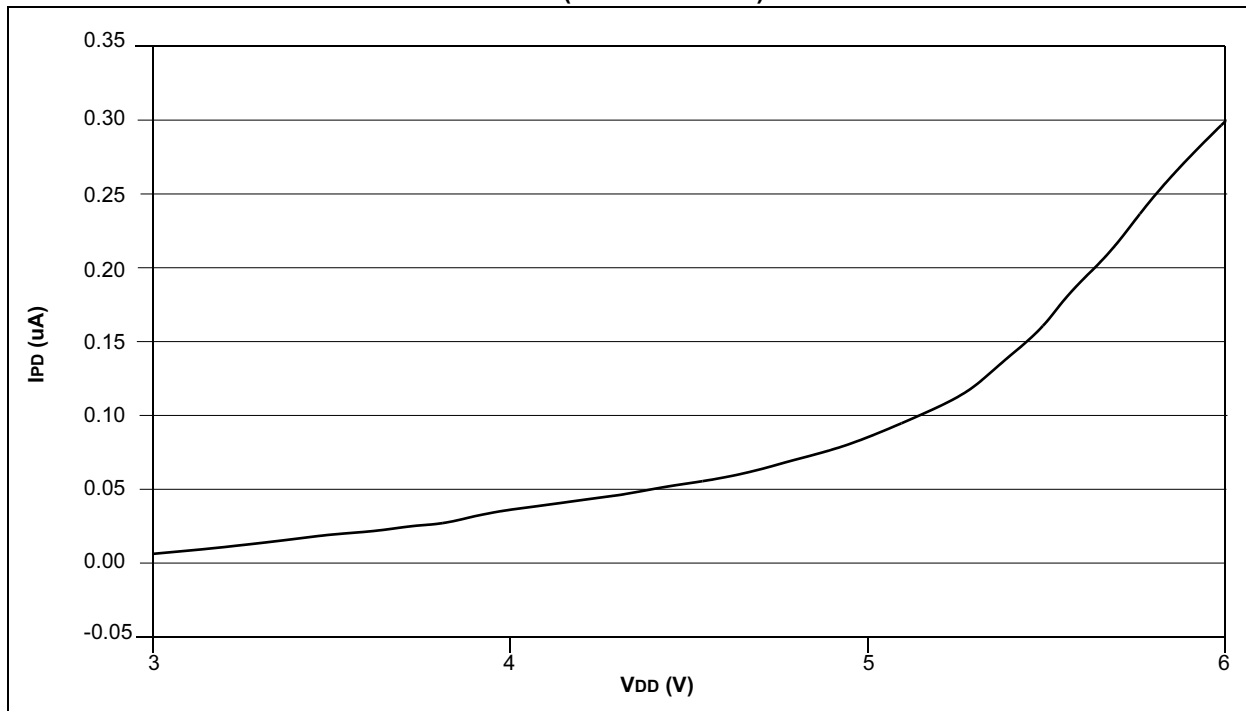


FIGURE 13-2: PIC16C622A I_{PD} VS. V_{DD} (WDT DISABLE)



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