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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	·
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	13
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 6V
Data Converters	·
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c622-04e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

OPTION Register 4.2.2.2

The OPTION register is a readable and writable register, which contains various control bits to configure the TMR0/WDT prescaler, the external RB0/INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note:	To achieve a 1:1 prescaler assignment for
	TMR0, assign the prescaler to the WDT
	(PSA = 1).

REGISTER 4-2:	OPTION REGISTER (ADDRESS 81H)
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RBPU INTEDG TOCS TOSE bit 7 bit 7 RBPU: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual por bit 6 INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin bit 5 TOCS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT) bit 4 TOSE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0 0 = Increment on low-to-high transition on RA4/T0 bit 3 PSA: Prescaler Assignment bit	PSA t latch va DCKI pin DCKI pin	PS2	PS1	PS0 bit 0
bit 7 RBPU: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual por bit 6 INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin 0 = Interrupt on RA4/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT) bit 4 TOSE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0 0 = Increment on low-to-high transition on RA4/T0 bit 3	t latch va DCKI pin DCKI pin	alues		bit 0
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1 = Increment on high-to-low transition on RA4/T0 0 = Increment on low-to-high transition on RA4/T0 bit 3 PSA : Prescaler Assignment bit	CKI pin CKI pin			
0 = Increment on low-to-high transition on RA4/T0 bit 3 PSA : Prescaler Assignment bit	OCKI pin			
bit 3 PSA : Prescaler Assignment bit				
1 = Prescaler is assigned to the WDT				
0 = Prescaler is assigned to the Timer0 module				
bit 2-0 PS<2:0> : Prescaler Rate Select bits				
Bit Value TMR0 Rate WDT Rate				
000 1:2 1:1				
001 1:4 1:2				
101 1:64 1:32				
110 1:128 1:64				
111 1:256 1:128				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for all interrupt sources except the comparator module. See Section 4.2.2.4 and Section 4.2.2.5 for a description of the comparator enable and flag bits.

Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x		
	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF		
	bit 7			<u>.</u>		<u>.</u>		bit 0		
bit 7	GIE: Globa	I Interrupt E	nable bit							
	1 = Enables	1 = Enables all un-masked interrupts								
1.11.0		0 = Disables all interrupts								
0 110	PEIE: Perip		upt Enable i	DIT 	-					
	1 = Enables 0 = Disable	s all un-mas	sked periphe eral interrun	eral interrupt	S					
bit 5		0 Overflow	Interrunt En	able bit						
bit o	1 = Enables	s the TMR0	interrupt							
	0 = Disables the TMR0 interrupt									
bit 4	INTE: RB0/	INT Externa	al Interrupt E	Enable bit						
	1 = Enables	s the RB0/I	NT external	interrupt						
	0 = Disable	0 = Disables the RB0/INT external interrupt								
bit 3	RBIE: RB F	ort Change	Interrupt E	nable bit						
	1 = Enables	s the RB po	rt change in	iterrupt						
L:4 0	0 = Disables the RB port change interrupt									
DIL ∠		J OVernow i		g Dit	- ared in coff	+				
	1 = TMR0 r 0 = TMR0 r	register did	not overflow	(ที่มีประ มีฮ มีฮ /	aleu ili son	ware				
bit 1	INTF: RB0/	INT Externa	al Interrupt F	-lag bit						
	1 = The RB0/INT external interrupt occurred (must be cleared in software)									
	0 = The RB	30/INT exter	nal interrupt	t did not occ	ur					
bit 0	RBIF : RB F	ort Change	Interrupt Fl	lag bit						
	1 = When a	at least one	of the RB<7	':4> pins cha	anged state	(must be cle	ared in soft	ware)		
	0 = None o	f the RB<1	4> pins nave	e changea s	tate					
	Larandi									
	Legend:									

REGISTER 4-3:	INTCON REGISTER (ADDRESS 0BH OR 8BH)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

7.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise the maximum delay of the comparators should be used (Table 12-2).

7.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When the CM<2:0> = 110, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 7-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/ disable for the RA3 and RA4 pins while in this mode.

- Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
 - 2: Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified.

FIGURE 7-3: COMPARATOR OUTPUT BLOCK DIAGRAM



9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC16C62X devices can be operated in four different oscillator options. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (Figure 9-1). The PIC16C62X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (Figure 9-2).

FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



See Table 9-1 and Table 9-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC



TABLE 9-1:CAPACITOR SELECTION FOR
CERAMIC RESONATORS

R	~[]					
Mode	Freq	OSC1(C1)	OSC2(C2)			
ХТ	455 kHz 2.0 MHz 4.0 MHz	22 - 100 pF 15 - 68 pF 15 - 68 pF	82 - 100 pF 15 - 68 pF 15 - 68 pF			
HS	8.0 MHz 16.0 MHz 🔨	10-68 bF 10-22 pF	10 - 68 pF 10 - 22 pF			
Higher capacitance increases the stability of the oscil- lator but also increases the start-up time. These walkes are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.						

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1(C1)	OSC2(C2)			
LP	32 kHz	68 - 100 pF	68 - 100 pF			
	200 kHz	15 - 30 pF	15 - 30 pF			
хт	100 kHz	68 - 150 pF	150 - 300 pF			
	2 MHz	15 - 30 pF	15 - 30 pF			
	4 MHz	15 - 30 pF	15 - 30 pF			
HS	8 MHz	15-30 pF	^V 15 - 30 pF			
	10 MHz	15-30 pF	15 - 30 pF			
	20 MHz 🔨	15-30 pF	15 - 30 pF			
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.						

9.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used; one with series resonance or one with parallel resonance.

Figure 9-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180° phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 9-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT



Figure 9-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 k Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 9-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



9.2.4 RC OSCILLATOR

For timing insensitive applications the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 9-5 shows how the R/C combination is connected to the PIC16C62X. For REXT values below 2.2 k Ω , the oscillator operation may become unstable or stop completely. For very high REXT values (e.g., 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep REXT between 3 k Ω and 100 k Ω .

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 13.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 13.0 for variation of oscillator frequency due to VDD for given REXT/CEXT values, as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (Figure 3-2 for waveform).

FIGURE 9-5: RC OSCILLATOR MODE



9.3 RESET

The PIC16C62X differentiates between various kinds of RESET:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during SLEEP
- d) WDT Reset (normal operation)
- e) WDT wake-up (SLEEP)
- f) Brown-out Reset (BOR)

Some registers are not affected in any RESET condition Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset,

MCLR Reset, WDT Reset and MCLR Reset during SLEEP. They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different RESET situations as indicated in Table 9-2. These bits are used in software to determine the nature of the RESET. See Table 9-5 for a full description of RESET states of all registers.

A simplified block diagram of the on-chip RESET circuit is shown in Figure 9-6.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See Table 12-5 for pulse width specification.





9.5 Interrupts

The PIC16C62X has 4 sources of interrupt:

- External interrupt RB0/INT
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB<7:4>)
- · Comparator interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. GIE is cleared on RESET.

The "return from interrupt" instruction, RETFIE, exits interrupt routine, as well as sets the GIE bit, which reenable RB0/INT interrupts.

The INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flag is contained in the special register PIR1. The corresponding interrupt enable bit is contained in special registers PIE1.

When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h.

FIGURE 9-15: INTERRUPT LOGIC

Once in the interrupt service routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid RB0/ INT recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 9-16). The latency is the same for one or two cycle instructions. Once in the interrupt service routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

- Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.
 - 2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The CPU will execute a NOP in the cycle immediately following the instruction which clears the GIE bit. The interrupts which were ignored are still pending to be serviced when the GIE bit is set again.



TABLE 9-6: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS ⁽¹⁾
0Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	CMIF	—	_	_	—	—	—	-0	-0
8Ch	PIE1	—	CMIE	_	_	_	—	_	_	-0	-0

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

9.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W register and STATUS register). This will have to be implemented in software.

Example 9-3 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 9-3:

- · Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- · Restores the W register

EXAMPLE 9-3: SAVING THE STATUS AND W REGISTERS IN RAM

MOVWF	W_TEMP	;copy W to temp register, ;could be in either bank
SWAPF	STATUS,W	;swap status to be saved into W
BCF	STATUS, RPO	;change to bank 0 regardless ;of current bank
MOVWF	STATUS_TEMP	;save status to bank 0 ;register
:		
:	(ISR)	
:		
SWAPF	STATUS_TEMP, W	;swap STATUS_TEMP register ;into W, sets bank to origi- nal ;state
MOVWF	STATUS	;move W into STATUS register
SWAPF	W_TEMP,F	;swap W_TEMP
SWAPF	W_TEMP,W	;swap W_TEMP into W

BTFSS	Bit Test f, Skip if Set	CALL	Call Subroutine				
Syntax:	[<i>label</i>]BTFSS f,b	Syntax:	[<i>label</i>] CALL k				
Operands:	$0 \leq f \leq 127$	Operands:	$0 \le k \le 2047$				
Operation:	0 ≤ b < 7 skip if (f) = 1	Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCI ATH<4:3>) → PC<12:11>				
Encoding:		Status Affected:	None				
Encouring.	If hit 'h' in register 'f is '1', then the	Encoding:	10 Okkk kkkk kkkk				
Description.	next instruction is skipped. If bit 'b' is '1', then the next instruc- tion fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction.	Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immedi- ate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is				
Words:	1		a two-cycle instruction.				
Cycles:	1(2)	vvords:	1				
Example	HERE BTFSS FLAG,1	Cycles:	2				
	TRUE • DE	Example	HERE CALL THER E				
	Before Instruction PC = address HERE After Instruction if FLAG<1> = 0, PC = address FALSE if FLAG<1> = 1, PC = 1,		PC = Address HERE After Instruction PC = Address THERE TOS = Address HERE+1				
		CLRF	Clear f				
		Syntax:	[<i>label</i>] CLRF f				
		Operands:	$0 \le f \le 127$				
		Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$				
		Status Affected:	<u>Z</u>				
		Encoding:	00 0001 1fff ffff				
		Description:	The contents of register 'f' are cleared and the Z bit is set.				
		Words:	1				
		Cycles:	1				
		Example	CLRF FLAG_REG				
			Before Instruction FLAG_REG = 0x5A After Instruction FLAG_REG = 0x00 Z = 1				

MOVF	Move f									
Syntax:	[<i>label</i>] MOVF f,d									
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$									
Operation:	$(f) \rightarrow (dest)$									
Status Affected:	Z									
Encoding:	00 1000 dfff ffff									
Description:	The contents of register f is moved to a destination dependent upon the status of d. If $d = 0$, destination is W register. If $d = 1$, the destination is file register f itself. $d = 1$ is useful to test a file register since status flag Z is affected.									
Words:	1									
Cycles:	1									
Example	MOVF FSR, 0									
	W = value in FSR register Z = 1									
MOVWF	Move W to f									
Syntax:	[<i>label</i>] MOVWF f									
Operands:	$0 \leq f \leq 127$									
Operation:	$(W) \rightarrow (f)$									
Status Affected:	None									
Encoding:	00 0000 1fff ffff									
Description:	Move data from W register to reg- ister 'f'.									
Words:	1									
Cycles:	1									
Example	MOVWF OPTION									
	Before Instruction OPTION = 0xFF W = 0x4F									
	Atter Instruction OPTION = 0x4F W = 0x4F									

NOP	No Operation								
Syntax:	[label]	NOP							
Operands:	None								
Operation:	No operation								
Status Affected:	None								
Encoding:	00	0000	0xx0	0000					
Description:	No opera	tion.							
Words:	1								
Cycles:	1								
Example	NOP								

OPTION	Load Op	tion Reg	gister							
Syntax:	[label]	OPTION	1							
Operands:	None									
Operation:	$(W) \rightarrow OPTION$									
Status Affected:	None									
Encoding:	00	0000	0110	0010						
Description: Words:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a read- able/writable register, the user can directly address it.									
Cycles:	1									
Example										
	To maintain upward compatibil- ity with future PICmicro [®] products, do not use this instruction.									

11.0 DEVELOPMENT SUPPORT

The PICmicro[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB C30 C Compiler
 - MPLAB ASM30 Assembler/Linker/Library
- · Simulators
 - MPLAB SIM Software Simulator
- MPLAB dsPIC30 Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD 2
- Device Programmers
 - PRO MATE® II Universal Device Programmer
 - PICSTART[®] Plus Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™] 1 Demonstration Board
 - PICDEM.net[™] Demonstration Board
 - PICDEM 2 Plus Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 4 Demonstration Board
 - PICDEM 17 Demonstration Board
 - PICDEM 18R Demonstration Board
 - PICDEM LIN Demonstration Board
 - PICDEM USB Demonstration Board
- Evaluation Kits
 - KEELOQ®
 - PICDEM MSC
 - microID®
 - CAN
 - PowerSmart®
 - Analog

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows[®] based application that contains:

- · An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- · A full-featured editor with color coded context
- · A multiple project manager
- Customizable data windows with direct edit of contents
- · High level source code debugging
- Mouse over variable inspection
- Extensive on-line help
- The MPLAB IDE allows you to:
- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files (assembly or C)
 - absolute listing file (mixed assembly and C)
 - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

11.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- · User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

NOTES:

12.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings †

Ambient Temperature under bias	40° to +125°C
Storage Temperature	65° to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	-0.6V to VDD +0.6V
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0 to +14V
Voltage on RA4 with respect to Vss	8.5V
Total power Dissipation (Note 1)	1.0W
Maximum Current out of Vss pin	
Maximum Current into VDD pin	
Input Clamp Current, Iк (Vi <0 or Vi> VDD)	±20 mA
Output Clamp Current, IOK (Vo <0 or Vo>VoD)	±20 mA
Maximum Output Current sunk by any I/O pin	25 mA
Maximum Output Current sourced by any I/O pin	25 mA
Maximum Current sunk by PORTA and PORTB	
Maximum Current sourced by PORTA and PORTB	
Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD - \sum IOH} + \sum	$\{(VDD-VOH) \times IOH\} + \sum (VOI \times IOL).$

2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16C62X











12.1 DC Characteristics: PIC16C62X-04 (Commercial, Industrial, Extended) PIC16C62X-20 (Commercial, Industrial, Extended) PIC16LC62X-04 (Commercial, Industrial, Extended)

PIC16C	$\begin{array}{c} \textbf{62X} \\ \textbf{62X} \\ \end{array} \begin{array}{l} \textbf{52X} \\ \textbf{62X} \\ \textbf{62X} \\ \textbf{62X} \\ \end{array} \begin{array}{l} \textbf{52X} \\ \textbf{62X} \\ $									
PIC16L	C62X		Stand Oper	Standard Operating Conditions (unless otherwise stated)Operating temperature -40° C \leq TA \leq +85°C for industrial and 0° C \leq TA \leq +70°C for commercial and -40° C \leq TA \leq +125°C for extendedOperating voltage VDD range is the PIC16C62X range.						
Param. No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions			
D001	Vdd	Supply Voltage	3.0		6.0	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5			
D001	Vdd	Supply Voltage	2.5	—	6.0	V	See Figures 12-1, 12-2, 12-3, 12-4, and 12-5			
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode			
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode			
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	Vss	—	V	See section on Power-on Reset for details			
D003	VPOR	VDD start voltage to ensure Power-on Reset	_	Vss	—	V	See section on Power-on Reset for details			
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details			
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details			
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.3	V	BOREN configuration bit is cleared			
D005	VBOR	Brown-out Detect Voltage	3.7	4.0	4.3	V	BOREN configuration bit is cleared			
D010	Idd	Supply Current ⁽²⁾	_	1.8	3.3	mA	Fosc = 4 MHz, Vdd = 5.5V, WDT disabled, XT mode, (Note 4)*			
			—	35	70	μA	Fosc = 32 kHz, VDD = 4.0V, WDT disabled, LP			
			_	9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V, WDT disabled, HS mode			
D010	Idd	Supply Current ⁽²⁾	—	1.4	2.5	mA	Fosc = 2.0 MHz, VDD = 3.0V, WDT disabled, XT mode, (Note 4)			
			-	26	53	μA	Fosc = 32 kHz, VDD = 3.0V, WDT disabled, LP mode			
D020	IPD	Power-down Current ⁽³⁾	—	1.0	2.5 15	μΑ μΑ	VDD=4.0V, WDT disabled (125°C)			
D020	IPD	Power-down Current ⁽³⁾	_	0.7	2	μA	VDD=3.0V, WDT disabled			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in Active Operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD,

 \overline{MCLR} = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula: Ir = VDD/2REXT (mA) with REXT in kΩ.

5: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

TABLE 12-1: COMPARATOR SPECIFICATIONS

Operating Conditions: VDD range as described in Table 12-1, -40°C<TA<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Тур	Мах	Units	Comments
Input offset voltage			± 5.0	± 10	mV	
Input common mode voltage		0		Vdd - 1.5	V	
CMRR		+55*			δβ	
Response Time ⁽¹⁾			150*	400* 600*	ns ns	PIC16C62X(A) PIC16LC62X
Comparator mode change to output valid				10*	μs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2, while the other input transitions from Vss to VDD.

TABLE 12-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions:VDD range as described in Table 12-1, -40°C<TA<+125°C. Current consumption is specified in Table 12-1.

Characteristics	Sym	Min	Тур	Мах	Units	Comments		
Resolution			VDD/24 VDD/32		LSB LSB	Low Range (VRR=1) High Range (VRR=0)		
Absolute Accuracy				<u>+</u> 1/4 <u>+</u> 1/2	LSB LSB	Low Range (VRR=1) High Range (VRR=0)		
Unit Resistor Value (R)			2K*		Ω	Figure 8-1		
Settling Time ⁽¹⁾				10*	μs			
* These parameters are characterized but not tested. Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.								

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Parameter No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾		75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
11*	TosH2ck H	OSC1↑ to CLKOUT↑ ⁽¹⁾	_	75 —	200 400	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
12*	TckR	CLKOUT rise time ⁽¹⁾		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
13*	TckF	CLKOUT fall time ⁽¹⁾		35 —	100 200	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
14*	TckL2ioV	CLKOUT \downarrow to Port out valid ⁽¹⁾	_	_	20	ns	
15*	TioV2ckH	Port in valid before CLKOUT ↑ ⁽¹⁾	Tosc +200 ns Tosc +400 ns	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
16*	TckH2iol	Port in hold after CLKOUT $\uparrow^{(1)}$	0	—		ns	
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	_	50	150 300	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
18*	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100 200	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
19*	TioV2osH	Port input valid to OSC1 [↑] (I/O in setup time)	0	_	—	ns	
20*	TioR	Port output rise time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
21*	TioF	Port output fall time	_	10 —	40 80	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
22*	Tinp	RB0/INT pin high or low time	25 40	_	_	ns ns	PIC16C62X(A) PIC16LC62X(A) PIC16CR62XA PIC16LCR62XA
23	Trbp	RB<7:4> change interrupt high or low time	Тсү	—	—	ns	

TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

14.0 PACKAGING INFORMATION

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)



	Units	INCHES*			MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		18			18		
Pitch	р		.100			2.54		
Top to Seating Plane	А	.170	.183	.195	4.32	4.64	4.95	
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19	
Standoff	A1	.015	.023	.030	0.38	0.57	0.76	
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26	
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49	
Overall Length	D	.880	.900	.920	22.35	22.86	23.37	
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81	
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30	
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52	
Lower Lead Width		.016	.019	.021	0.41	0.47	0.53	
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80	
Window Width		.130	.140	.150	3.30	3.56	3.81	
Window Length	W2	.190	.200	.210	4.83	5.08	5.33	

* Controlling Parameter
 § Significant Characteristic
 JEDEC Equivalent: MO-036
 Drawing No. C04-010

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